IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

PACT XPP SCHWEIZ AG, *Plaintiff* v. **INTEL CORPORATION,** *Defendant*	Case No. 1:19-cv-01006-JDW

MEMORANDUM

On May 30, 2019, Plaintiff PACT XPP Schweiz AG filed suit against defendant Intel Corporation, alleging infringement of 12 of its patents. The patents relate to multi-core processing systems and, more specifically, reconfigurable data processing architectures. The parties have submitted to the Court for construction 10 terms from eight of the patents in suit, Patent Nos. 7,928,763 ("the '763 patent"); 8,312,301 ("the '301 patent"); 8,471,593 ("the '593 patent"); 8,819,505 ("the '505 patent"); 9,075,605 ("the '605 patent"); 9,170,812 ("the '812 patent"); 9,436,631 ("the '631 patent"); and 9,552,047 ("the '047 patent").

I. LEGAL STANDARD

"It is a bedrock principle of patent law that the claims of a patent define the invention to which the patentee is entitled the right to exclude." *Phillips v. AWS Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (quote omitted). Claim construction is a matter of law. *See Teva Pharm. USA v. Sandoz, Inc.*, 135 S. Ct. 831, 837 (2015). There is no "magic formula or catechism" for construing a

patent claim, nor is a court barred from considering "any particular sources or required to analyze sources in any specific sequence." *Phillips*, 415 F.3d at 1323. Instead, a court is free to attach the appropriate weight to appropriate sources "in light of the statutes and policies that inform patent law." *Id.*

A court generally gives the words of a claim their ordinary and customary meaning, which is the "meaning that the term would have to a person of ordinary skill in the art at the time of the invention, i.e., as of the effective filing date of the patent application." *Id.* at 1312-13 (quote omitted). Usually, a court first considers the claim language; then the remaining intrinsic evidence; and finally, the extrinsic evidence in limited circumstances. *See, e.g., Interactive Gift Exp., Inc. v. Compuserve, Inc.*, 256 F.3d 1323, 1331 (Fed. Cir. 2001). While "the claims themselves provide substantial guidance as to the meaning of particular claim terms," a court also must consider the context of the surrounding words. *Id.* at 1314. In addition, the patent specification is "always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term." *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996). But, while a court must construe claims to be consistent with the specification, the court must "avoid the danger of reading limitations from the specification into the claim," *Phillips,* 415 F.3d at 1323. This is a "fine" distinction. *Comark Communications, Inc. v. Harris Corp.,* 156 F.3d 1182, 1186–87 (Fed.Cir.1998). In addition, "[e]ven when the specification describes only a single embodiment, the claims of the patent will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using

words or expressions of manifest exclusion or restriction. *Hill-Rom Svcs., Inc. v. Stryker Corp.*, 755 F.3d 1367, 1372 (Fed. Cir. 2014) (quote omitted).

A court may refer to extrinsic evidence only if the disputed term's ordinary and accustomed meaning cannot be discerned from the intrinsic evidence. *Vitronics,* 90 F.3d at 1584. Although a court may not use extrinsic evidence to vary or contradict the claim language, extrinsic materials "may be helpful to explain scientific principles, the meaning of technical terms, and terms of art that appear in the patent and prosecution history. . .." *Markman v. Westview Instruments, Inc.,* 52 F.3d 967, 980 (Fed. Cir. 1995). Extrinsic evidence is used "to ensure that the court's understanding of the technical aspects of the patent is consistent with that of a person of skill in the art." *Phillips,* 415 F.3d at 1318. The Federal Circuit has cautioned against relying upon expert reports and testimony that is generated for the purpose of litigation because of the likelihood of bias. *Id.*; *see also Daubert v. Merrell Dow Pharms., Inc.,* 509 U.S. 579, 595, 113 S.Ct. 2786, 125 L.Ed.2d 469 (1993) ("Expert evidence can be both powerful and quite misleading because of the difficulty in evaluating it.")

Ultimately, the "construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be . . . the correct construction." *Renishaw PLC v. Marposs Societa' per Anzioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998). It follows that a "claim interpretation that would exclude the inventor's device is rarely the correct interpretation." *Osram GmbH v. Int'l Trade Comm'n*, 505 F.3d 1351, 1358 (Fed. Cir. 2007) (quote omitted).

II. CONSTRUCTION OF DISPUTED TERMS

A. '763 Patent Terms

1. "A multi-processor chip, comprising" (Preamble of claims 1, 31)

PACT Limiting
INTEL Not limiting
COURT Not limiting

Preamble language that "merely states the purpose or intended use of an invention is generally not treated as limiting the scope of the claim." *Pacing Tech., LLC v. Garmin Intern., Inc.*, 778 F.3d 1021, 1023-24 (Fed. Cir. 2015) (quote omitted). "However, when limitations in the body of the claim rely upon and derive antecedent basis from the preamble, then the preamble may act as a necessary component of the claimed invention." *Id.* (cleaned up; quote omitted). That is, the preamble is limiting if it "recites essential structure or steps, or if it is necessary to give life, meaning, and vitality to the claim." *Catalina Mktg. Int'l, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002) (quote omitted). There is no "litmus test" to determine whether preamble language is limiting. *Bicon, Inc. v. Straumann Co.*, 441 F.3d 945, 952 (Fed. Cir. 2006). Whether to treat a preamble term as a claim limitation is "determined on the facts of each case in light of the claim as a whole and the invention described in the patent." *Storage Tech. Corp. v. Cisco Sys., Inc.,* 329 F.3d 823, 831 (Fed. Cir. 2003).

The preamble to these claims does not animate the claims and is not limiting. The body of each claim lacks any reference to the preamble. To the

contrary, the body of each claim describes a complete system on its own. The language in the preamble is a descriptor, not a limitation.

Pact argues that the preamble must be limiting because two dependent claims, Claims 20 and 50, refer back to it. It is possible that the preamble is limiting as to those dependent claims. That question is not before the Court. However, language in a preamble can be limiting as to a dependent claim but not as to the independent claim from which it derives. *See TQ Delta, LLC v. 2WIRE, Inc.*, Civ A. No. 1:13-cv-01835, 2018 WL 4062617, at * 4-5 (D. Del. Aug. 24, 2018). So, even if the preamble is limiting as to dependent Claims 20 and 50, it is not limiting as to independent Claims 1 and 31.

Pact also argues that the specification requires the components to be internal to a single chip and that the preamble provides that specificity. The preamble refers to "**a**" chip. (D.I.90-8 at Claims 1, 31 (emphasis added).) "[A]n indefinite article 'a' or 'an' in patent parlance carries the meaning of 'one or more' in open-ended claims containing the transitional phrase 'comprising.'" *Baldwin Graphic Sys., Inc. v. Siebert, Inc.*, 512 F.3d 1338, 1342 (Fed. Cir. 2008). Pact argues that this rule does not apply to preambles, but it offers no support for that position. The Court sees no reason not to apply the rule to a preamble. Pact also argues that the specification's reference to external components, such as a hard drive, demonstrates that in this case "a" really means "one." Pact reads too much into the specification. The claims describe a complete system. There will always be components that are external to that system. That would be true whether the claims require a single chip or permitted multiple chips. Because

the claim and specification leave open the possibility of a multi-chip system with all of the claimed elements, the specification does not require deviation from the ordinary rules of construction.

2. "Programmably[/dynamically] interconnecting at runtime at least one of data processing cells and memory cells and one or more of the at least one interface unit" (Claims 1, 31)

PACT Connect at least one data processing cell, at least one memory cell, and at least one interface unit with each other at runtime Programmably and dynamically do not require construction
INTEL Programmably reconfiguring interconnects at runtime/dynamically reconfiguring interconnects at runtime
COURT Variably interconnecting at runtime at least one of data processing cells and memory cells and one or more of the at least one interface unit

The Parties agree that the terms "programmably" and "dynamically" are interchangeable and that the claim language requires reconfigurability. (Tr. at 11-12.[1]) They also agreed during the *Markman* hearing to construe words after "runtime" according to their plain and ordinary meaning. (*Id.* at 12-13.) The Court will adopt that agreed-upon construction.

The '763 patent specification indicates that reconfigurable architecture refers to "units [] having a plurality of elements whose function and/or interconnection is variable during run time." (D.I. 90-8 at 1:26-28.) The Court's construction assigns a single meaning to the terms "programmably" and

[1] Citations to "Tr." refer to the Transcript of the *Markman* hearing on June 10, 2020.

"dynamically," consistent with the specification's mandate that interconnection be "variable." *See Vitronics*, 90 F.3d at 1582 ("The specification acts as a dictionary when it expressly defines terms used in the claims."). At the same time, the Court's construction maintains the claim language's mandate that the variable interconnection occur at "runtime," and it preserves the elements that are subject to interconnection. The Court's construction also eliminates potential confusion from the fact that the two claims use two different words—"programmably" and "dynamically"—to mean the same thing.

Intel's proposal would have the Court add the word "reconfiguring" to the construction of "programmably" and "dynamically." Doing so would not add anything. The Court's construction already requires a variable interconnection at runtime. That necessarily means there will be reconfiguration. Adding the word "reconfiguring" does not change anything. It only introduces ambiguity because it suggests that there is some additional requirement above and beyond the variable interconnection.

3. "Data processing cells, each adapted for sequentially executing" (Claims 1, 31)

PACT Plain and ordinary meaning; no construction necessary
INTEL Reconfigurable processor function cells adapted for sequentially executing
COURT Plain and ordinary meaning; no construction necessary

This claim language does not require construction. There is no ambiguity in what is disclosed, nor is it subject to multiple possible interpretations. It is a basic principle of patent law that the patent claims define the invention to which

the patentee is entitled the right to exclude. Thus, "a claim construction analysis must begin and remain centered on the claim language itself, for that is the language the patentee has chosen to particularly point out and distinctly claim the subject matter which the patentee regards as his invention." *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1116 (Fed. Cir. 2004) (cleaned up).

Intel argues that the Court should introduce the word "reconfigurable" to the construction. But nothing in the patent suggests that the data processing cells themselves must be reconfigurable. Quite the opposite. The specification explains that the "term reconfigurable architecture is understood to refer to units [] having a plurality of elements **whose function and/or interconnection is variable during run time.**" (D.I. No. 90-8 at 1:26-28 (emphasis added).) This language demonstrates that the data processing cells themselves do not have to be reconfigurable. The interconnection can be, instead. In other places, the specification reiterates that something other than the data processing cells can satisfy the reconfigurability requirement. (*E.g.*, *id.* at 7:22-25 (describing ways to enable sequencer-type data processing but omitting any requirement that function cells be reconfigurable).) While "[i]t is entirely proper to use the specification to interpret what the patentee meant by a word or phrase in the claim," it is improper to add an extraneous limitation appearing in the specification into a claim "wholly apart from any need to interpret what the patentee meant by particular words or phrases in the claim." *E.I. du Pont de Nemours & Co. v. Phillips Petroleum Co.*, 849 F.2d 1430, 1433 (Fed. Cir. 1988)

(quote omitted); *Phillips v. AWH Corp.*, 415 F.3d 1303, 1323 (Fed. Cir. 2005)("To avoid importing limitations from the specification into the claims, it is important to keep in mind that the purposes of the specification are to teach and enable those of skill in the art to make and use the invention and to provide a best mode for doing so.") But that is exactly what Intel would have this Court do.

Intel also points to Figure 1 of the '763 patent, for which the specification makes clear that "the particular functions of function cells are configurable." (D.I. No. 90-8 at 7:56-57) Figure 1 is only one of the many embodiments in the patent. The Federal Circuit has warned against "read[ing] limitations from the specification into claims" when "the only embodiments, or all of the embodiments, contain a particular limitation." *Thorner v. Sony Computer Entm't Am. LLC*, 669 F.3d 1362, 1366 (Fed. Cir. 2012).

B. '593 Patent Term—"A data processor on a chip comprising" (Preamble of claims 1, 16)

PACT Limiting
INTEL Not limiting
COURT Limiting as to "data processor"

The preamble to these claims refers to a "data processor on a chip comprising . . .." (D.I. No. 90-8 at 12:19.) The claim then describes, among other things, "at least one interface unit for providing at least one communication channel between **the data processor** and external memory." (*Id.* at 12:28-30 (emphasis added).) The term "data processor" in the preamble provides antecedent basis for the term "data processor" in the body of the claim.

Therefore, that term is limiting. *See Pacing Tech.*, at 778 F.3d at 1024. Although the term "data processor" is limiting, neither party seems to think that the term requires anything other than its plain and ordinary meaning, and the Court agrees.

Pact goes one step further and contends that (a) the entire preamble is limiting and (b) the phrase "on a chip" means that the patent is limited to a single chip. The Court disagrees. A court does not have to construe an entire preamble just because it construes a portion of it. *See TomTom, Inc. v. Adolph*, 790 F.3d 1315, 1323 (Fed. Cir. 2015). Here, nothing in the body of the claim indicates that the phrase "on a chip" is limiting. It does not animate or give life to any aspect of the body of the claim.

Even if the phrase "on a chip" were limiting, it would not help Pact. Pact contends that the phrase indicates that there must be a single chip. But as with the '763 Patent, nothing about the claim language or the specification demonstrates that there must be only one chip. The specification's reference to external components only stands for the non-controversial proposition that some components will be external to the system disclosed in the claim. Those external components could exist if there is a single-chip system or a multi-chip system. The specification's reference to external components therefore does not offer a reason to deviate from the normal rules of construction concerning the use of the article "a."

C. '631 Patent Term—"A plurality of bus segments for each processor of the multiprocessor system" (Claim 1)

PACT No construction necessary; plain and ordinary meaning
INTEL A plurality of bus segments for each processor of the multiprocessor system, each bus segment connected to only one of the processors
COURT Plain and ordinary meaning; no construction necessary

The parties agree that, on its face, this language contemplates multiple bus segments for each processor. Intel, however, claims that the prosecution history demonstrates that each bus segment can connect only to a single processor. "The doctrine of prosecution disclaimer . . . preclud[es] patentees from recapturing through claim interpretation specific meanings disclaimed during prosecution." *Mass. Inst. of Tech. v. Shire Pharm., Inc.*, 839 F.3d 1111, 1119 (Fed. Cir. 2016) (quote omitted). "The party seeking to invoke prosecution history disclaimer bears the burden of proving the existence of a 'clear and unmistakable' disclaimer that would have been evident to one skilled in the art." *Trivascular, Inc. v. Samuels*, 812 F.3d 1056, 1063–64 (Fed. Cir. 2016) (quote omitted). The Federal Circuit has declined to find a prosecution disclaimer "[w]here the alleged disavowal is ambiguous, or even 'amenable to multiple reasonable interpretations.'" *Mass. Inst. of Tech.*, 839 F.3d at 1119 (quote omitted).

During prosecution, the examiner initially rejected Claim 1 of the '631 patent on the grounds that it was obvious in light of US Patent No. 5,905,875 (the "Takahashi" reference). Pact distinguished Takahashi by explaining that "each of the bus segments. . . [in] Fig. 1 of Takahashi[] are not provided *for each*

processor, but are rather each connected to *multiple* processors." (D.I. 90-12 at 933 (emphasis in original). Pact contended to the examiner that "Takahashi fails to disclose 'a plurality of bus segments for each processor of the multiprocessor system comprising a plurality of flexible data channels to each processor of the multiprocessor system.'" (*Id.*) Intel interprets Pact's statement as limiting the claim such that "each of the claimed bus segments connects to only one processor." (D.I. 90 at 32).

Intel's proposed interpretation is a reasonable one. Pact's argument to the examiner about Takahashi could limit Claim 1 so that each bus segment could connect to one processor. That interpretation would distinguish the '631 Patent from Takahashi, which contemplates connection to multiple processors. But Intel's proposed interpretation is not the only reasonable interpretation of Pact's arguments to the examiner. Pact's position could also mean that the '631 Patent discloses a system in which each bus segment connects to each processor. Pact's argument to the examiner could be read to disclose more connections than Takahashi, not fewer.

The Court does not have to determine which reading is correct. It just has to determine that Pact's statement was not a clear and unmistakable disavowal. Pact's argument is a reasonable interpretation of the file history. As Pact pointed out during the *Markman* hearing, Takhashi does not show one bus segment for each processor. It shows multiple bus segments connected through bus extender mechanisms that link to many processors, but not necessarily all. In addition, Figures 5 and 6 of the '631 Patent disclose each bus segment connected to many

processors, not just one. While Pact cannot reclaim in the specification what it disavowed, the fact that the specification contemplates an invention that is consistent with Pact's interpretation of the file history at least suggests that Pact's interpretation is a reasonable one. The Court concludes that both Intel's and Pact's readings of the file history are reasonable. That vagueness dooms Intel's disavowal argument.

D. '812 Patent Term—"Instruction dispatch unit . . . configured to dispatch software threads to the array data processor for parallel execution by the parallel processing arithmetic units" (Claim 12)

PACT Plain and ordinary meaning
INTEL Subject to 35 U.S.C. § 112 ¶ 6 Function: Dispatch software threads to the array data processor for parallel execution by the parallel processing arithmetic units Structure: Fig. 80A, configuration unit (CT)
COURT Plain and ordinary meaning; § 112 ¶ 6 does not apply

The parties dispute whether the term "instruction dispatch unit" conveys a structure that a person skilled in the art would have understood at the time of the application (Pact's view) or whether it is defined by its function under 35 U.S.C. § 112, ¶ 6.[2] Courts presume that claim terms without the word "means" do not invoke Section 112, ¶ 6. *See Williamson v. Citrix Online,* LLC, 792 F.3d

[2] The America Invents Act recodifies Section 112, ¶ 6 as 35 U.S.C. § 112(f), but the pre-AIA statute applies here.

1339, 1348 (Fed. Cir. 2015) (en banc).[3] The presumption is not strong. To rebut it, a challenger must demonstrate that a claim term either fails to "recite sufficiently definite structure" or recites "function without reciting sufficient structure for performing that function." *Id.* at 1349. A challenger does not have to show that the limitation is devoid of anything that can be construed as structure. Instead, it only has to show that the structure is not "sufficient." *Id.*; *see also Egenera, Inc. v. Cisco Sys., Inc.*, -- F.3d --, 2020 WL 5084288, at * 3 (Fed. Cir. Aug. 28, 2020). The essential inquiry is "whether the words of the claim are understood by persons of ordinary skill in the art to have a sufficiently definite meaning as the name for structure." *MTD Prod. Inc. v. Iancu*, 933 F.3d 1336, 1341 (Fed. Cir. 2019) (quote omitted).

The Court concludes that the term "instruction dispatch unit" recites a definite structure to one skilled in the art. The term is not used in the patent's lengthy specification, so the intrinsic evidence does not shed any light on its meaning or structure. The extrinsic evidence does, though. Pact has identified patents and treatises that use the term. Intel points out that none of those sources defines the term "instruction dispatch unit." But their repeated use of the term indicates that a person skilled in the art would have understood it, including its structure. In that regard, it is notable that at least some of the sources on which Pact relies do not define "instruction dispatch unit" by its

[3] An *en banc* Federal Circuit joined the portion of the *Williamson* decision discussing the applicability of Section 112. *See Williamson*, 892 F.3d at 1347-49 & n.3.

function. Instead, those sources appear to assume that a person skilled in the art will understand the structure of such a unit. (*E.g.*, D.I. at 2:55-57.)

In addition, Pact's expert Andrew Wolfe explains in his Declaration that an instruction dispatch unit has a structure that a person skilled in the art would understand. Dr. Wolfe provides his understanding of an instruction dispatch unit, and he points to sources on which he bases his opinion. Intel and its expert Todd Mowry criticize Dr. Wolfe's opinion, but they do not do enough to overcome it, given that Intel bears the burden of proving that Section 112, ¶ 6 applies. Dr. Mowry criticizes the litany of sources on which Dr. Wolfe relies, but the Court is persuaded that the wide use of the term in the literature indicates that a person skilled in the art would have understood it at the time. Because the term "instruction dispatch unit" has a known meaning, the case is unlike the one before the Federal Circuit decision in *Deibold*, where the patent used a term with no known structure or meaning. *See Diebold Nixdorf, Inc. v. Int'l Trade Comm'n*, 899 F.3d 1291, 1298-99 (costruing "cheque standby unit").

Intel's other arguments for the application of Section 112, ¶ 6 also fail to satisfy its burden of proof. For example, Intel asserts that the references on which Pact and Dr. Wolfe rely focus on the area of general, rather than reconfigurable, processors. The idea that there is a distinction between the two is the nub of Intel's defense to many of the infringement claims in this case. And it might be true. But Intel has not, at this stage, offered evidence from which the Court can determine that the distinction renders Pact's authorities inapplicable. It would have to offer such evidence to carry its burden of proof.

So too with Intel's distinction between processing threads and instructions. Dr. Mowry asserts, in conclusory fashion, that there is a distinction, and Intel makes the argument that there is. But the Court does not have any evidence, other than Dr. Mowry's say-so, that the distinction matters here. Notably, the patent's specification calls the distinction into doubt. The patent defines threads as "finely granular applications and/or application parts" that are distributed among resources within the processor. (D.I. No. 90-13 at 19:63-65) Nothing in the record suggests that these applications or application parts cannot constitute a set of instructions that an instruction dispatch unit can distribute throughout the processor. To the contrary, extrinsic evidence in the record refers to threads as a series of instructions. (*E.g.*, D.I. 90-6 at 25:46-47 ("Such an instruction may be a single instruction within a thread represented by multiple strands."), 25:59-61 ("A thread may include multiple strands such that instructions of different strands may depend upon each other.")). Without more, Intel has not met its burden. Nor do Intel's other arguments suffice to carry its burden of showing that the "instruction dispatch unit" either lacks structure or lacks a structure to carry out a particular function.

E. '047 Patent Terms

1. Preambles in '047 Patent (Claims 1, 19)

PACT Limiting
INTEL Not limiting
COURT Not limiting

Claim 1 of this patent describes a "multiprocessor system," and claim 19 describes a "mobile device." In each case, the body of the claim then lays out all elements of the claimed system. Nothing in the body of the claims refers back to the preamble. Nor is there anything in the body of the claims that gets life or animation from the preamble. While it is true that certain dependent claims refer back to these preambles, that establishes, at most, that the preamble is limiting as to those dependent claims. It does not provide a basis to deviate from the ordinary rule that preambles are not limiting.

2. "Data processing unit" and/or "data processing units . . . adapted for sequentially processing data" (Claims 1-5, 8, 10, 15, 19, 22, 24)

PACT No construction required, except that "sequentially processing data" means "passing results onto one or more other data processing units which are subsequently processing data"
INTEL Reconfigurable and sequential data processors where the data results from one processor are fed to another, for each processor to perform a separate computation
COURT Sequential data processors that pass results to one or more additional data processing units to perform additional computations

During the prosecution of this patent, Pact limited its invention to sequential data processors. To operate as a disclaimer, the statement in the prosecution history must be clear and unambiguous, and constitute a clear disavowal of scope. *See Trivascular*, 812 F.3d at 1063-64; *Verizon Servs. Corp. v. Vonage Holdings Corp.*, 503 F.3d 1295, 1306 (Fed. Cir. 2007). The examiner rejected all claims in the '047 Patent in light of prior art, Kikinis (U.S. Pat. No.

5,502,838). Pact then amended its application to distinguish Kikinis with the following explanations:

- "Kikinis does not disclose a multiprocessor system comprising sequential data processors. All the Kikinis processors are conventional processors and all the same architecture;"
- "Applicant respectfully submits that **the claims are limited to sequential data processors** that have register sets for storing data for sequential data processing, and neither are disclosed in Kikinis;" and
- "These limitations are significant and define over Kikinis."

(D.I. 90-21 at 14-15 (emphasis added).)

These statements to the examiner constitute a clear, unequivocal disclaimer of scope. Pact's use of definitive language contradicts Pact's argument that these statements are too vague to constitute a disclaimer. Pact also argues that the Court should adopt its interpretation of "sequentially processing data" because the interpretation comes from the patent's specification. Pact also argues that its proposed construction should prevail because it is consistent with the patent's specification. But Pact made representations to the examiner to secure the '047 Patent. It cannot now contradict those representations and use the specification to claw back subject matter that it gave up during prosecution. *See Mass. Inst. Of Tech.*, 839 F.3d at 1119; *Omega Eng'g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1324-28 (Fed. Cir. 2003).

The Parties offer similar definitions of "sequentially processing data." They agree that one data processor performs a computation, and then passes its results on to another processor, which also performs a computation. Pact takes issue with Intel's description of subsequent data processors performing "separate" computations. According to Pact, the word "separate" could cause confusion because it might suggest that there are no dependencies between the data processor calculations. In order to avoid any confusion, the Court refers to "additional" computations, rather than "separation" computations. The word "additional" allows subsequent computations to be independent or dependent of the earlier computations.

As with the '763 Patent, Intel seeks to define the data processors as "reconfigurable." As with that patent, the Court declines to include that term because it ignores the possibility that the interconnections, rather than the cells themselves, can be reconfigurable.

F. '605 Patent Terms

1. "Data processing unit" and/or "data processing units . . . adapted for sequentially processing data" (Claim 1)

The parties briefed this claim term in conjunction with the similar terms for the '047 Patent, which is part of the same family. The Court construes it the same way as it construed this term in the '047 Patent.

2. "To a minimum" (Claim 1)

PACT Plain and ordinary meaning. No construction necessary.
INTEL To a level no more than is required for the preservation of memory contents or the like
COURT Plain and ordinary meaning. No construction necessary.

A court should "indulge a heavy presumption that a claim term carries its ordinary and customary meaning." *Amgen Inc. v. Hoechst Marion Roussel, Inc.*, 314 F.3d 1313, 1327 (Fed. Cir. 2003). The Court sees no ambiguity in the claim term, and therefore, nothing to be gained by further defining it. The full claim language reads, "the multiprocessor system setting a clock frequency, of at least a part of the multiprocessor system to a minimum in accordance with a number of pending operations of a first processor." (D.I. No. 90-23 at 15, claim 1) Intel contends that the claim "provides no context for determining what constitutes 'a minimum.'" (D.I. No. 90 at 72.) But a closer reading of the claim language proves otherwise: the inventors intended to set a clock frequency "to a minimum **in accordance with a number of pending operations of a first processor**." In other words, the clock frequency is set at the minimum amount required to carry out the tasks of the first processor—whatever those tasks might be.

Intel suggests that Pact limited this term in prosecuting the claim. But the prosecution history does not show a clear disavowal of the claim's scope. On the contrary, Pact explained the use of "minimum" in the claim by referring to the specification, which "discloses that one or more cells may have a clock frequency set to a minimum, to **for instance**, preserve the contents of a memory." (D.I. 90-

22 at 14.) The Court reads Pact's statement as providing but one example of a "pending operation" according to which a minimum clock frequency would be set, not as a limitation or disavowal. Intel seeks to transform this limitation into an absolute minimum. But the claim language indicates that the minimum frequency is relative to the number of operations of a first processor, not just the preservation of memory contents.

G. '301 Patent Term—"Data processing element" and/or "data processing elements adapted for programmably processing sequences" (Claims 3, 6, 8-10, 12-14, 16-18, 23-26, 30, 32, 35)

PACT Plain and ordinary meaning; no construction necessary.
INTEL reconfigurable and sequential data processors where the data results from one processor are fed to another, for each processor to perform a separate computation
COURT Plain and ordinary meaning; no construction necessary.

The '301 Patent is a parent of the '047 and '065 Patents. Because they are part of the same family, Intel argues that Pact's disclaimer during prosecution of the '047 Patent concerning the term "data processing unit . . . adapted for sequentially processing data" applies here. Intel's argument fails for two reasons. *First*, the claim language at issue is not the same. The Court has no reason to conclude that Pact's disclaimer concerning "sequentially processing data" applies to a disclosure about "programmably processing sequences." Indeed, nothing in the prosecution history equates those two phrases. *Second*, Pact's disclaimer came after the '301 Patent issued. A patentee is held to what he claims in his patent and what he declares during its prosecution. *See Springs Window*

Fashions LP v. Novo Indus., L.P., 323 F.3d 989, 995 (Fed. Cir. 2003). That is, the scope of the patent is fixed at the time that the patent issues. The patentee cannot narrow the scope of his patent retroactively, even in the prosecution of a related patent. This predictability ensures that the public is put on notice and offers the patentee some degree of assurance in his right to exclude.

Finally, Intel again seeks to define the data processors as "reconfigurable." The Court again declines to do so, for the same reason.

III. CONCLUSION

The Court will construe the disputed claims as described above, and it will adopt the parties' agreed-upon constructions. An appropriate Order follows.

BY THE COURT:

/s/ Joshua D. Wolson
JOSHUA D. WOLSON, J.

September 30, 2020