UNITED STATES DISTRICT COURT
DISTRICT OF MASSACHUSETTS

ACQIS, LLC,	*	
	*	
Plaintiff,	*	
	*	
v.	*	Civil Action No. 14-cv-13560
	*	
EMC CORPORATION,	*	
	*	
Defendant.	*	

MEMORANDUM AND ORDER ON CLAIM CONSTRUCTION

BURROUGHS, D.J.

Plaintiff ACQIS, LLC ("ACQIS") alleges that certain computer storage products of Defendant EMC Corporation ("EMC") infringe 22 claims of the following eleven patents owned by ACQIS: U.S. Patent Nos. 7,363,416 (the "'416 Patent"), 7,676,624 (the "'624 Patent"), 7,818,487 (the "'487 Patent"), 8,041,873 (the "'873 Patent"), RE41,294 (the "'294 Patent"), RE42,814 (the "'814 Patent"), RE43,171 (the "'171 Patent"), RE44,468 (the "'468 Patent"), RE42,984 (the "'984 Patent"), RE43,119 (the "'119 Patent"), and RE41,961 (the "'961 Patent") (collectively, the "patents-in-suit"). [ECF No. 307 at ¶¶ 7−18]. The EMC products at issue are modular computer systems, and the patents-in-suit each describe and claim one or more computer modules that can be removed from one console and placed in another console. [ECF No. 102 at 1]. The console (*e.g.*, keyboard, mouse, display, and disk drive) is a platform into which a module containing the core computing hardware (*e.g.*, central processing unit ("CPU"), memory, input/output, and hard drive) can be inserted in order to form a complete personal computer. [ECF No. 71 at 2].

The parties filed claim construction briefs concerning three disputed terms, and the Court conducted a hearing on July 27 and July 28, 2017 at which the parties presented their proposed

constructions. [ECF Nos. 350, 352]. For the following reasons, the Court construes the terms as set forth below.

I. BACKGROUND

On September 9, 2013, ACQIS filed its initial complaint against EMC in the United States District Court for the Eastern District of Texas. [No. 13–00639, ECF No. 1]. On December 6, 2013, EMC moved to transfer the action to the District of Massachusetts pursuant to 28 U.S.C. § 1404(a). [No. 13–00639, ECF No. 21]. On April 30, 2014, before ruling on the motion to transfer, the court consolidated the action against EMC with three related lawsuits brought by ACQIS against other defendants in the Eastern District of Texas. [No. 13–00639, ECF No. 38]. On September 10, 2014, Judge Leonard Davis conditionally granted EMC's motion to transfer the action to the District of Massachusetts, retaining jurisdiction over EMC through the claim construction process and noting that the transfer would become effective upon the issuance of his claim construction opinion. [ECF No. 44]. On February 12, 2015, Judge Davis held a Markman hearing concerning the disputed claim terms. [ECF No. 76 at 1]. On April 13, 2015, he issued a claim construction opinion and an order transferring the case against EMC to this Court. [ECF Nos. 71, 72].

On April 27, 2015, EMC filed a motion to stay the case pending Inter Partes Review ("IPR") of two of the patents-in-suit. [ECF No. 80]. IPR is an expedited procedure for challenging the validity of a patent before the United States Patent and Trademark Office ("PTO") and its Patent Trial and Appeal Board ("PTAB"). [ECF No. 102 at 4]; see 35 U.S.C. §§ 311−319. The IPRs involved 3 of the 22 claims asserted in the litigation: Claim 61 of the '873 Patent and Claims 24 and 31 of the '814 Patent. On June 10, 2015, the Court stayed the case in its entirety until a decision issued in the IPRs. [ECF No. 102]. On March 8, 2016, the PTAB

issued final written decisions finding that EMC had not proven that the challenged claims were unpatentable. [ECF No. 140]. On August 10, 2016, this Court lifted the stay. Id. On February 22, 2017, the parties filed a Joint Claim Construction Statement identifying each party's interpretation of the following disputed terms: (1) "Peripheral Component Interconnect (PCI) bus transaction"; (2) "Encoded . . . serial bit stream of Peripheral Component Interconnect (PCI) bus transaction and related terms"; and (3) "communicating . . . PCI bus transaction." [ECF No. 192]. A Markman hearing was then held on July 27 and July 28, 2017. [ECF Nos. 350, 352].

II. LEGAL STANDARD

Claim construction is the first stage of a patent infringement analysis, where "the scope and meaning of the patent claims asserted are determined" as a matter of law by the court. Clearstream Wastewater Sys., Inc. v. Hydro-Action, Inc., 206 F.3d 1440, 1444 (Fed. Cir. 2000); see Markman v. Westview Instruments, Inc., 517 U.S. 370, 372 (1996) (holding that "construction of a patent, including terms of art within its claim, is exclusively within the province of the court"). Although Judge Davis has issued a claim construction opinion in this matter, which is entitled to "reasoned deference," Iovate Health Sciences, Inc. v. Allmax Nutrition, Inc., 639 F. Supp. 2d 115, 124 (D. Mass. 2009) (citation omitted),[1] the Court may "engage in a rolling claim construction, in which the court revisits and alters its interpretation of the claim terms as its understanding of the technology evolves." Pressure Prods. Med. Supplies, Inc. v. Greatbatch Ltd., 599 F.3d 1308, 1316 (Fed. Cir. 2010) (quoting Pfizer, Inc. v. Teva

[1] See Visto Corp. v. Sproqit Techs., Inc., 445 F. Supp. 2d 1104, 1108−09 (N.D. Cal. 2006) (quoting Innovations, LP v. Intel Corp., No. 04−450, 2006 WL 1751779 at *4 (E.D. Tex. June 21, 2006)) ("The Court concludes that [a claim construction order from outside the instant jurisdiction] is entitled to 'reasoned deference,' with such deference turning on the persuasiveness of the order; 'in the end, [however, the Court] will render its own independent claim construction.'").

Pharm., USA, Inc., 429 F.3d 1364, 1377 (Fed. Cir. 2005)); see Pfizer, Inc., 429 F.3d at 1377 ("[A] conclusion of law such as claim construction is subject to change upon the development of the record. . . .").

In claim construction, a court generally must give claim terms their ordinary and accustomed meaning as understood by one of ordinary skill in the art in question at the time of the invention and in the context of the entire patent. See Phillips v. AWH Corp., 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc). "[W]here the ordinary meaning of claim language as understood by a person of skill in the art is not readily apparent," courts generally consider a "hierarchy of sources to aid in claim construction." Skyline Software Sys., Inc. v. Keyhole, Inc., 421 F. Supp. 2d 371, 375 (D. Mass. 2006). First, the claim language itself is where claim construction "must begin and remain centered" because "the claims of a patent define the invention to which the patentee is entitled the right to exclude." Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc., 381 F.3d at 1111, 1115–16 (Fed. Cir. 2004). Second, the specification "is always highly relevant to the claim construction analysis" and "[u]sually . . . is dispositive." Phillips, 415 F.3d at 1315 (quoting Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576, 1582 (Fed. Cir. 1996)). In the specification, a patentee may define his own terms, give a claim term a different meaning than the term would otherwise possess, or disavow certain meanings. Id. at 1316. That being said, the Federal Circuit has "warned against importing limitations from the specification into the claims absent a clear disclaimer of claim scope." Andersen Corp. v. Fiber Composites, LLC, 474 F.3d 1361, 1373 (Fed. Cir. 2007). Third, the prosecution history can provide additional insight into how the inventor and the PTO understood the patent. See Phillips, 415 F.3d at 1317. Finally, district courts may consider extrinsic evidence, such as inventor

testimony, dictionaries, or learned treatises, but must "keep in mind the flaws inherent in each type of [extrinsic] evidence and assess that evidence accordingly." Id. at 1317, 1319.

Here, a central issue is whether and how IPRs that took place after Judge Davis's claim construction order should impact this Court's interpretation. The doctrine of prosecution disclaimer precludes patentees from recapturing, through claim construction, specific meanings disclaimed during the prosecution of a patent, including in IPR proceedings. See Aylus Networks, Inc. v. Apple Inc., 856 F.3d 1353, 1359–60 (Fed. Cir. 2017) ("Extending the prosecution disclaimer doctrine to IPR proceedings will ensure that claims are not argued one way in order to maintain their patentability and in a different way against accused infringers."). "Thus, when the patentee unequivocally and unambiguously disavows a certain meaning to obtain a patent, the doctrine of [prosecution] disclaimer narrows the meaning of the claim consistent with the scope of the claim surrendered." Id. (quoting Biogen Idec, Inc. v. GlaxoSmithKline LLC, 713 F.3d 1090, 1095 (Fed. Cir. 2013)). Prosecution disclaimer thereby "'protects the public's reliance on definitive statements made during prosecution' by 'precluding patentees from recapturing through claim interpretation specific meanings [clearly and unmistakably] disclaimed during prosecution.'" Computer Docking Station Corp. v. Dell, Inc., 519 F.3d 1366, 1374–75 (Fed. Cir. 2008) (quoting Omega Eng'g, Inc. v. Raytek Corp., 334 F.3d 1314, 1323–24 (Fed. Cir. 2003)). "[S]tatements giving rise to a disclaimer may be made in response to a rejection over the prior art, but they may also take place in other contexts." Uship Intellectual Props., LLC v. United States, 714 F.3d 1311, 1315 (Fed. Cir. 2013); see id. (Federal Circuit cases "broadly state that an applicant's statements to the PTO characterizing its invention may give rise to prosecution disclaimer"). Prosecution disclaimer may "occur through amendment or argument," Aylus, 856 F.3d at 1359, and is binding even if the PTAB does not

adopt the amendment or argument. See Springs Window Fashions LP v. Novo Indus., LP, 323 F.3d 989, 995 (Fed. Cir. 2003).

The standard for prosecution disclaimer is "exacting." Poly-America, LP v. API Indust., Inc., 839 F.3d 1131, 1136 (Fed. Cir. 2016). In order to overcome the "heavy presumption" that "claim terms carry their full ordinary and customary meaning," Plantronics, Inc. v. Aliph, Inc., 724 F.3d 1343, 1350 (Fed. Cir. 2013) (citation omitted), the "alleged disavowing actions or statements made during prosecution" must be both "clear and unmistakable." Aylus, 856 F.3d at 1359 (quoting Omega Eng'g, Inc., 334 F.3d at 1323). "If the challenged statements are ambiguous or amenable to multiple reasonable interpretations, prosecution disclaimer is not established." Tech. Props. Ltd. LLC v. Huawei Techs. Co., Ltd., 849 F.3d 1349, 1358 (Fed. Cir. 2017).

III. DISCUSSION

A. "Peripheral Component Interconnect (PCI) bus transaction"

ACQIS's Proposed Construction	EMC's Proposed Construction	Judge Davis's Construction [ECF No. 71]
"information, in accordance with the PCI Standard, for communicating with an interconnected peripheral component" In the alternative, "a transaction, in accordance with the PCI Standard, for communicating with an interconnected peripheral component"	"a transaction, as defined by the industry standard PCI Local Bus Specification, involving a PCI bus"	"information, in accordance with the PCI standard, for communication with an interconnected peripheral component"

Judge Davis construed "Peripheral Component Interconnect (PCI) bus transaction" ("PCI bus transaction") as "information, in accordance with the PCI standard, for communication with

an interconnected peripheral component." [ECF No. 71 at 10]. During this Court's Markman hearing, the parties agreed on the use of the word "transaction" and they had already agreed to include the relevant industry standard, the PCI Local Bus Specification. [ECF No. 350 at 27:9−28:20; ECF No. 189 at 19].

The central dispute remaining is whether the term requires the presence of a PCI bus. Before Judge Davis, EMC interpreted PCI bus transaction as "signals communicated over a PCI bus," but ultimately "failed to show that a PCI bus 'transaction' necessarily implies the presence of a PCI 'bus.'" [ECF No. 71 at 8]. Using Claim 24 of the '171 Patent as an example, Judge Davis showed that the claim language described "an integrated interface controller and bridge unit to output an encoded serial bit stream of address and data bits of [a] Peripheral Component Interconnect (PCI) bus transaction, the integrated interface controller and bridge unit coupled to the central processing unit without any intervening PCI bus." Id. at 9 (emphasis added). Accordingly, he concluded that a PCI bus transaction "can be encoded and conveyed serially without the existence of an originating PCI bus." Id. at 10.

EMC argues that its current proposal does not contradict Judge Davis's opinion, because its proposed construction only requires that a PCI bus is involved, not that it be an "originating" or "intervening" PCI bus. According to EMC, the plain meaning of PCI bus transaction should naturally involve a "PCI bus" and a "transaction," and every embodiment described in the patents-in-suit includes at least one PCI bus. EMC further asserts that ACQIS's statements during the IPR proceedings disclaimed any construction that does not require a PCI bus.

ACQIS responds that Judge Davis already rejected EMC's similar prior proposal and that ACQIS did not in any way disclaim the scope of its claims. Like Judge Davis, ACQIS relies on the claims that specifically exclude the presence of a CPU side intervening bus to contradict

EMC's reading. In ACQIS's view, the presence of a PCI bus in the peripheral system of the console (as opposed to the computing system) is irrelevant and outside of the claim scope.

The Court agrees with Judge Davis's interpretation, even taking into account EMC's broader proposal. For example, Claim 24 of the '171 Patent recites in relevant part:

> 24. A method comprising:
> providing a computer module, the module comprising
> a central processing unit,
> a connection program,
> an integrated interface controller and bridge unit to output an encoded serial bit stream of address and data bits of [a] Peripheral Component Interconnect (PCI) bus transaction, the integrated interface controller and bridge unit coupled to the central processing unit without any intervening PCI bus, and
> a low voltage differential signal channel coupled to the integrated interface controller and bridge unit to convey the encoded serial bit stream of PCI bus transaction; . . . .

'171 Patent at col. 20:3-16. Although this claim describes a method without a CPU side intervening PCI bus, EMC attempts to read the presence of a PCI bus on the peripheral side into the claim. The Court acknowledges that the specifications disclose embodiments that have PCI busses at some location in the console. However, with respect to claims that expressly exclude an intervening bus, the claim language does not suggest that the presence of a PCI bus outside of the computing system has any relevance. Claim 24, for example, describes a module involving an integrated interface controller and bridge unit coupled to the "central processing unit." The presence or absence of a PCI bus wholly disconnected from the central processing unit falls outside of the plain meaning of the claim. Moreover, the parties agree that "PCI bus transaction" incorporates the industry standard PCI Local Bus Specification. As Judge Davis noted, "a PCI bus transaction must include all information required by the PCI standard," but the PCI Local Bus Specification does not define such transactions by the presence of a PCI bus. See [ECF No.

189-8 at § 3.3]. Accordingly, the claim language and specification do not require that a PCI bus transaction involve a PCI bus.

Turning to the prosecution history, EMC submits that, during the IPRs, ACQIS disclaimed its position that a PCI bus transaction does not require a PCI bus. ACQIS stated in its patent owner's response that the relevant prior art references did not "generate PCI bus transactions or PCI transactions at the CPU side" because the CPU side contained "no PCI bus" or "removed the PCI bus." [ECF No. 185-8 at 10]. At the IPR hearing, ACQIS further stated that with respect to a particular prior art reference, "[y]ou don't have to have the PCI bus." [ECF No. 185-16 at 21]. However, ACQIS later clarified its position that the presence of a PCI bus is only "one indicator" of a PCI transaction but it is "not determinative" because "[y]ou could generate a PCI transaction without a bus." Id. at 21−22.

Taken as a whole, the statements above do not constitute "clear and unmistakable" disclaimer of the meaning of PCI bus transaction. ACQIS did not repeatedly assert that a PCI bus is required for a PCI bus transaction. See Aylus, 856 F.3d at 1362−63 (finding prosecution disclaimer where patent owner repeated and reiterated statements to distinguish prior art). Instead, ACQIS described a feature of the prior art—the lack of a PCI bus—but did not expressly distinguish the claimed invention based on the presence or absence of a PCI bus. See Computer Docking Station Corp., 519 F.3d at 1375 ("Prosecution disclaimer does not apply, for example, if the applicant simply describes features of the prior art and does not distinguish the claimed invention based on those features."). EMC's interpretation of ACQIS's position taken during the IPRs is also plainly belied by ACQIS's statement that a PCI bus transaction may be generated without a bus. See Tech. Props. Ltd. LLC, 849 F.3d at 1358 (prosecution disclaimer is not established if the challenged statements are ambiguous).

Considering "the importance of uniformity in the treatment of a given patent," Markman, 517 U.S. at 390, the Court "would be remiss to overlook another district court's construction of the same claim terms in the same patent." Finisar Corp. v. DirecTV Grp., Inc., 523 F.3d 1323, 1329 (Fed. Cir. 2008). Accordingly, given Judge Davis's construction and the discussion above, the Court construes "Peripheral Component Interconnect (PCI) bus transaction" to mean "**a transaction, in accordance with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component**."

B. "Encoded . . . serial bit stream of Peripheral Component Interconnect (PCI) bus transaction and related terms"

ACQIS's Proposed Construction	EMC's Proposed Construction	Judge Davis's Construction [ECF No. 71]
"code representing a PCI bus transaction"	"a PCI bus transaction that has been serialized from its original parallel format"	"code representing a PCI bus transaction"

When Judge Davis construed "encoded PCI bus transaction" as "code representing a PCI bus transaction," he rejected EMC's proposal that the term require converting information from parallel form to serial form, because the intrinsic evidence did not suggest that "encoding" was tethered to a parallel-to-serial conversion, nor had ACQIS stated in the reexamination proceedings that parallel-to-serial conversion was "always necessary." [ECF No. 71 at 11]. Before this Court, EMC argues that because a "PCI bus transaction" is generated in parallel form, a PCI bus transaction that has been "serialized" or encoded in a "serial bit stream" necessarily must have been converted from parallel to serial. [ECF No. 185 at 24–25]. EMC also points out that "every single disclosed embodiment [of the patents-in-suit] depicts a serialization of originally parallel bus transaction data." Id. at 25. Finally, EMC asserts that ACQIS clearly and unmistakably argued in the IPRs that its claims require parallel-to-serial conversion.

ACQIS objects to the parallel-to-serial limitation and recommends that the Court follow Judge Davis's construction, because the claims do not focus on the original form of the PCI bus transaction, only on the serial form of the transaction output. ACQIS suggests that because several of the claims describe communicating encoded PCI bus transactions "without an intervening PCI bus," parallel-to-serial conversion must not be required. [ECF No. 189 at 23]. ACQIS also disputes that it took the position during the IPRs that "encoding" requires parallel-to-serial conversion. Id. at 24−26.

Given that Judge Davis has already construed this term based on the information available at the time of his opinion, the Court begins with the question of whether ACQIS disclaimed the scope of its patents during the IPRs.[2] In both of its patent owner's responses filed in the IPRs, ACQIS stated that "one key to the invention was to serialize the otherwise parallel PCI bus transactions to increase communication speeds for peripherals." [ECF No. 185-7 at 11; ECF No. 185-8 at 8]. In comparing prior art references to ACQIS's patents, ACQIS claimed that "these references never used a serialized PCI bus transaction, only parallel." [ECF No. 185-8 at 9]. According to ACQIS, its inventions boost the speed of communication between the CPU and peripheral devices "by making the PCI communication serial rather than parallel." [ECF No. 185-7 at 15; ECF No. 185-8 at 13]; see [ECF No. 185-8 at 18] ("This serial form of a PCI bus transaction increases speed over parallel forms of a PCI bus transaction").

[2] If ACQIS's statements in the IPRs constitute prosecution disclaimer as to the patents at issue in those proceedings, the disclaimer may also apply to related patents containing the same or similar terms. See Trading Techs. Int'l, Inc. v. Open E Cry, LLC, 728 F.3d 1309, 1323 (Fed. Cir. 2013) ("In general, the prosecution history regarding a particular limitation in one patent is presumed to inform the later use of that same limitation in related patents, unless otherwise compelled" (citation and quotation omitted)); Omega Eng'g, Inc. v. Raytek Corp., 334 F.3d 1314, 1334 (Fed. Cir. 2003) (where patentee disclaimed claim scope in prosecution of one patent, court will "presume, unless otherwise compelled, that the same claim term in the same patent or related patents carries the same construed meaning").

ACQIS's patent owner's responses also explained that PCI bus transactions "must comply with a particular format for peripheral devices and their PCI drivers to understand," and that the "PCI standard specified 32-bit parallel communications." [ECF Nos. 185-7 at 17−19; 185-8 at 15−17]. ACQIS summarized the '873 Patent and the '814 Patent as a "solution to the problem caused by the PCI standard's use of parallel communications." [ECF Nos. 185-7 at 20; 185-8 at 18]. Because the claims use "encoded" in the context of communicating or transmitting a PCI bus transaction in serial form, ACQIS's patent owner's responses strongly suggest that the claims require serializing an otherwise parallel transaction.

ACQIS reiterated the importance of parallel-to-serial conversion throughout the IPR hearing. In distinguishing the claimed invention from prior art, ACQIS stated, "The whole point [of ACQIS's invention] is you start PCI . . . whether it's the CPU or the printer. You start with the PCI address that's in the parallel slow form, serialize it and then take it back to the PCI form at the end." [ECF No. 189-21 at 32−33]. While the prior art references do not have a "physical address that's then scrambled and then put back together down here," ACQIS explained that its patents have a "PCI address . . . spelled out here, [a] 32-bit word, and I take it, I put it on my serial line. So that's the whole point. I'm going from parallel, I'm putting on a serial line." Id. at 31−32. Further, ACQIS maintained that "the whole point of this invention and these claims is that they are centered around dealing with a standard. All of the computers out there have PCI. And so the point was, how do you speed up PCI? And the point is you take it from parallel to serial and then back to parallel." Id. at 35. When asked by one of the PTAB judges, "Your patents also changed the bus too, right? You said a parallel bus doesn't work so we are going to change it to a serial bus. So it's also not a standard PCI bus," ACQIS described its patent as an "hourglass:" "You have got a standard PCI bus, you have got the invention, depending on how

you do it, but you have got the new bus in the center, and what that's doing is taking the parallel 32 bits coming down, putting them on a serial bus, moving them and then taking them back out." Id. at 40−41. In comparison, with respect to one of the prior art references, ACQIS argued that "[t]here's no standard [PCI bus transaction] on the front end that drives a standard transaction on the back end," whereas ACQIS's patents have a "standard [PCI bus transaction] on the front end, standard [PCI bus transaction] on the back end and a serial link in between." Id. at 44.

This same theme continued during the discussion of Figure 8 of the '873 Patent, which ACQIS argues controverts EMC's construction. With respect to Figure 8 and the relevant claim, ACQIS said, "But the point here is—actually, this point is there's no intervening PCI bus. But when you look at this and when you read it, there is a PCI transaction here that is ["scrabbleized"][3] and then put on the serial link and then recreated back here." Id. at 45−46. Further, "If you are going to comply with the PCI standard, which I believe Figure 8 is a PCI limited embodiment, I would have to confirm that, you need to take the PCI transaction on the front end, serialize it and do the PCI transaction on the back end. That's the embodiment." Id. at 46. In addressing Figure 8 specifically, ACQIS stated:

> So on Figure 8 of the '873 [P]atent, you have to look at the text. It's talking about a PCI transaction. And so the claims don't require a bus. They require a PCI transaction to take place. You are looking at the standard the whole time. I'm putting a transaction together that looks like a PCI transaction. So all of my PCI-compliant drivers know how to read it. So I have created my PCI transaction. That's why it matters, my drivers can read it. And then I'm taking it at a parallel form, putting it into serial form and then back to parallel.

[3] During the hearing, ACQIS described a PCI bus transaction by referring to Scrabble cubes: "[EMC's] expert describes it . . . as Scrabble cubes. I've got a PCI address, I have got it spelled out here, 32-bit word, and I take it, I put it on my serial line. So that's the whole point. I'm going from parallel, I'm putting on a serial line. And on the bottom end I have got to be able to reassemble my word." [ECF No. 189-21 at 31−32].

Id. at 47. ACQIS then emphasized, "So you are starting with your PCI transaction and converting it" and "the point is if you are trying to match [Figure 8] to the claims, you are taking a PCI transaction and serializing it. That's what you are starting with." Id. at 48.

The PTAB judge specifically inquired whether the term "encoded serial bit stream of peripheral component interconnect PCI bus transaction," as used in a '873 Patent claim, should be construed such that the "encoded serial bit stream must have originated from a PCI to begin with." Id. at 51. ACQIS replied that despite not knowing what the judge meant by "originate," "what the claim requires is that it is a PCI bus transaction. That is defined by the standard. You know the three portions: Address, data, and control. And you have to take that, whatever that would be in a parallel form and you are going to encode it, encode a serial bit stream. So I'm taking the transaction data, I don't think it matters where it originates from, then I'm going to take it, I'm going to serialize it and then send it out over my serial bus for speed purposes." Id. at 51. After the judge clarified that he intended no special meaning with respect to "originate," ACQIS confirmed that its construction "is the hourglass." Id. at 52. During the rebuttal testimony, ACQIS again said, "Remember I said the hourglass, you start with the PCI, you got the parallel bits, serialize them, get them to the other side, push them back out." Id. at 66.

ACQIS's numerous and repetitive statements in the IPRs clearly and unmistakably show that an encoded PCI bus transaction requires that a PCI bus transaction be encoded for serial transmission from a parallel form. Similar to Aylus, ACQIS repeatedly represented that "the whole point" of the invention is to convert a PCI bus transaction from parallel to serial and back to parallel. See Aylus, 856 F.3d at 1362 (relying in part on patentee's statement that "'this is a key aspect of the claimed invention" in finding prosecution disclaimer). ACQIS's argument was not only clear and unmistakable but also consistent throughout its briefing and oral argument.

Each of the statements identified above reinforced ACQIS's chosen metaphor of the hourglass, which, if nothing else, represents a PCI bus transaction beginning in parallel, converting to serial, and then back to parallel.

The claim language and specification are also consistent with an interpretation requiring parallel-to-serial conversion. The disputed term essentially contains the following elements: (1) encoded, (2) serialized or "serial bit stream," and (3) PCI bus transaction. ACQIS focuses solely on the meaning of "encoded," but the Court must interpret the term as a whole and in context with surrounding words. See ACTV, Inc. v. Walt Disney Co., 346 F.3d 1082, 1088 (Fed. Cir. 2003) ("While certain terms may be at the center of the claim construction debate, the context of the surrounding words of the claim also must be considered in determining the ordinary and customary meaning of those terms."). As discussed above, the meaning of PCI bus transaction relates directly to the industry standard PCI Local Bus Specification. The Court agrees with ACQIS that a PCI bus transaction does not require the presence of a PCI bus, but it cannot ignore that the PCI Local Bus Specification was developed for communication over a PCI bus, which is indisputably parallel. See [ECF No. 189-4 at 36] ("The PCI standard bus was a 32-bit wide parallel bus with multiplexed address and data bits and separate command and timing control lines."). ACQIS itself described the PCI Local Bus Specification as applying to "32-bit parallel communications." [ECF Nos. 185-7 at 17−19; 185-8 at 15−17]. ACQIS also pointed out in the IPRs that the '873 Patent specification accurately incorporated the PCI Local Bus Specification by describing the required address, data, and control bits as "multiplexed parallel address/data (A/D) bits and control bits . . . ." [ECF No. 185-5 at 16−17]; '873 Patent at col. 17:41-43. The claim language and specification, when read in context with the industry standard, support the construction that a PCI bus transaction is in a parallel form prior to being serialized.

ACQIS primarily relies on Figure 8 of the '873 Patent—an embodiment that involves a host interface controller and bridge connected to a peripheral interface controller and bridge without any intervening PCI bus—to show that parallel-to-serial conversion is not required. However, a detailed diagram of one embodiment of the host interface controller shows that it has a "parallel to serial converter" and "[e]ncoders" that "format the PCI address/data bits to a form more suitable for parallel to serial conversion. . . . ." '873 Patent at fig. 10, col. 16:55-58. The specification further suggests that ACQIS's invention involves "turning signals into bits," which is a type of encoding that ACQIS acknowledges involves parallel-to-serial conversion. [ECF No. 189 at 17]; see '873 Patent at col. 5:31-39 ("The present invention overcomes the aforementioned disadvantages of prior art by interfacing two PCI or PCI-like buses using a non-PCI or non-PCI-like channel. In the present invention, PCI control signals are encoded into control bits and the control bits, rather than the control signals that they represent, are transmitted on the interface channel."); see also '814 Patent at col. 13:17-21 ("The preferred [attached computer module to peripheral console] interconnection includes circuitry to transmit and receive parallel bus information from multiple signal paths as a serial bit stream on a single signal path.").[4]

Therefore, in consideration of the claim language, the specification, and the prosecution disclaimer, the Court construes "Encoded . . . serial bit stream of Peripheral Component

[4] ACQIS also argued that "grouping bits into specified size blocks of bits" is a type of encoding that does not require parallel-to-serial conversion. [ECF No. 185-7 at 28]; [ECF No. 189 at 23]. ACQIS's citation to the '873 Patent specification, however, indicates that this type of encoding may also involve parallel-to-serial conversion. See '873 Patent at col. 17:54−60 ("The multiplexed parallel A/D bits and some control bits input to [a] transmitter . . . are serialized by parallel to serial converters . . . into 10 bit packets. These bit packets are then output on data lines . . . of the XPBus. Other control bits are serialized by [a] parallel to serial converter . . . into 10 bit packets. . . .").

Interconnect (PCI) bus transaction and related terms" as "**a PCI bus transaction that has been serialized from a parallel form**."

C. **"Communicating . . . PCI bus transaction"**

ACQIS's Proposed Construction	EMC's Proposed Construction	Judge Davis's Construction [ECF No. 71]
"communicating," "communicate," "transmitting," "transmit," "convey," and "output," are terms that are easily understood by a lay person and need no construction	"communicating a PCI bus transaction, including all address, data, and control bits, without discarding any of those bits"	Judge Davis did not construe this term.

At this Court's Markman hearing, the parties agreed to the following construction of "Communicating . . . PCI bus transaction:" "communicating a PCI bus transaction, including all address, data, and control bits." [ECF No. 352 at 227–228, 230]. Courts are only obligated to construe terms when the parties present a dispute. See U.S. Surgical Corp. v. Ethicon, Inc., 103 F.3d 1554, 1568 (Fed. Cir. 1997) ("Claim construction is a matter of resolution of disputed meanings and technical scope, to clarify and when necessary to explain what the patentee covered by the claims, for use in the determination of infringement. It is not an obligatory exercise in redundancy."); Vivid Techs., Inc. v. Am. Science & Eng'g, Inc., 200 F.3d 795, 803 (Fed. Cir. 1999) ("only those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy"); see also Amgen, Inc. v. F. Hoffmann-La Roche Ltd., 494 F.Supp.2d 54, 70 n.1 (D. Mass. 2007) ("Where the parties agree upon claim construction, that construction properly governs the course of subsequent proceedings just as would a stipulation of fact."). Because this construction is also supported by the intrinsic evidence, the Court adopts the parties' agreed-upon construction of "communicating . . . PCI bus

transaction" as "**communicating a PCI bus transaction, including all address, data, and control bits.**"

IV. CONCLUSION

For the foregoing reasons, the Court interprets the disputed terms in the manner set forth above.

SO ORDERED.

Dated: December 8, 2017

/s/ Allison D. Burroughs
ALLISON D. BURROUGHS
U.S. DISTRICT COURT JUDGE