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UNITED STATES DISTRICT COURT

DISTRICT OF MINNESOTA

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Chandramouli Vaidyanathan,	)	Civil 09-1212 (DWF/JSM)
individually,	)	
	)	
Plaintiff,	)	CIVIL JURY TRIAL
	)	VOLUME VI
-v-	)	
	)	
Seagate US LLC, a Delaware	)	
limited liability company;	)	
and Seagate Technology, LLC,	)	
a Delaware limited liability	)	
company,	)	8:00 o'clock, a.m.
	)	November 17, 2010
Defendants.	)	St. Paul, Minnesota

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BEFORE THE HONORABLE JUDGE DONOVAN W. FRANK  
 UNITED STATES DISTRICT COURT JUDGE  
 CIVIL JURY TRIAL PROCEEDINGS  
 VOLUME VI

\* \* \*

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1 MR. BRENT SNYDER: Just one witness, Your  
2 Honor, the Plaintiff calls Roger Rolbiecki.

3 THE COURT: Sir, if you want to step to the  
4 front of the courtroom? The witness stand is over here.  
5 Once I get you close to the front, I will administer the  
6 oath. If you would please raise your right hand?

7 (Witness sworn.)

8 Then there is a step up there, sir. If you  
9 want to have a seat behind the microphone and then once  
10 you move up to the microphone, if you would please state  
11 your full name and spell your last name?

12 THE WITNESS: Roger Rolbiecki,  
13 R-o-l-b-i-e-c-k-i.

14 THE COURT: You may inquire whenever you are  
15 ready, Counsel.

16 ROGER ROLBIECKI,  
17 DIRECT EXAMINATION

18 BY MR. BRENT SNYDER:

19 Q. Good afternoon. Thank you for being with us  
20 this afternoon, Mr. Rolbiecki. I understand that you  
21 are here pursuant to subpoena, is that correct?

22 A. That is correct.

23 Q. Please give us a -- please tell us your  
24 educational background.

25 A. I have undergraduate degrees in math and

1 physics, and a Master's Degree in Physics.

2 Q. From what University?

3 A. From Winona State University and Ohio  
4 University in Athens, Ohio, on the Master's.

5 Q. What year was your Master's Degree?

6 A. In 1978.

7 Q. Can you give me a brief overview of your  
8 professional experience since 1978?

9 A. I have been employed in the semiconductor  
10 industry since 1978 and I have worked primarily in the  
11 semiconductor industry performing device analysis, yield  
12 enhancement, physical design, design support, software  
13 support, design tools.

14 Q. Which organizations have you worked for?

15 A. I have worked for yield enhancement at DTC,  
16 Semiconductor, Fairchild Semiconductor, Cypress  
17 Semiconductor, AMI Semiconductor. I have also worked at  
18 Control Data as a consultant, at Sperry Univac as a  
19 yield enhancement engineer, SLE as a design engineer,  
20 CAD engineer, worked at Seagate as a design engineer,  
21 and also in Guidant as a physical design engineer in the  
22 medical industry.

23 Q. When -- well, I should ask this. What is  
24 your current vocation?

25 A. I am currently self-employed, working under

1 my own LLC company, Go Semis. And I am performing  
2 engineering support to the industry.

3 Q. And what is your hourly rate?

4 A. It is at \$115 an hour.

5 Q. And I believe the Plaintiff is compensating  
6 you for your time away from your business?

7 A. Yes, that is correct.

8 Q. Tell me when you began working for Seagate?

9 A. I began April, the end of April of 2007.

10 Q. What position were you hired to at that time?

11 A. I was hired to do PDK development that is  
12 Process Design Kit development to support the design of  
13 magnetic memories.

14 Q. Were you ever a member of the ATG crew?

15 A. Yes, I was.

16 Q. When did you become a member of that group?

17 A. Well, ATG was the group that we were hired  
18 into. It was both design and process.

19 Q. And that was 2007?

20 A. 2007, April of 2007.

21 Q. Do you know the Plaintiff in this case, Dr.  
22 Vaidyanathan?

23 A. Yes, I do.

24 Q. How do you know him?

25 A. Through work at Seagate.

1 Q. Do you remember when you first met him?

2 A. Roughly the end of 2007, you know.

3 Q. Was it after he was already an employee at  
4 Seagate?

5 A. Yes.

6 Q. Were you involved in his hiring at all?

7 A. No, I had no involvement at all.

8 Q. Or his recruitment? Did you have any  
9 involvement in his recruitment and or hiring?

10 A. No, I had no knowledge of the hiring process,  
11 recruitment or hiring process.

12 Q. Did you know him at all while he was employed  
13 with Texas Instruments?

14 A. No, I did not.

15 Q. Did you understand he was a yield engineer at  
16 Texas Instruments?

17 A. Yes, I did.

18 Q. What was your understanding that he was hired  
19 to do at Seagate?

20 A. I understood that he was a yield enhancement  
21 engineer.

22 Q. Did Seagate employ any other yield  
23 enhancement engineers within that ATG group?

24 A. Not to my knowledge.

25 Q. Please describe for me the interaction you

1 had with him while you were both employed within the  
2 ATG?

3 A. Well, we were all primarily working on the  
4 future generation of the memory bit cell, and the design  
5 rules. So, the entire organization was involved in  
6 revising the process or revising the design rules,  
7 revising the next generation memory cell.

8 Q. Working on a product, if you will?

9 A. Working on test chips, and also potentially a  
10 higher density in memory array.

11 Q. What was the status of those test chips  
12 during this 2008 time period?

13 A. They were fluid. They were in constant  
14 revision. They were being designed and enhanced along  
15 the way as more knowledge became available to us, and  
16 also as new semiconductor processing became available to  
17 us.

18 Q. Was there a baseline in place?

19 A. There was not a baseline.

20 Q. Was there a repeatable process?

21 A. There was not a repeatable process.

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Q. Your experience as a yield enhancement engineer at prior organizations, how many years did you spend performing those duties for organizations?

A. I would say easily six.

Q. Can you give me an idea of what those duties were that you performed in that function?

A. Well, at Cypress Semiconductor, they were a memory house. They produced SRAMs, which is different from an MRAM. We performed parateo analysis, bitmapping, trend charting, process flow, you know, statistical process flow of data versus, you know, in-line data, final test data versus in-line test data.

At Fairchild Semiconductor, it was a large



1 logic house. You know, our duties there were based on a  
2 statistical analysis of a process that is running, it  
3 was based on a process they had and established yield.  
4 The duties were to sustain existing yields, and also  
5 through enhanced yields, by again using statistics.

6 Q. At those organizations, tell me about the  
7 status of the product that you were working on?

8 A. Well, there was always in existence to do  
9 yield enhancement, there was always an existing baseline  
10 to characterize your process from. It was then possible  
11 to enhance the yield.

12 It was a division between, you know, a mature  
13 process that you could do enhancement on, versus a  
14 process that was under development.

15 Q. I am going to put exhibit, Plaintiff's  
16 Exhibit 6 back up here. And Plaintiff's Exhibit 6 has  
17 the title, yield engineer position.

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Did you perform any of these functions in your previous roles as a yield engineer?

A. Yes, I have.

Q. Which ones?

A. Bitmap analysis, run correlations between in-line fab data and electrical data to identify signals for product yield improvements, correlate wafer bin fallout, layer defect in-line and be able to perform statistical analysis, work with the failure analysis groups to determine the root cause of the failures.

The candidate must be able to engage in tool vendors for testing. I did not do that. There was a specific group that would normally service the testing functions.

Candidate must have a strong cross-functional understanding of device and process, that is true.

Q. Did you perform any of these functions while you were employed in the ATG group?

A. No, I didn't.

Q. You weren't a yield engineer there, were you?

A. No, I was not.

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Q. Please describe for me your interaction with Dr. Vaidyanathan, whether monthly, weekly, daily, if you can describe that for us, please.

A. Well, certainly. It was, you know, multiple times a week. It was not necessarily daily, but we were all closely tied together in developing next generation process and next generation, you know, memory and test chip. So, we would interface quite regularly between the design groups and the process groups. It was on a one-to-one basis, it was on a group basis. We only held, you know, we had strong communication meetings that, you know, there was a technical exchange on a

1 regular basis that people were invited to discuss what  
2 they are working on for information exchange and also to  
3 educate, you know, former co-workers.

4 Q. Did you have an opportunity to observe Dr.  
5 Vaidyanathan at work?

6 A. Yes.

7 Q. When you were observing him at work, did you  
8 see him performing any of these functions as stated? I  
9 will take them one by one.

10 First one, bitmap analysis to generate yield  
11 parateo, et cetera. Did you see him perform those  
12 functions?

13 A. No, I did not see him perform that.

14 Q. How about number two?

15 A. I did not see him perform that.

16 Q. How about number two?

17 A. I did not see him perform that, either.

18 Q. Three?

19 A. I did not see number three.

20 Q. How about four?

21 A. No, I did not see four.

22 Q. How about the others?

23 A. I did not see the engagement with tool  
24 vendors. I believe that the candidate has a strong  
25 cross-functional understanding of process and device. I

1 believe that was indeed true.

2 Q. True for you, as well, probably?

3 A. Yes, and many of the others --

4 Q. And for most of the other members on the  
5 team.

6 A. Um, the candidate must be able to lead  
7 cross-functional teams, I believe that was true; and  
8 coordinate, certainly coordinate activities with design  
9 process product and reliability engineering, was true.

10 Q. I want to focus on these top four for the  
11 next couple of questions. Are these duties consistent  
12 with your understanding of a yield enhancement engineer?

13 A. Yes, they would be.

14 Q. Did you see anybody at Seagate performing  
15 these functions?

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A. It would be possible to do this for an experimental basis, but to statistically do yield enhancement by using bitmap analysis and trying to correlate in-line data to electrical data, if there is not any baseline yield, is a task that cannot be done.

Q. Are you employed at Seagate any longer?

A. No, I am not.

Q. When did you, when did your employment with Seagate in the ATG end?

A. My employment ended May 13th of 2009.

Q. Was that a part of a reduction in force?

A. Yes. The entire organization was reduced.

Q. I want to talk to you about the status of the ATG in 2007. This would have been your first year, I believe. That you were employed within the ATG.

A. That is correct.

Q. And I think you said April is when you started?

A. The end of April, yes.

Q. Now, what did -- what did you hear during

1 that time at meetings and the like about the status of  
2 the ATG? Where was it?

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8 A. It was my understanding that  
9 Seagate had some aggressive goals, that we were all  
10 involved with development of initial memory cell to  
11 improve the technology. And we also were exercising the  
12 design functions, we were exercising the process  
13 functions, you know, we had aggressive goals to release  
14 a chip as soon as possible to evaluate the memory of the  
15 bit cell.

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Q. What did you hear about  
the future of the organization?

A. You know, initially, there was a very  
aggressive posture and it seemed to have total support

1 of Seagate behind our activities. We produced a test  
2 chip, and after the test chip was processed and came out  
3 of fab, there seemed to be a slight change in the  
4 direction. And the initial bit size of the device that  
5 came out was large. And that meant that the device was  
6 not suitable for our production device. You have to  
7 have a certain density in a memory array to be  
8 competitive with other technologies.

9           So, there was some constraints in the bit  
10 cell design that limited the usefulness of the device  
11 for production. And the fact that it did not yield when  
12 it came out, it constrained the ability to characterize  
13 the process.

14           Q.       What did Seagate want to do about this?

15           A.       Well, I think that it was the realization  
16 that more aggressive semiconductor technology had to be  
17 obtained that, you know, it could be obtained either  
18 through partnership, through merging, through the sale  
19 of the ATG.

20           You know, I think that the hopes of the  
21 organization, you know, were to continue with the  
22 memory, the magnetic memory. I believe it was certainly  
23 my feeling and many others that the solid state memory  
24 was the direction that Seagate needed to pursue.

25           And at some point, you know, when the bit



1 cell was too large and the yields were not there, you  
2 know, it was my understanding that another strategy had  
3 to be obtained, besides having Seagate solely funded,  
4 you know, the solid state memory had to be produced in  
5 volume. If it was a competitive technology with Seagate  
6 having \$13 billion in revenue, they produced quite a few  
7 disk drives. So, you would have to have a pretty major  
8 effort into the development of a magnetic, you know,  
9 memory.

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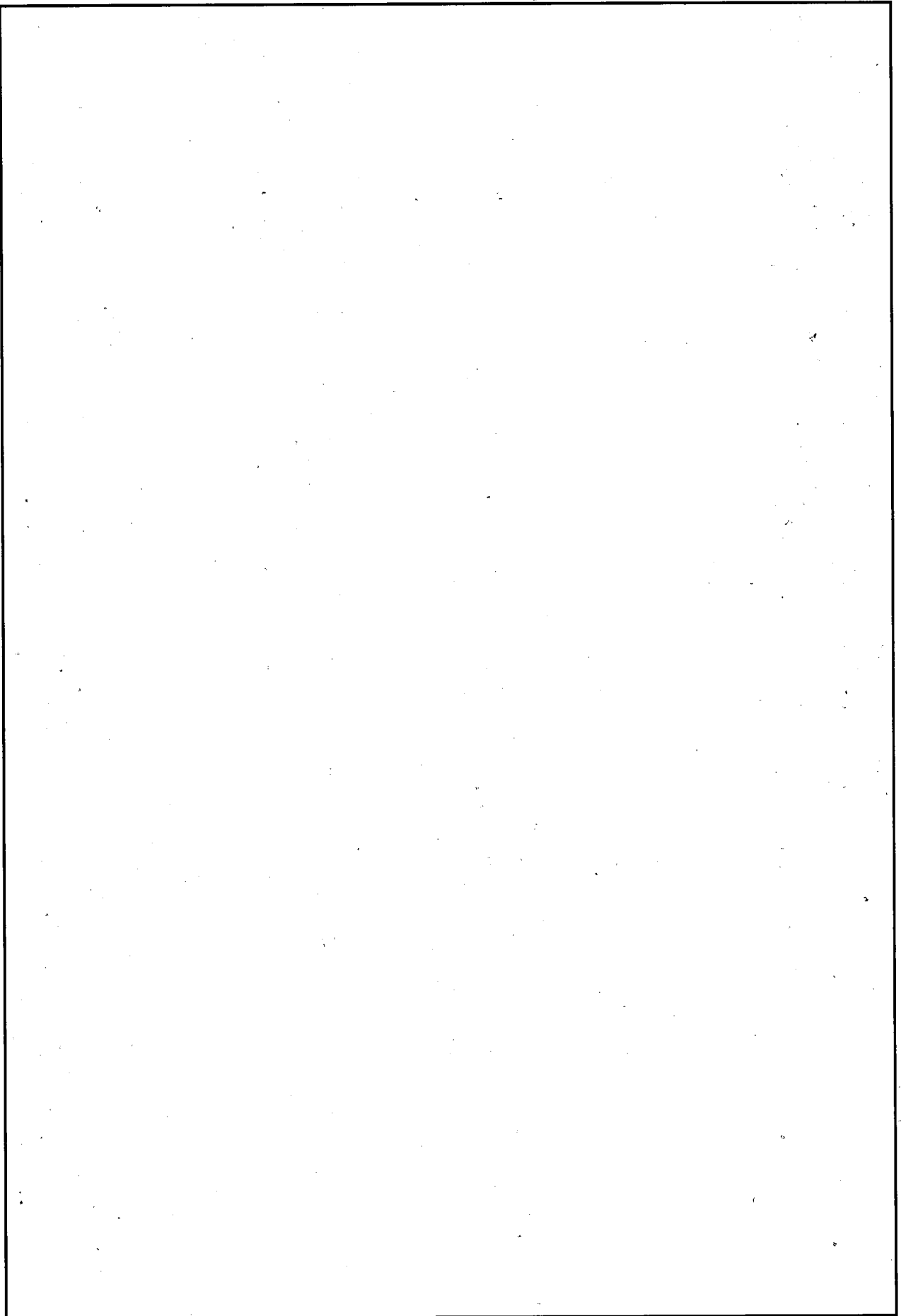
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2           A.                   It was my perception that the  
3 process portion of ATG continued to grow at higher rate  
4 than the design. And it was my belief that this would  
5 be consistent with establishing the appearance of having  
6 a credible semiconductor facility. And a credible  
7 semiconductor facility would have a baseline yield,  
8 would have a baseline process, would have an  
9 organization that supported that function. And if the  
10 company would be sold, it would be beneficial to have an  
11 all inclusive function as a stand-alone semiconductor  
12 house, even though we didn't have all of the process  
13 tools that we needed.

14                   It would make it -- the emphasis was in  
15 structure of ATG, the emphasis was on developing  
16 intellectual properties which, you know, gave us value  
17 as a stand-alone company, just the memory portion of it.  
18 Those are my perceptions of the things that had changed.

19                   MR. BRENT SNYDER: I don't have anymore  
20 questions at this time.

21                   THE COURT: You may inquire if you wish.

22                                   CROSS EXAMINATION

23 BY MS. ROBBINS:

24           Q.           Hi, Mr. Rolbiecki. How are you this  
25 afternoon?

1 A. Fine.

2 Q. Good. I have a few questions for you. First  
3 of all, did you work with good people at the ATG?

4 A. Yes, of course.

5 Q. Smart people, capable people?

6 A. Yes, very capable.

7 Q. And really across the board there were 100  
8 some people at one point smart, capable people; correct?

9 A. Yes, very capable.

10 Q. A lot of people with Ph.D.'s?

11 A. Yes.

12 Q. A lot of people with deep backgrounds like  
13 your many years of experience?

14 A. Yes.

15 Q. And would you agree that it was an  
16 interesting, challenging project?

17 A. Yes, it was.

18 Q. Did you go there to the ATG because you found  
19 it to be an interesting project?

20 A. No.

21 Q. That didn't -- it didn't interest you when  
22 you moved there?

23 A. You know, I had another interesting project  
24 there I was working on.

25 Q. And you testified about having some years of

1 experience. And did you -- when did you work in the  
2 yield area?

3 A. You know, 1980 through 1992, roughly.

4 Q. I thought you had testified that you worked  
5 about 6 years in yield engineering.

6 A. I did. You know, not all of those years were  
7 exclusively yield engineering, yield enhancement, so I  
8 tried to segregate it to exactly when I was performing  
9 those duties.

10 Q. I understand. So, you worked in yield  
11 engineering on and off between 1980 and 1992?

12 A. Yes. You know, it was a shared  
13 responsibility that sometimes it was exclusively yield  
14 enhancement, and sometimes I would migrate into  
15 different duties.

16 Q. Okay. So, you would go into different areas,  
17 but you could still come back to doing yield engineering  
18 at another time?

19 A. It wasn't that, you know, fluid. You did  
20 yield enhancement and then you left and you did a  
21 different job.

22 Q. Okay, and then you came back and did more  
23 yield enhancement?

24 A. Not in all cases, no. Sometimes it was a  
25 permanent switch. And in the later years it was kind of

1 a permanent switch.

2 Q. So, sometimes it was consistent, sometimes it  
3 was on and off?

4 A. Right.

5 Q. All right. And we have heard some testimony  
6 that yield engineering changes very rapidly, is that  
7 true?

8 A. Can you elaborate on the question a little  
9 bit more about the change, what changes.

10 Q. Did the skills you need for yield engineering  
11 change very quickly?

12 A. Well, I wouldn't say so, you know, there is a  
13 core set of skills, you know, being able to understand a  
14 process. And if you certainly change the process, you  
15 change your skills and learn a new understanding, you  
16 know, but the techniques employed, parateo analysis,  
17 trend charting, statistical analysis, those are all  
18 pretty standard in the industry.

19 Q. So, is it your testimony that if you are in  
20 yield engineering at one time, you could get back into  
21 it at a later date without much trouble?

22 A. Well, no, the -- you know, going back into  
23 yield engineering requires the understanding of the  
24 process. It understands, you know, obviously somebody  
25 would have to hire you. And you know, that is one thing

1 that I offer as far as consulting, but I have not had  
2 anybody that took me up on yield enhancements.

3 Q. So, you do yield consulting, even though you  
4 haven't actually worked in that field since 1992?

5 A. It is something I put on my resume, you know,  
6 as a skill set. You know, whether I can do that, I have  
7 not been able to do that again. You know,  
8 traditionally, what the industry looks at, you know, is  
9 your last job. I would have a much higher probability  
10 getting into the design, you know, PDK development that  
11 I was doing at Seagate, rather than going back on an old  
12 skill set.

13 Q. Given that you have it on your resume, do you  
14 think you would be capable of continuing to do some  
15 yield engineering?

16 A. I think, certainly, everybody is retrainable.  
17 You can relearn skills. What I have observed in the  
18 industry is that the long-term vision of companies is no  
19 longer there. You know, people don't want to retrain  
20 you. They don't want to invest in an employee over the  
21 long-term, they want somebody that can come in, perform  
22 a certain function, which is why I am trying the  
23 consulting fee, because you go in and you have an  
24 opportunity to work a month, or two months or three  
25 months, and then you are done.

1 Q. Okay. But, during that period in 1980  
2 through 1992, you did yield engineering on that  
3 on-and-off basis as we discussed, right?

4 A. Yes.

5 Q. You are here today as a paid witness, is that  
6 correct?

7 A. That is correct.

8 Q. And your rate, did you say -- what did you  
9 say your rate was?

10 A. It was \$115 an hour.

11 Q. And so did you charge also for time that you  
12 worked with Plaintiff's -- with Dr. Vaidyanathan's  
13 lawyers?

14 A. Yes.

15 Q. How much time have you charged Dr.  
16 Vaidyanathan for this case?

17 A. It would be four hours.

18 Q. And with respect to Dr. Vaidyanathan, is he  
19 someone that you were friendly with when you worked at  
20 Seagate?

21 A. Yes, I hope I was friendly with everyone.

22 Q. Have you remained in touch with him since he  
23 left Seagate?

24 A. No, unfortunately not.

25 Q. You mentioned that when you were working at



1 Seagate, all of the people who were working in the ATG  
2 were, I think the phrase you used was closely tied? And  
3 I am getting the sense that that is closely tied within  
4 the work that they did, is that right?

5 A. Yes.

6 Q. That whole group of the ATG, right?

7 A. Yes.

8 Q. And that would include Christina Hutchinson?

9 A. Yes. Not as closely, you know, because her  
10 functions and mine didn't overlap; but, certainly, you  
11 know, we all had regular meetings together.

12 Q. Would that include Andrew Habermas?

13 A. Yes. Oh, Andrew, yes, for sure.

14 Q. Would that include Sriram Viswanathan?

15 A. No.

16 Q. He was in the ATG, right?

17 A. I don't remember the name.

18 Q. You don't remember -- okay. That is fair  
19 enough. One of the things you mentioned was the word,  
20 the baseline. What do you mean by baseline?

21 A. Baseline is the validation of a process. And  
22 that is through a yield. And when you have -- you have  
23 to have some product that you run to characterize your  
24 fab. And when you run the product, it establishes a  
25 baseline. A baseline is a given yield, it helps you

1 characterize, you know, the defect density of the fab,  
2 it gives you kind of a signature of this state of how  
3 your fab is running. And from a baseline, you can infer  
4 what a different style product will do.

5 Say if you have a memory device, typically  
6 they run a small memory device, establish a baseline  
7 yield, you know, do bitmapping of that device to  
8 establish a defect density. You can infer, then, you  
9 know, what will happen on a larger chip or potentially  
10 on a different type of chip. It could be a logic chip  
11 versus a memory chip.

12 Q. And you had two test chips by the fall of  
13 2007 in the ATG, correct?

14 A. Yes.

15 Q. With respect to yield development, which is  
16 the way you described some of your past experience, is  
17 the idea of yield development to move to higher yield?

18 A. Yes.

19 Q. You want the yield to get better, right?

20 A. Yes, that is true.

21 Q. So, if there is no yield, you want to get to  
22 1 percent yield. If there is 90 percent yield, you want  
23 to get to 95 percent yield?

24 A. That is not a baseline enhancement, it's a --

25 Q. That is not the question I asked.

1 A. Oh, I'm sorry.

2 Q. I just asked you if you want to get -- from  
3 0, you want to get to 1. If you get to 95, you want to  
4 get to 100?

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12 You testified that the yields weren't there.  
13 So there was something called a yield, correct?

14 A. 0 yield.

15 Q. So, you are saying there was absolutely no  
16 yield of what?

17 A. There was never a die that functioned at 100  
18 percent.

19 Q. Were there bits working on a chip?

20 A. I am sure there were, yes.

21 Q. And were there bits working on some chips at  
22 high yield?

23 A. You know, I am sure the yield varied, you  
24 know. I would not say high yield.

25 Q. Okay. But, you weren't a yield engineer at

1 Seagate, right?

2 A. No.

3 Q. So that wasn't your job to find that out,  
4 right?

5 A. No, it was not.

6 Q. And you didn't do failure analysis, correct?

7 A. No, I did not.

8 Q. You weren't in the test group?

9 A. I was not.

10 Q. To whom did you report?

11 A. I reported into Harry Liu.

12 Q. So, not to Antoine Khoueir, right?

13 A. No, I did not.

14 Q. So, you were in a different reporting  
15 structure than Dr. Vaidyanathan, correct?

16 A. That is correct.

17 Q. And then you would all report up to Brian  
18 Lee, or not?

19 A. No, Harry Liu was parallel to Brian Lee.

20 Q. So, Dr. Vaidyanathan reported to Antoine  
21 Khoueir, right?

22 A. Yes, that is right.

23 Q. And Mr. Khoueir reported to Brian Lee,  
24 correct?

25 A. That is correct.

1 Q. And Mr. Lee reported to Mr. Ryan, correct?

2 A. That is correct.

3 Q. And so you reported to Mr. Liu, correct?

4 A. Harry Liu.

5 Q. Harry Liu. And Harry Liu reported also to  
6 Mr. Ryan, is that --

7 A. Initially, that is true, but if my memory is  
8 correct, at some point Harry Liu reported in to Brian  
9 Lee. It didn't really matter, because that was another  
10 level beyond.

11 Q. Was there some fluidity in terms of people  
12 were working in different groups with one another?

13 A. Everybody was working together.

14 Q. Okay. You looked at that list of job duties  
15 with the bullet points on it, and you testified that the  
16 last four bullet points, you saw Dr. Vaidyanathan do all  
17 of those things, correct?

18 A. Yes, that is correct.

19 Q. Would it also be correct that you did not  
20 observe everything he did?

21 A. That is true, yes.

22 Q. You weren't his boss?

23 A. No, I was not.

24 Q. And you didn't follow him around?

25 A. No, I did not.

1 Q. You had other things to do, right?

2 A. Yes, that is correct.

3 Q. And you never interviewed Dr. Vaidyanathan,  
4 correct?

5 A. I did not interview him.

6 Q. You did not sit in on any interviews with  
7 him?

8 A. No, did not.

9 Q. You never talked to him during the recruiting  
10 process, right?

11 A. I did not.

12 Q. You never knew what was said to him during  
13 that process?

14 A. That is correct.

15 Q. And was your employment terminated by  
16 Seagate?

17 A. Yes, it was.

18 Q. When did that happen?

19 A. It was May 13th of 2009.

20 MS. ROBBINS: I have no further questions.  
21 Thank you Mr. Rolbiecki.

22 THE COURT: Redirect if you wish?

23 REDIRECT EXAMINATION

24 BY MR. BRENT SNYDER:

25 Q. Just one quick follow-up. Mr. Rolbiecki, I

1 think you mentioned a moment ago there was never a  
2 functional die in the ATG group?

3 A. Yes that is true.

4 Q. Tell me why that is significant in terms of  
5 yield enhancement engineering?

6 A. That establishes your baseline. In order to  
7 do bitmap analysis and characterize your fab, that you  
8 need a functional die enabled to establish a defect  
9 density. You need some working device, you know, that  
10 works 100 percent to do yield enhancement.

11 MR. BRENT SNYDER: Okay. No more questions.

12 MS. ROBBINS: Nothing further, Your Honor.

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