UNITED STATES DISTRICT COURT
DISTRICT OF NEW MEXICO

STC.UNM,

Plaintiff,

v.

INTEL CORPORATION

Defendant.

Civil No. 1:10-cv-01077-RB-WDS

STC'S INITIAL CLAIM CONSTRUCTION BRIEF

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I. Introduction

A patent must provide (1) a written description of the invention, and (2) a set of claims that define the subject matter of the invention. Much like a written contract, the meaning and scope of a patent are determined by the courts as a matter of law. Thus, when a court construes the claims of the patent, it defines the federal legal rights created by the patent document. Where the parties disagree about the meaning of any language in the patent claims, the court construes the language as a matter of law. STC and Intel have identified 7 claim terms for construction by the Court.

The main difference between the parties' proposed claim constructions are readily apparent. In accordance with well established patent law, STC's constructions are consistent with the teachings of the patent, and the plain and ordinary meaning of the claim language.

On the other hand, Intel's constructions are detached from the patent. For certain terms, Intel's proposed constructions are overly broad with the apparent purpose of attacking the validity of the patent. For other terms, Intel's constructions are overly narrow, clearly in an attempt to avoid infringement of its own processes.

In this brief, STC provides the support for its proposed constructions, and some preliminary comments on Intel's constructions to highlight the incorrect interpretations that Intel is urging the Court to adopt. STC will provide a more detailed analysis of Intel's constructions in its responsive brief.

II. The Technology at Issue

The technology at issue involves advancements in lithography, which is an integral part of the semiconductor manufacturing process. Lithography advancements have been a driving force that allows for the fabrication of ever smaller components, *e.g.*, transistors, on semiconductor chips. The smaller the transistors, the more there are that can be packed on a chip, and the more powerful the chip. Today's semiconductors are made with minimum feature sizes of 32nm (22nm coming soon). For comparison, a human hair is about 60,000nm in diameter. Exh. 2 [Mack Dec.], ¶2.

While the beginning-to-end manufacturing process of a semiconductor chip is immensely complicated, STC highlights here some of the basic lithographic operations that are most relevant to this case.

A. Semiconductor Wafers

Semiconductor chips are made on silicon wafers. One wafer can contain over 300 billion transistors, and hundreds of chips are cut from a finished wafer.[1] A semiconductor wafer is comprised of many layers. At the most basic level, the transistors are made first in semiconductive material, then the metal and insulating layers (the wiring interconnecting features and circuit elements) are made on top of the transistors. *Id. at* ¶3. Below is a cross-section depiction of exemplary device layers in a semiconductor wafer (right). The top layers represent the interconnecting features and circuit elements, while the underlying layers represent the transistor level.

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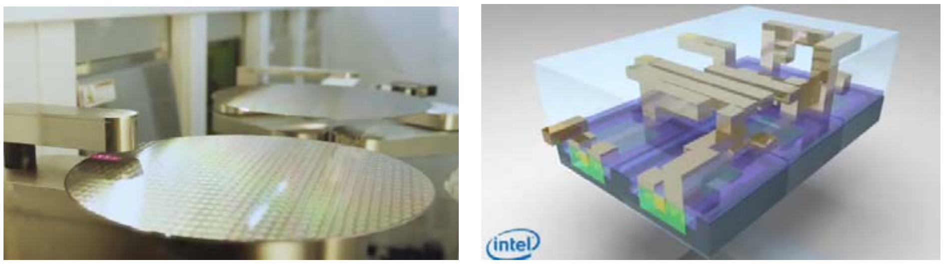
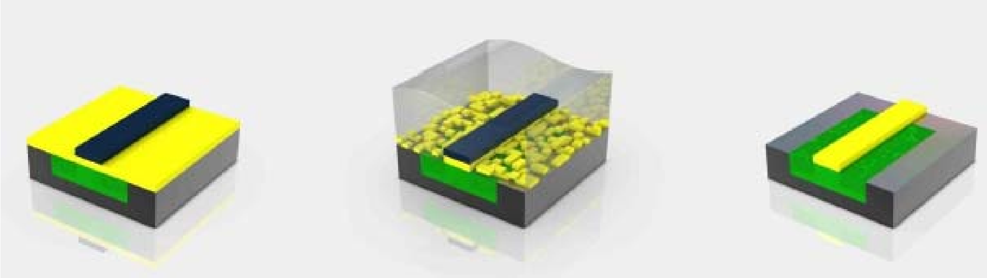
[1] The images shown in this section of the brief come from the following Intel sources: *Factory Tour - 32nm Manufacturing Technique*, *www.youtube.com/watch?v= SeGqCl3YAaQ*; *From Sand to Silicon: the Making of a Chip*, *www.youtube.com/watch?v=Q5paWn7bFg4.*



A WAFER (LEFT), AND A SMALL PORTION OF A CHIP SHOWING TRANSISTORS INTERCONNECTED WITH METAL WIRING (RIGHT)

B. A Basic Lithography Sequence

Lithography is used to pattern the various layers. First, a layer of photoresist is “spun” onto the wafer. Photoresist material is sensitive to light and allows for the transfer of an image through what is basically a photographic exposure process. Next, laser light is used to expose a pattern on the photoresist. After the photoresist is exposed, portions of it become soluble and are washed away in developer. The pattern in the photoresist is then transferred by etching into the underlying layer. *Id. at* ¶4. The following sequence shows a patterned line of black photoresist (first figure) that is used to protect the underlying yellow layer during an etch process (second figure). The yellow portions not under the black is etched away, then the resist is stripped away leaving the yellow pattern (third figure).



PATTERNED PHOTORESIST, ETCHING, AND RESULTING PATTERN

The above sequence of images is simplified, showing only part of one of the 300 billion transistors that are made on each wafer. The subsequent layers that are made on top of the transistors, *e.g.*, metal interconnect wires, etc., are also made using these same basic operations.

III. The '998 Patent

STC's U.S. Patent No. 6,042,998 (the '998 patent) covers advanced lithography techniques that make very small patterns for use in semiconductor manufacturing. The inventions claimed in the '998 patent were conceived by University of New Mexico faculty members in the 1990s. The chief inventor, Dr. Steven Brueck, is a Distinguished Professor of Electrical and Computer Engineering. Since 1986, Dr. Brueck has been the head of the University's Center for High Technology Materials. Dr. Brueck is a Fellow of the IEEE, the Optical Society of America, and the American Association for the Advancement of Science.

The '998 patent is a continuation-in-part of an earlier patent that is also owned by STC, U.S. Patent No. 5,705,321 (the '321 patent).[2] The '321 patent also names Dr. Brueck as an inventor, and is incorporated by reference in its entirety into the '998 patent. While the '998 patent is in a highly technical field, the claimed inventions can be understood with an appreciation of some of key concepts, which are discussed below.

A. Limitations of Lithography Equipment

Due to basic scientific principles that govern the physics of light, the lithography equipment that is used in current manufacturing processes has limitations. Those limitations prevent the manufacture of features smaller than about 37nm in dimension. In simple terms, the physics of

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[2] A continuation-in-part is an application filed during the lifetime of an earlier patent application, repeating some substantial portion or all of the earlier patent application and adding matter not disclosed in the earlier patent application. *See* Manual of Patent Examining Procedure § 201.08 (8th ed., Rev. 8, 2010).

light do not provide for sufficient resolution to make sub 37nm patterns on the wafer in the basic lithography sequence described above, using lithography manufacturing equipment available today. The invention disclosed in the ‘998 patent provides for a lithographic technique known as “double patterning” that allows for the extension to smaller feature dimensions and improved pattern quality. In this way, it is possible to fit a greater number of features on a wafer. Exh. 2 [Mack Dec], at ¶5.

B. Double Patterning Lithography

Double patterning is the execution of two lithography sequences – expose, develop, etch – in the <u>same</u> device layer. The particular type of double patterning claimed by the ‘998 patent requires the use of two photoresist layers with an intermediate development process. *See* Exh. A [‘998 Patent], claim 6. Moreover, it requires that the two patterns that are formed in the respective lithography sequences be combined in a specific manner that results in the creation of features that cannot be achieved in one lithography sequence. *Id; 9:29-30.*[3] The resultant patterns will have sharp corners (12:56-63; 13:29-31), smaller features (2:29; 20:10-13), and/or higher pattern density than is possible with one lithography sequence (16:7-8). These unique characteristics are explained further in the following section.

C. Two Embodiments

The ‘998 patent covers two basic embodiments of double patterning. The first embodiment is now commonly referred to as “line trimming,” or “line cutting.” In this embodiment, a first pattern is created in a first lithography sequence, which may be a pattern of lines and spaces. A second pattern is created at a right angle to the first. When those two patterns are combined, the

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[3] References to the ‘998 Patent are to the column and line numbers of the specification. For example, 9:29 is a reference to column 9, line 29. The ‘998 Patent is attached hereto as Exhibit A. Annotations have been provided in the margins of Exhibit A to show support for STC’s claim constructions.

result is a pattern with features that have sharp corners, as shown in the “top-down” images of Figure 6B of the patent, reproduced below.

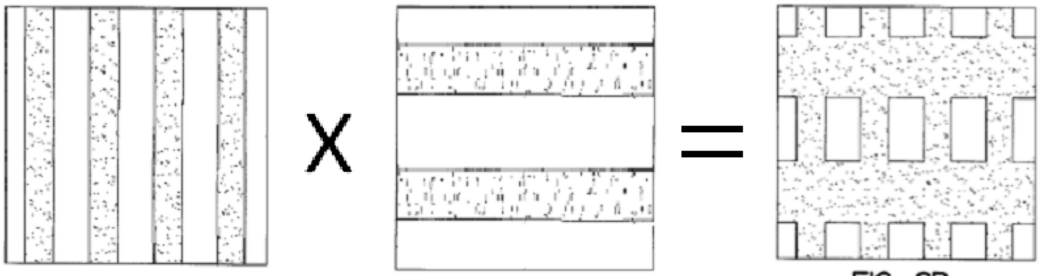


FIG. 6B

Due to the resolution limitation discussed above, prior lithography methods simply could not achieve patterns with sharp corners on such small features in one lithography sequence. Instead, the resultant pattern from one lithography sequence typically suffers from rounded corners, which are undesirable from a manufacturing perspective. *See* Figure 6A (reproduced below).

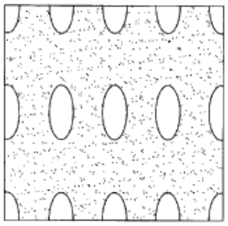


FIG. 6A

Sharp corners allow manufacturers to pack the transistors closer together, which translates to more powerful chips, and larger profit margins. Exh. 1 [‘998 Patent], at 20:10-14.

The second embodiment of double patterning lithography covered by the ‘998 patent, now commonly referred to as “inter-digitation,” or “pitch division” (*See e.g.,* Figs. 9 and 10), is not a subject of the infringement charge.

D. Frequency Space

The inventors of the ‘998 patent described and claimed their invention in the very precise scientific terms of frequency space. Much in the same way that sound can be described as being made up of frequency waves, the coordinates of two- and three- dimensional spatial objects can be described mathematically in frequency space. All physical objects, including the ultra small transistors, can be described mathematically in frequency space. Those incredibly tiny features have spatial frequencies that correspond to their geometrical shape and distance from one another. Exh. 2 [Mack Dec.], at ¶6.

An important concept regarding spatial frequencies is that increased spatial frequency corresponds to higher resolution. Exh A. [‘998 Patent], at 2:16-18. This means that the high resolution sharp corners obtained in Fig. 6B, above, result in increased spatial frequencies in comparison to rounded corners of Fig 6A: “In contrast to the prior art methods which typically yield rounded comers on the structures as shown in FIG. 6A, the present invention suitably yields the patterns shown in FIG. 6B, namely rectangles with sharp, well-defined corners.” (12:56-59). The ‘998 patent provides the mathematical equations for the spatial frequency calculations in columns 12, 13 and 16. The claim terms “spatial frequencies,” and “high spatial frequencies” are disputed claim terms, and are discussed in more detail in Section V below.

E. Hardmask

Another important concept that is discussed in the ‘998 patent is the use of a “hard mask.” The ‘998 patent also refers to this term by other commonly used descriptors within the industry: “mask material” (10:1; 16:7), “sacrificial layer” (14:1), and “suitable thin-film layer” (12:15-22). The ‘998 patent discloses the use of a hard mask for two distinct purposes.

First, a hard mask is used to protect the underlying layer that is being patterned during etching (which is the conventional way to use a hard mask). Second, and crucial to the invention, the hard mask is used to store the pattern from the first lithography sequence for use in combination with the second pattern (12:15-22; 13:14-31). This is depicted in the cross sections below. The green hardmask layer 44 is used in Figure 9D to hold the first pattern, while the second pattern 46 is formed above. Figure 9E shows the combination of both patterns in hardmask 44.

FIG. 9C

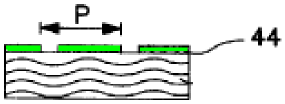


FIG. 9D

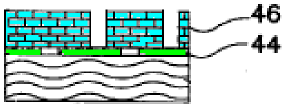
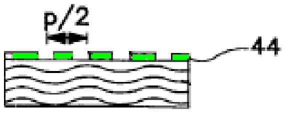


FIG. 9E



The claim terms “mask material” and “combined mask” are disputed claim terms, and are discussed in more detail in Section V below.

IV. The Law on Claim Construction

All appeals of patent cases go to the Federal Circuit Court of Appeals ("Federal Circuit"). The Federal Circuit has issued several seminal opinions concerning claim construction, the most recent being the 2005 *en banc* decision *Phillips v. AWH Corp*., 415 F.3d 1303 (Fed. Cir. 2005).[4] Set forth below are the basic canons of claim construction. These well-settled rules of claim construction, when applied, will resolve the vast majority of the disputes regarding the construction of the identified claim terms.

A. The Claim Language – Plain and Ordinary Meaning

- ☐ “A claim construction analysis must begin and remain centered on the claim language itself.” *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc., 381 F.3d 1111,* 1116 (Fed. Cir. 2004).

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[4] Other notable cases include *Markman v. Westview Instruments, Inc*., 52 F.3d 967 (Fed. Cir. 1995) (*en banc*), *Vitronics Corp. v. Conceptronic, Inc*., 90 F.3d 1576 (Fed. Cir. 1996); and *Innova/Pure Water, Inc. v. Safari Water Filtration Systems, Inc*., 381 F.3d 1111 (Fed. Cir. 2004).

☐ The words of a claim “are generally given their ordinary and customary meaning,” which “is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, *i.e.*, as of the effective filing date of the patent application.” *Phillips*, 415 F.3d at 1312-13 (citation omitted). In fact, there is a “heavy presumption” that claim terms carry their plain and ordinary meaning. *W.E. Hall. Co. v. Atlanta Corrugating*, 370 F.3d 1343, 1350 (Fed. Cir. 2004) (citation omitted).

☐ Often, this meaning is readily apparent to those of skill in the art, and a construction of “plain meaning” or “ordinary meaning” is all that is required. *See, e.g.*, *Mentor H/S, Inc. v. Med. Device Alliance, Inc.*, 244 F.3d 1365, 1380 (Fed. Cir. 2001).

B. The Specification

☐ In addition to the claim language, the patent specification “‘is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.’” *Phillips*, 415 F.3d at 1315 (citation omitted).

☐ For example, “a claim interpretation that excludes a preferred embodiment from the scope of the claim is rarely, if ever, correct.” *MBO Labs., Inc. v. Benton, Dickinson & Co.*, 474 F.3d 1323, 1333 (Fed. Cir. 2007).

☐ The specification may also “reveal a special definition given to a claim term by the patentee,” *Phillips*, 415 F.3d at 1316, though it “cannot support a definition that is contrary to *the ordinary meaning of a claim term* unless it communicates a deliberate and clear preference for this alternative definition,” *Kumar*, 351 F.3d at 1368.

☐ Moreover, “as a general rule, claims of a patent are not limited to the preferred embodiment or to the examples listed within the patent specification.” *Glaxo Wellcome, Inc. v. Andrx Pharms., Inc.*, 344 F.3d 1226, 1233 (Fed. Cir. 2003) (citation omitted).

- ☐ A corollary rule is that it is improper to import limitations from the specification into a claim. *MBO Labs., Inc. v. Becton, Dickinson & Co.*, 474 F.3d 1323, 1333 (Fed. Cir. 2007) ("patent coverage is not necessarily limited to inventions that look like the ones in the figures. To hold otherwise would be to import limitations onto the claim from the specification, which is fraught with danger").

C. Extrinsic Evidence

- ☐ A court, in its discretion, may also consider extrinsic evidence. *Phillips*, 415 F.3d at 1319. Courts are cautioned, however, to discount any extrinsic evidence that contradicts the intrinsic evidence, as extrinsic evidence is "less reliable than the patent and its prosecution history in determining how to read claim terms." *Id*. at 1318.
- ☐ "Extrinsic evidence in the form of expert testimony can be useful to a court for a variety of purposes, such as to provide background on the technology at issue, to explain how an invention works, to ensure that the court's understanding of the technical aspects of the patent is consistent with that of a person of skill in the art, or to establish that a particular term in the patent or the prior art has a particular meaning in the pertinent field." *Id*.

V. STC's Constructions

STC has charged Intel with infringement of claim numbers 6 and 7 (reproduced below). The parties' competing constructions are set forth in the below tables followed by STC's discussion of the terms.

6. A method for obtaining a pattern wherein the Fourier transform of said pattern contains high spatial frequencies by combining nonlinear functions of intensity of at least two exposures combined with at least one nonlinear processing step intermediate between the two exposures to form three dimensional patterns comprising the steps of:

   coating a substrate with a first mask material and a first photoresist layer;

exposing said first photoresist layer with a first exposure

developing said photoresist to form a first pattern in said first photoresist layer, said first pattern containing spatial frequencies greater than those in a two dimensional optical intensity image imposed onto said photoresist layer in said first exposure as a result of a nonlinear response of said first photoresist layer;

transferring said first pattern into said first mask material, said first mask material comprising at least one of SiO_2, $Si_3 N_4$, a metal, a polysilicon and a polymer;

coating said substrate with a second photoresist;

exposing said second photoresist with a second exposure

developing said second photoresist layer to form a second pattern in said second photoresist layer, said second pattern containing spatial frequencies greater than those in a two dimensional optical intensity image imposed onto said photoresist layer in said second exposure as a result of a nonlinear response of said second photoresist layer;

transferring said first pattern and said second pattern into said substrate using a combined mask including parts of said first mask layer and said second photoresist;

removing said first mask material and said second photoresist.

7. The method of claim 6 wherein said transferring step includes at least one of etching, deposition and-lift off, and damascene.

A. *"Spatial Frequencies"*

STC: A mathematical representation of a pattern. Technically defined, spatial frequencies are the coordinates in the Fourier plane resulting from the Fourier transform of the features that have been patterned.	Intel: a measure of how often components of an image or pattern repeat in a given unit of distance Optional further explanation if the Court desires: "Technically speaking, a mathematical operation called the 'Fourier transform' represents the image or pattern as a series of waves, and 'spatial frequencies' indicate how frequently each of those waves repeats across space.

This technical term is properly construed based on a skilled person's common understanding, and further solidified by the teachings used in the '998 patent. Exh. 2 [Mack Dec], at ¶7. First, STC's construction makes clear that spatial frequencies are mathematical representations of the pattern. Support for this aspect of the construction is found throughout the specification, including the equations used to calculate the spatial frequency information through the use of Fourier transform mathematics. The equations, found in columns 12, 13 and 16, are extremely advanced. Aside from appreciating that they provide the underlying calculations representing the patterns, the equations need not be comprehended to construe this term.

> ***Mathematically***, the resulting spatial frequency transform is preferably the product of appropriate [sin($f_x a_x$)/($f_x a_x$) and [sin($f_y a_y$)/ ($f_y a_y$)] functions which yields the spatial ***Fourier transform*** of the desired ***rectangular pattern***, viz:
>
> $$T(x, y) = \tag{6}$$
>
> $$\tau[E_1(x)] \times \tau[E_2(y)] = \frac{a_x a_y}{4} \sum_{n=-\infty}^{\infty} \left[\frac{\sin\left(\frac{2\pi n a_x \sin(\theta_x)}{\lambda}\right)}{\left(\frac{2\pi n a_x \sin(\theta_x)}{\lambda}\right)} e^{i\frac{4\pi n x \sin(\theta_x)}{\lambda}} \right] \times$$
>
> $$\sum_{n'=-\infty}^{\infty} \left[\frac{\sin\left(\frac{2\pi n' a_y \sin(\theta_y)}{\lambda}\right)}{\left(\frac{2\pi n' a_y \sin(\theta_y)}{\lambda}\right)} e^{\frac{i4\pi n' y \sin(\theta_y)}{\lambda}} \right]$$

Exh. A ['998 Patent], at 12:63-13:14 (emphasis added); *see also* 16:9-27. As can be seen from the above, Fourier transform mathematics are used to calculate the spatial frequencies associated with the patterns that are made by the invention. This technical aspect of the claim term is also incorporated into STC's construction. Exh. 2 [Mack Dec], at ¶8.

Intel's proposed construction, on the other hand, is unnecessarily limiting in that it only applies to repeating patterns. One of ordinary skill in the art would appreciate that spatial frequencies can be applied to isolated, non-repeating patterns just as well as to repeating patterns. STC's construction is compatible with such non-repeating patterns, but Intel's proposed construction is not. Exh. 2 [Mack Dec], at ¶9.

B. *"A Pattern Wherein the Fourier Transform of Said Pattern Contains High Spatial Frequencies"*

STC: The final pattern resulting from the below method steps have spatial frequencies (1) that are not present in any of the individual exposures, and (2) whose magnitudes are larger than the limit of the linear optical system response, resulting in sharper corners, smaller features, or higher pattern density.	Intel: a pattern whose density in the x–y plane (the plane of the substrate) is greater than the optical system could produce

As explained in Section II (above), double patterning produces increased spatial frequency content. In the context of the '998 patent, "high spatial frequencies" has a very specific meaning, and is properly construed in the light of the teachings in the specification. Exh. 2 [Mack Dec], at ¶11. The magnitudes of "high spatial frequencies" are defined by two parameters:

> (1) frequencies found in the final pattern, but that are not present in either the first or second exposure, and
>
> (2) frequencies that are beyond the limits of the lithography equipment.

Support for these two important parameters are set forth in the Abstract, Field of the Invention, and Summary of the Invention sections of the '998 patent (Exh. 2 [Mack Dec], at ¶12):

> The present invention is related, generally, to a method and apparatus for extending the available spatial frequency content of an image, and more particularly, to a method and apparatus for combining nonlinear functions of intensity of multiple images to form three dimensional patterns with ***spatial frequencies that are not present in any of the individual exposures*** and whose ***magnitudes are larger than 2/λ, the limit of linear optical system response***, in all three spatial directions.

Exh. 1 ['998 Patent], at Field of the Invention (1:66-2:7) (emphasis added). *See also*, Abstract; and Summary of the Invention (9:25-35).

Finally, STC's construction incorporates the hallmarks of high spatial frequencies, sharper corners, smaller feature sizes, or higher pattern density. Since these physical characteristics are the ultimate goal of the double patterning process, they are an important part of the construction. Examples from the specification include (Exh. 2 [Mack Dec], at ¶13):

> The ***quality of an image*** is limited by the spatial frequencies within the image (2:10-11).
>
> * * *
>
> Thus, decreasing λ and increasing NA typically results in increased spatial frequency content and in an improved, ***higher resolution image***. (2:17-18) (emphasis added).
>
> * * *
>
> Historically, the semiconductor industry has worked to both decrease λ and increase NA in its steady progress towards ***smaller feature sizes***. (2:28-30) (emphasis added).
>
> * * *
>
> FIG. 11E shows a concept drawing of how the aforementioned frequency doubling technique might be applied to a circuit pattern, . . . changing the design to a CD grid would allow a straightforward doubling of the ***pattern density***. (18:18-26) (emphasis added).
>
> * * *
>
> FIG. 6B, namely rectangles with ***sharp, well-defined comers*** (12:59-60) (emphasis added).
>
> While the image is significantly closer to the desired pattern than the incoherent imaging results, there is still significant rounding of the corners of the printed features due to the unavailability of the ***spatial frequencies needed to provide sharp corners***. (7:26-30) (emphasis added).

STC's construction is appropriate as it provides a measure of what defines a high spatial frequency, *i.e.,* frequencies not present in any of the individual exposures, and beyond the limit of the optical system. For further understanding to the trier of fact, STC's definition describes the physical characteristics of high spatial frequencies that the inventors used to define their invention, smaller feature sizes, higher pattern density, or sharper corners.

On its face, Intel's proposed construction does not sufficiently define high spatial frequencies insofar as it attempts to limit the claim term to pattern density. In fact, Intel's proposed construction is so limiting, if applied, it would read certain embodiments out of the specification of the patent, which violates one of the basic tenants of claim construction: "a claim interpretation that excludes a preferred embodiment from the scope of the claim is rarely, if ever, correct." *MBO Labs., Inc. v. Benton, Dickinson & Co.*, 474 F.3d 1323, 1333 (Fed. Cir. 2007). As explained in Dr. Mack's declaration, Intel's proposed construction does not account for the high spatial frequencies associated with square corners. *See* Exh. 2 [Mack Dec.], at ¶¶14-19.

C. *"Combining Nonlinear Functions of Intensity of at Least Two Exposures Combined With at Least One Nonlinear Processing Step Intermediate Between the Two Exposures"*

STC**:** Combining the patterns that were formed in the two exposed photoresists, and having a non-linear process step, for example, development of the first resist, after the first exposure and before the second exposure.	Intel**:** Combining the response of two exposures of photoresist and at least one non-linear processing step (for example, development of the first photoresist) that occurs after the first exposure and before the second exposure

This claim term is properly construed based on the intrinsic evidence and a mathematical understanding of the word "function." *See* Exh. 2 [Mack Dec.], at ¶21. The claim term sets forth method steps later recited in the body of the claim. *i.e.*, a development step that occurs after the first exposure, and before the second exposure. Thus, STC's construction is consistent with the plain language of the claim.

STC's construction also specifies what is "combined." Consistent with the other language used to claim the invention, the inventors used mathematical language to describe what is being combined by the claimed method. In this regard, the patent claims "functions of intensity of at least two exposures." A mathematical function, by definition, has an output that depends on an input (the function assigns exactly one output to each input). For example, the mathematical functions sine and cosine have input variables, and outputs. Exh. 2 [Mack Dec.], at ¶22.

In the context of the "functions of intensity of at least two exposures" the claimed function is the exposure and subsequent processing (e.g., development) of photoresist. The input is the light energy that affects chemical change to the photoresist, and the output is the pattern formed in the resist. The input of the claimed exposure function, light energy, is used to affect change to the photoresist layer, which results in the output of a pattern. Exh. 2 [Mack Dec.], at ¶23.

Consistent with STC's construction, the '998 patent describes the combination of the two output patterns as the combination of two input functions (Exh. 2 [Mack Dec.], at ¶24).

> In a preferred embodiment, two (or more) exposures are individually subjected to thresholding nonlinearities, then the images are preferably combined (added or multiplied) resulting in a pattern containing additional spatial frequencies that are not substantially present in any of the individual images. Mathematically, the specific embodiment of multiplication is equivalent to:
>
> $$T(x, y) = \tau[E_1(x, y)] \times \tau[E_2(x, y)] \times \ldots \tau[E_n(x, y)] \qquad (4)$$

Exh. A ['998 Patent], at 12:22-32. An example of combining the mathematical functions with multiplication is then given.

> Mathematically, the resulting spatial frequency transform is preferably ***the product of appropriate*** $[\sin(f_x a_x)/(f_x a_x)$ and $[\sin(f_y a_y)/(f_y a_y)]$ ***functions*** which yields the spatial Fourier transform of the desired rectangular pattern, viz:
>
> $$T(x, y) = \qquad (6)$$
>
> $$\tau[E_1(x)] \times \tau[E_2(y)] = \frac{a_x a_y}{4} \sum_{n=-\infty}^{\infty} \left[\frac{\sin\left(\frac{2\pi n a_x \sin(\theta_x)}{\lambda}\right)}{\left(\frac{2\pi n a_x \sin(\theta_x)}{\lambda}\right)} e^{i\frac{4\pi n x \sin(\theta_x)}{\lambda}} \right] \times \sum_{n'=-\infty}^{\infty} \left[\frac{\sin\left(\frac{2\pi n' a_y \sin(\theta_y)}{\lambda}\right)}{\left(\frac{2\pi n' a_y \sin(\theta_y)}{\lambda}\right)} e^{\frac{i4\pi n' y \sin(\theta_y)}{\lambda}} \right]$$

Id. at 12:63-13:14 (emphasis added), *see also* 16:8-33.

STC's construction is also consistent with the Summary of the Invention section of the patent specification, which states that the two patterns are used in combination for the final pattern:

> Upon suitable development and/or processing ***the result is a layering of the two lithographic patterns in the two layers and/or in the hard mask layer. These layers in combination*** are used as masks for further processing of the underlying wafer to transfer a pattern that is the product of the two masks into the underlying materials.

Id. at 9:52-62 (emphasis added). Thus, this term is claiming the combination of the two patterns that are the result of the exposure steps.

Preliminarily, STC notes that Intel's construction falls short as it does not specify that the output of the exposure function is a pattern, which is what the entire '998 patent is about, *i.e*., the formation and combination of patterns. Exh. 2 [Mack Dec.], at ¶25.

D. *"[First/Second] Pattern in Said [First/Second] Photoresist Layer"*

STC: Shape(s) resulting from developing the photoresist	Intel: the configuration of the [first/second] photoresist layer remaining after developing

The parties' constructions for this term are similar, but STC's is more consistent with the plain and ordinary meaning of the term. Exh. 2 [Mack Dec.], at ¶27. First, the subject of the phrase that is being construed is the "pattern." Thus, the focus of the construction should be on the pattern or shapes that is being transferred to the final pattern, and not the physical embodiment of the shape in the photoresist. This is reflected in STC's use of the word "shapes" in its construction.

Second, STC's construction is consistent with the specification, as the inventors described the patterns used by the claimed method as "shapes." *See* Exh. 1 ['998 Patent], at 9:19-23; Exh. 2 [Mack Dec.], at ¶28. On the other hand, the words chosen by Intel for this term, *i.e.*, configuration, are not used in the patent specification to describe the patterns formed in the photoresist layers.

E. *"First Mask Material"*

STC: A layer of material used to preserve the first pattern for later use in the combined mask.	Intel**:** Material that is not photoresist, and that shields some or all of the underlying layer.

The '998 patent uses a hard mask in a very special and necessary way in order to manufacture a final pattern that has the physical characteristics of high spatial frequencies. Thus, this claim term is properly construed based on the plain language of the claim and intrinsic evidence. Exh. 2 [Mack Dec.], at ¶30 . STC's construction captures this necessary use of the hard mask, while Intel's overly broad construction does not.

To achieve a final pattern with sharp corners, small features, or high density, the '998 patent uses a hard mask to preserve the first pattern for use in subsequent processing steps. As called for by the plain language of the claims, after the first pattern is transferred to the hard mask, the mask is further patterned with a second lithography sequence to use *in combination* with the pattern preserved in the mask material. Exh. 2 [Mack Dec.], at ¶31. The two relevant steps from claim 6 recite:

> ***transferring said first pattern into said first mask material***, said first mask material comprising at least one of SiO_2, $Si_3 N_4$, a metal, a polysilicon and a polymer;
>
> ***transferring said first pattern and said second pattern into said substrate using a combined mask*** including parts of said first mask layer and said second photoresist;

STC's definition of this term is also consistent with embodiments taught in the '998 patent, which teach that the hard mask is used in ***subsequent*** process steps to transfer structures containing high spatial frequencies into underlying layers. Exh. 2 [Mack Dec.], at ¶32.

> "The present invention preferably employs nonlinear processes either in the photoresist intensity response and/or in additional processing steps in order to create high spatial frequencies,. . . in a pattern produced on ***a suitable thin-film layer*** [mask material] on a wafer that is used, ***in subsequent process steps***, to transfer the structures containing the high spatial frequencies . . . into the underlying film structure."

Exh. 1 ['998 Patent], at 12:15-22 (emphasis added).

The specification text associated with Figure 7 of the patent teaches that the first pattern was transferred into nitride film (13:19), and then combined with the pattern from the second layer of photoresist (13:25-26).

> FIGS. 7A-7B show an experimental realization of this pattern. . . . The pattern was developed, ***transferred into the nitride film*** [mask material], and the remaining photoresist removed. . . . FIG. 7B shows an exemplary ***resulting pattern: the vertical lines are in the nitride, the horizontal lines are in the second photoresist layer***.

Exh. 1 ['998 Patent], at 13:14-31 (emphasis added). The specification text associated with Figure 9 of the patent teaches that the first pattern is transferred into a hard mask (15:62-63), which is then used to preserve the first pattern so that it can be combined with the second pattern (16:1-9).

> With reference to FIG. 9C, any suitable etching process preferably ***transfers periodic pattern 48 (the lines) into hard mask 44***.

FIG. 9B

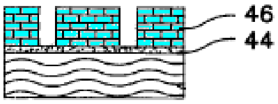
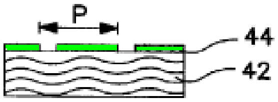


FIG. 9C



> ***With reference to FIG. 9E, any suitable etching process preferably transfers lines 50 into hard mask material 44***, thereby resulting in a pattern 48, 50 with about one half the pitch of original structure 40.

FIG. 9D

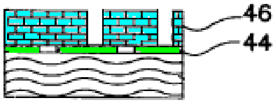
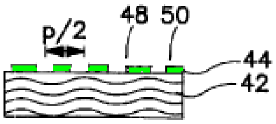


FIG. 9E



STC's definition of "mask material" captures the innovations claimed by the '998 patent that enable the manufacture of patterns with sharp corners, small features, or high density. Preliminarily, STC notes that Intel's proposed definition only defines "mask material" in the negative by merely defining what it is not. Exh. 2 [Mack Dec.], at ¶33.

F. *"Parts of Said First Mask Layer"*

STC: Some or all of the first pattern from the first mask layer.	Intel: the portions of the 'first mask material' that remain after the first 'transferring' step

"Parts of said first mask layer" is part of a larger phrase that is separately defined below. STC submits that this term cannot be properly construed in a vacuum. Thus, STC's definition of this term is consistent with the appropriate construction of the larger phrase. Exh. 2 [Mack Dec.], at ¶34. The step of the claimed method in which these terms appear is:

> transferring said ***first pattern*** and said ***second pattern*** into said substrate using a combined mask including ***parts of said first mask layer*** and said second photoresist;

Thus, this step of the claimed method is about transferring the two patterns into the substrate (which is the layer that is ultimately patterned). Exh. 2 [Mack Dec.], at ¶35. While the parties' respective constructions appear to be similar, there is an important difference. STC's construction is consistent with the above-cited plain language of the claim, *i.e.,* the part of the first mask layer that is used in the "combined mask" is itself the first pattern. *Innova*, 381 F.3d at

1116 (Fed. Cir. 2004). ("A claim construction analysis must begin and remain centered on the claim language itself.").

STC's construction is also consistent with the specification, which teaches that combined mask is a combination of two "patterns," which are combined with the mathematical operations of multiplication or addition. Exh. 2 [Mack Dec.], at ¶36.

> Together ***the two mask patterns provide a multiplication*** of the individual images . . .
>
> * * *
>
> Finally, FIG. 8C shows an exemplary result of ***multiplying the two patterns to get the final result***, thereby showing the dramatic improvement in the profiles.
>
> * * *
>
> Thus, in a preferred embodiment, the ***combined etch mask provides the multiplication operation***.

Exh. 1 ['998 Patent], at 13:26-27; 13:45-47; 14:13-15, *see also* 15:63-16:10 (mathematically combining two patterns by addition).

On the other hand, Intel's construction defines this term as the mask material that remains after the first transfer step. This construction simply misses the mark. The entire '998 patent is about combining patterns to achieve a final pattern. "Ultimately, the interpretation to be given a term can only be determined and confirmed with a full understanding of what the inventors actually invented and intended to envelop with the claim. The construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be, in the end, the correct construction." *Phillips*, at 1316 (*citing Renishaw PLC, v. Marposs Societa' Per Azioni*, 158 F.3d 1243 (Fed. Cir. 1998)). Thus, the "part of the first mask" that is combined in the broader "combined mask" term discussed below is the <u>first pattern</u>.

G. *"Combined Mask Including Parts of Said First Mask Layer and Said Second Photoresist"*

STC: Layering of the two lithographic patterns in the two layers and/or in the hard mask layer.	Intel: A single mask consisting of (i) parts of said first mask layer (defined above) and (ii) the patterned second photoresist, with each of the two independently shielding some part of the substrate not shielded by the other.

This term is properly construed in light of the claim language and explicit teachings in the specification: It is copied word-for-word from the specification at column 9, lines 57-59. Exh. 2 [Mack Dec.], at ¶38.

First, like the previous "parts of said first mask layer" term discussed above, this claim term is part of a larger phrase, which calls for the combination of *patterns*:

> transferring said ***first pattern*** and said ***second pattern*** into said substrate using a combined mask including ***parts of said first mask layer*** and said second photoresist;

Thus, STC's construction is consistent with the plain language of the larger claim term. Exh. 2 [Mack Dec.], at ¶39.

STC's construction is also consistent with the specification. The '998 Patent establishes that there are two ways a "combined mask" can be created, depending on the final structure being formed by the final pattern. For example, the embodiments disclosed in Figure 7 teaches both ways to create a combined mask, depending on whether one is make a structure that is above the surface (*e.g.*, bars, posts or pillars) or a structure that is below the surface (*e.g.*, holes). If a rectangular hole, with sharp corners is to be created, the embodiment of Figure 7 teaches that

> the vertical lines are in the nitride [hard mask], the horizontal lines are in the second photoresist layer. Together the two mask patterns provide a multiplication of the individual images . . . The composite mask pattern shows substantially right angles at the corners . . . .

Exh. 1 [‘998 Patent], at 13:23-30. Thus, Figure 7 teaches an embodiment where the “combined mask” consists of the pattern (i.e., the first mask layer) (nitride) and the pattern from the second photoresist layer. This embodiment, which requires the first mask layer and second photoresist layer to be physically present to transfer the final pattern, is covered by the precise language of STC’s construction for this term: the “layering of the two lithographic patterns in the two layers." Exh. 2 [Mack Dec.], at ¶40.

If rectangular shaped bars with square corners are to be produced, Figures 7 and 8 teach embodiments where the second photoresist is not physically present when the final pattern is transferred. Instead, the pattern from the second photoresist is transferred to the hardmask (the resist is then removed) to create a final pattern in the hardmask called the “combined mask.” Exh. 1 [‘998 Patent], at 11:22-28. The result of this embodiment is also covered by the precise language of STC’s construction: “the layering of the two lithographic patterns in the hard mask layer.” Exh. 2 [Mack Dec.], at ¶¶40-41.

The specification text associated with Figure 9 of the patent also teaches that the first pattern is transferred into a hard mask.

> With reference to FIG. 9C, any suitable etching process preferably transfers periodic pattern 48 (the lines) into hard mask 44. In a preferred embodiment, a very thin hard mask layer 44 is used such that the etching process does not have to be highly anisotropic.

Exh. 1 [‘998 Patent], at 15:62-63. The specification further teaches that the second pattern is created and then transferred into the same hard mask.

> With reference to FIG. 9D, a new photoresist layer 46 is suitably applied and structure 40 is suitably re-exposed and developed at substantially the same pitch, but with pattern 50 offset by $p_{min\ /2}$, thereby interpolating new lines 50 between (e.g. midway) previously defined lines 48 in hard mask 44. With reference to FIG. 9E, any suitable etching process preferably transfers lines 50 into hard mask material 44, thereby resulting in a pattern 48, 50 with about one half the pitch of original structure 40.

Id. at 16:1-9. The result of the Figure 9 (reproduced below) embodiment is also covered by the precise language of STC's construction of "combined mask": "the layering of the two lithographic patterns in the hard mask layer." Exh. 2 [Mack Dec.], at ¶42.

FIG. 9B

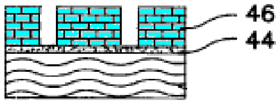


FIG. 9C

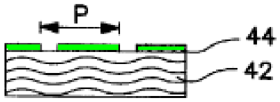


FIG. 9D

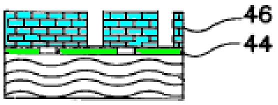
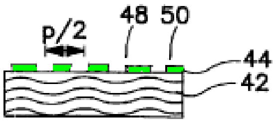


FIG. 9E



On the other hand, Intel's definition is extremely limiting and detached from the plain language of the claim, and the specific teachings of the patent; it would not cover the Fig 7 and 8 embodiments for bars, pillars and posts, and it would not cover the Fig. 9 embodiments. The patent law has long been clear that reading certain embodiments out of the claims of the patent, violates one of the basic tenants of claim construction: "a claim interpretation that excludes a preferred embodiment from the scope of the claim is rarely, if ever, correct." *MBO Labs.*, 474 F.3d at 1333. As explained in Dr. Mack's declaration, Intel's proposed construction does not provide for the manufacture of "posts" or "pillars" in the underlying layer, and only provides for the manufacture of "holes" when using the patterns of Fig. 7. Exh. 2 [Mack Dec.], at ¶¶43-51. Moreover, Intel's construction is incompatible with the combination of the two patterns through multiplication. *Id.*

Lastly, STC notes there is no mention in the ‘998 patent of the latter part of Intel’s proposed construction: “with each of the two independently shielding some part of the substrate not shielded by the other.” To the contrary, and as explained by Dr. Mack, Intel’s construction is not compatible with certain embodiments of the ‘998 patent. *Id.*

Dated: June 21, 2011

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CERTIFICATE OF SERVICE

The undersigned certifies that on the 21st day of June, 2011 the foregoing was filed electronically through the CM/ECF system, which caused all parties or counsel to be served by electronic means.

/s/ Steven R. Pedersen
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