Exhibit 2

Declaration of Dr. Chris Mack

UNITED STATES DISTRICT COURT
DISTRICT OF NEW MEXICO

STC.UNM, **Plaintiff,** **v.** **INTEL CORPORATION** **Defendant.**	**Civil No. 1:10-cv-01077-RB-WDS**

DECLARATION OF DR. CHRIS MACK

I, Chris Mack, under penalty of perjury, state as follows:

1. I have been retained by STC as a technical expert in the field of lithography, and have provided assistance to STC in developing its constructions for the claim terms of the '998 patent. I received my Ph.D from the University of Texas at Austin in 1998. For the past twenty eight years I have worked in the field of lithography in various capacities, including work for the federal government, private industry, and academia. In that time I have trained more than 2,500 lithographers from over 200 different companies around the world. I am currently an adjunct faculty member in the Electrical and Computer Engineering and Chemical Engineering Departments of the University of Texas at Austin. More information on my background can be found in my CV, which is attached as Exhibit A.

The Technology at Issue

2. Lithography advancements have been a driving force that allows for the fabrication of ever smaller components, *e.g.*, transistors, on semiconductor chips. The smaller the transistors, the more there are that can be packed on a chip, and the more powerful the chip. Today's semiconductors are made with minimum feature sizes of 32nm (22nm coming soon). For comparison, a human hair is about 60,000nm in diameter.

3. Semiconductor chips are made on silicon wafers. One wafer can contain over 300 billion transistors, and hundreds of chips are cut from a finished wafer. A semiconductor wafer is comprised of many layers. At the most basic level, the transistors are made first in semiconductive material, then the metal and insulating layers (the wires interconnecting features and circuit elements) are made on top of the transistors.

4. Lithography is used to pattern the various layers. First, a layer of photoresist is "spun" onto the wafer. Photoresist material is sensitive to light and allows for the transfer of an image through what is basically a photographic exposure process. In this process, laser light is used to expose a pattern on the photoresist. After the photoresist is exposed, portions of it become soluble and are washed away in developer. The pattern in the photoresist is then transferred by etching into the underlying layer.

5. Due to basic scientific principles that govern the physics of light, the lithography equipment that is used in current manufacturing processes has limitations. Those limitations prevent the manufacture of features smaller than about 37nm in dimension. In simple terms, the physics of light do not provide for sufficient resolution to make sub 37nm patterns on the wafer in the basic lithography sequence described above, using lithography manufacturing equipment available today. The invention disclosed in the '998 patent provides for a lithographic technique known as "double patterning" that allows for the extension to smaller feature dimensions and improved pattern quality. In this way, it is possible to fit a greater number of features on a wafer.

6. Much in the same way that sound can be described as being made up of frequency waves, the coordinates of two- and three- dimensional spatial objects can be described mathematically in frequency space. All physical objects, including the ultra-small transistors of a chip, can be described mathematically in frequency space. Those incredibly tiny features have spatial frequencies that correspond to their geometrical shape and distance from one another.

Spatial Frequencies

7. This technical term has a common understanding to those skilled in the art of lithography. The specification uses this term in a manner consistent with this common understanding.

8. One of ordinary skill in the art would review the teachings of the specification and conclude that the inventors used spatial frequencies to mathematically represent the physical patterns that were being created by the patented methods. This is evidenced by the Fourier transform equations disclosed in columns 12, 13 and 16 of the patent.

9. Intel's proposed construction, on the other hand, is unnecessarily limiting in that it only applies to repeating patterns. One of ordinary skill in the art would appreciate that spatial frequencies can be applied to isolated, non-repeating patterns just as well as to repeating patterns. STC's construction is compatible with such non-repeating patterns, but Intel's proposed construction is not.

10. Thus, the proper construction of this term is "a mathematical representation of a pattern. Technically defined, spatial frequencies are the coordinates in the Fourier plane resulting from the Fourier transform of the features that have been patterned."

High Spatial Frequencies

11. This claim term has a specific meaning in the context of the '998 patent and is properly construed in light of the teachings of the patent specification.

12. The magnitudes of "high spatial frequencies" are defined by two parameters in the '998 patent (1) frequencies found in the final pattern, but that are not present in either the first or second exposure, and (2) frequencies that are beyond the limits of the lithography equipment. Support for these two important parameters are set forth in the Abstract, Field of the Invention, and Summary of the Invention sections of the '998 patent. *See* Abstract; 1:66-2:7; 9:25-35.

13. Hallmarks of high spatial frequencies, as defined by the '998 Patent, include sharper corners, smaller feature sizes, or higher pattern density. Examples from the specification include:

> The ***quality of an image*** is limited by the spatial frequencies within the image. 2:10-11.
>
> * * *
>
> Thus, decreasing λ and increasing NA typically results in increased spatial frequency content and in an improved, ***higher resolution image***. 2:17-18 (emphasis added).
>
> * * *
>
> Historically, the semiconductor industry has worked to both decrease λ and increase NA in its steady progress towards ***smaller feature sizes***. 2:28-30 (emphasis added).
>
> * * *
>
> FIG. 11E shows a concept drawing of how the aforementioned frequency doubling technique might be applied to a circuit pattern, . . . changing the design to a CD grid would allow a straightforward doubling of the ***pattern density***. 18:18-26 (emphasis added).
>
> * * *
>
> FIG. 6B, namely rectangles with ***sharp, well-defined comers*** (12:59-60) (emphasis added).
>
> * * *
>
> While the image is significantly closer to the desired pattern than the incoherent imaging results, there is still significant rounding of the corners of the printed features due to the unavailability of the ***spatial frequencies needed to provide sharp corners***. 7:26-30 (emphasis added).

14. Intel's construction seems designed to exclude an important embodiment of the '998 Patent, one that is discussed at great length in the specification. Further, Intel's construction unnecessarily limits the application of spatial frequencies to dense patterns, so that the term "high spatial frequencies" is limited to only increases in the density of the pattern.

15. When describing a prior art method of forming patterns, the '998 Patent states

> "… there is still significant rounding of the corners of the printed features due to the unavailability of the spatial frequencies needed to provide sharp corners. That is, the magnitudes of the spatial frequencies necessary to define these corners are greater than $2/\lambda$, the limit of a linear optical system." ('998 Patent, 7:28-33)

16. Intel's construction specifically excludes this important result of "high spatial frequencies": spatial frequencies greater than the optical system could produce result in corners that are less rounded and more square.

17. Further in the specification, the prior art method of using two exposures without the non-linear (thresholding) processing step in between is described as producing rounded corners:

> "Because the intensities are added before the thresholding operation is applied, the resulting shapes exhibit significant rounding of the comers and are substantially elliptical rather than rectangular." ('998 Patent, 9:19-23)

18. Further, the specification makes clear that sharp corners are an important goal of the invention:

> "In contrast to the prior art methods which typically yield rounded corners on the structures as shown in FIG. 6A, the present invention suitably yields the patterns shown in FIG. 6B, namely rectangles with sharp, well-defined corners." ('998 Patent, 12:56-59)

19. Thus, Intel's claim construction will read out the embodiment illustrated in Figure 6B. In general, features with sharper corners can be placed closer together, so that making shaper corners can also be used to improve pattern density. Note, however, that the density of features shown in Figs. 6A (the prior art method) and 6B (the present invention) are the same. The only difference is in the sharpness of the corners.

20. Thus, the proper construction of this term is "The final pattern resulting from the below method steps have spatial frequencies (1) that are not present in any of the individual exposures, and (2) whose magnitudes are larger than the limit of the linear optical system response, resulting in sharper corners, smaller features, or higher pattern density."

Combining Nonlinear Functions of Intensity of at Least Two Exposures Combined With at Least One Nonlinear Processing Step Intermediate Between the Two Exposures

21. A person of ordinary skill in the art would properly understand this term based on the intrinsic evidence and a mathematical understanding of the word "function."

22. A mathematical function, by definition, has an output that depends on an input (the function assigns exactly one output to each input). For example, the mathematical functions sine and cosine have input variables, and outputs. Mathematical functions can, of course, be applied to real-world applications. An exemplary textbook reference providing such examples is attached hereto as Exhibit B, *Calculus, Concept and Contexts,* James Stewart, pp. 11-21 (2010) (discussing population as a function of time, etc.).

23. In the context of the "functions of intensity of at least two exposures" the claimed function is the exposure and subsequent processing (e.g., development) of photoresist. The input is the light energy that affects chemical change to the photoresist, and the output is the pattern formed in the resist. The input of the claimed exposure function, light energy, is used to affect change to the photoresist layer, which results in the output of a pattern.

24. The '998 patent describes the combination of the two output patterns as the combination of two input functions, and provides an example of combining the mathematical functions with multiplication at column 12, line 22 through column 13, line 14 (*see also* 16:8-33).

25. Intel's construction falls short as it does not specify that the output of the exposure function is a pattern, which is what the entire '998 patent is about, *i.e.*, the formation and combination of patterns.

26. Thus, the proper construction of this term is "combining the patterns that were formed in the two exposed photoresists, and having a non-linear process step, for example, development of the first resist, after the first exposure and before the second exposure."

[First/Second] Pattern in Said [First/Second] Photoresist Layer

27. A person of ordinary skill in the art would properly understand this term based on an examination of the plain language of the claim and specification.

28. The inventors described the patterns used by the claimed method as "shapes" at column 9, lines 19-23.

29. Thus, the proper construction of this term is "shape(s) resulting from developing the photoresist."

First Mask Material

30. A person of ordinary skill in the art would properly understand this term based on the plain language of the claim and the intrinsic evidence.

31. Hardmask materials were known to those skilled in the art at the time of the '998 Patent. What is unique to the '998 patent invention is the *use* that the hardmask is put to: preserving the first pattern so that it can be later combined with the second pattern in a combined mask through the use of the first mask material (which is commonly referred to as a hardmask). This is reflected in the plain language of the claim:

> ***transferring said first pattern into said first mask material***, said first mask material comprising at least one of SiO_2, $Si_3 N_4$, a metal, a polysilicon and a polymer;
>
> ***transferring said first pattern and said second pattern into said substrate using a combined mask*** including parts of said first mask layer and said second photoresist;

Thus, the construction of the claim term "first mask material" should reflect this usage.

32. The specification is also consistent with this meaning. The '998 Patent clearly illustrates the use of the first mask material as a method of preserving the first pattern for later use in the combined mask. Figs. 7, 8, 9 and 10 all illustrate the use of a hardmask (the first mask material) in order to preserve the first pattern after the first photoresist has been stripped away. When the second pattern is combined with the first pattern preserved in the first mask material, a combined mask results. *See also* column 12, lines 15-22.

33. Intel's proposed definition is vague as it defines "mask material" in the negative by merely defining what it is not.

Parts of Said First Mask Layer

34. This claim term is properly construed in light of the plain language of the larger claim term "transferring said first pattern and said second pattern into said substrate using a combined mask including parts of said first mask layer and said second photoresist," and the specification.

35. First, the larger claim term makes clear that what is being combined in the combined mask are *patterns:* "transferring said ***first pattern and said second pattern*** into said substrate using a combined mask . . ."

36. Consistent with the plain claim language, the specification teaches that the combined mask is a combination of two "patterns." And, consistent with all other aspects of the invention, the patent provides the mathematical detail of how the patterns are combined.

> Together ***the two mask patterns provide a multiplication*** of the individual images . . . ('998 Patent, at 13:23-29).

* * *

> Finally, FIG. 8C shows an exemplary result of ***multiplying the two patterns to get the final result***, thereby showing the dramatic improvement in the profiles. ('998 Patent, at 13:45-47).

* * *

> Thus, in a preferred embodiment, the ***combined etch mask provides the multiplication operation***. ('998 Patent, at 14:13-15).

See also 15:63-16:10 (mathematically combining two patterns by addition).

37. Thus, the proper construction of this term is "some or all of the first pattern from the first mask layer."

Combined Mask Including Parts of Said First Mask Layer and Said Second Photoresist

38. A person of ordinary skill in the art would properly understand this term in light of the plain language of the claim, and the teachings in the specification.

39. First, as mentioned above, the larger claim term makes clear that what is being combined in the combined mask are *patterns:* "transferring said ***first pattern and said second pattern*** into said substrate using a combined mask . . ."

40. The specification is also consistent with STC's construction. Figure 7 is an "experimental realization" that teaches an embodiment where the "combined mask" consists of the pattern (i.e., the first mask layer) (nitride) and the pattern from the second photoresist layer, and an embodiment where the second photoresist is not physically present in the combined mask when the final pattern is transferred. ('998 Patent, at 13:23-20).

41. Figure 8 teaches an embodiment where the second photoresist is not physically present when the final pattern is transferred through the use of a combined mask. ('998 Patent, at 13:32-51.

42. Figure 9 teaches an embodiment where the first pattern is transferred into a hard mask, and the second photoresist is not physically present in the combined mask. ('998 Patent, at 15:56 – 16:10).

43. Not only is Intel's proposed construction of this claim term unsupported by the intrinsic evidence of the '988 Patent, it in fact reads out important embodiments of the invention. Consider first the embodiment depicted in Fig. 8, reproduced below.

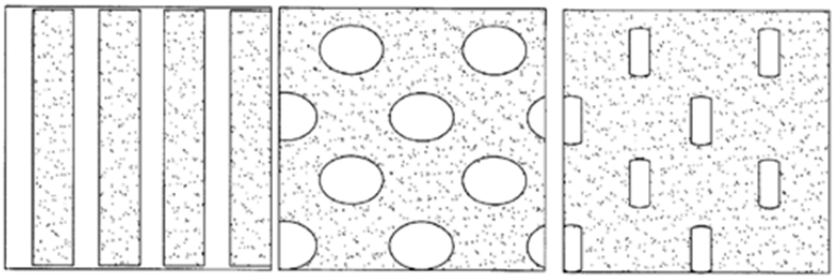


FIG. 8A FIG. 8B FIG. 8C

44. Fig. 8A shows the results of a first exposure and development of photoresist to form a pattern of long lines and spaces.

> "FIG. 8A shows an exemplary result of suitably applying a thresholding nonlinearity to a simple two-beam interferometric lithography exposure with a CD of 130 nm and a pitch of 260 nm." ('988 Patent, 13:34-37).

Figure 8B shows a pattern of oblong resist pillars.

> "FIG. 8B shows an exemplary pattern obtained from a conventional (incoherent illumination) optical lithography exposure of the mask corresponding to FIG. 1" ('988 Patent, 13:37-40).

Figure 8C shows the results of combining the two patterns of Figs. 8A and 8B in one embodiment of the invention.

> "Finally, FIG. 8C shows an exemplary result of multiplying the two patterns to get the final result, thereby showing the dramatic improvement in the profiles." ('988 Patent, 13:45-47).

45. Figure 1 is described as the pattern that is being fabricated using the steps depicted in Fig. 8.

> "FIGS. 8A-8C show exemplary results from a similar calculation for the prototypical array structure of FIG. 1." ('988 Patent, 13:32-33)

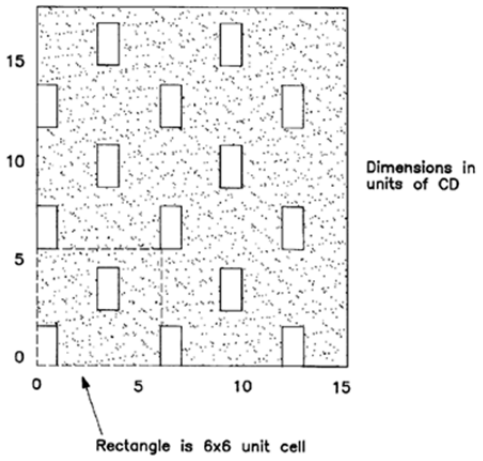


FIG. 1

46. Note that this figure uses the same illustrative style of clear rectangular regions surrounded by a speckled area. The description of Fig. 1 found earlier in the patent makes the nature of this pattern clear.

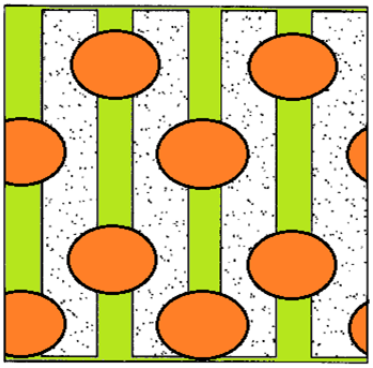
> "…FIG. 1 shows a prototypical array structure that might be part of a ultra-large-scale integrated circuit, particularly a circuit with a large degree of repetitiveness such as a memory chip or a programmable logic array. The dimensional units are in terms of the critical dimension (CD-smallest resolved image dimension) which is defined in the semiconductor industry roadmap. The industry goals for the CDs are 130 nm in 2003 and 100 nm in 2006. For easy comparison, the modeling examples given herein are all for the 130-nm CD generation. The pattern consists of **staggered bars** each 1x2 CD^2. The repetitive cell is demarked by the dotted lines and is 6x6 CD^2." ('988 Patent, 6:50-51, emphasis added)

The clear rectangular regions of Fig. 1 are described as "staggered bars". Thus, the clear white region is not a hole in the surrounding material, but rather a bar of the material sitting atop the substrate. It is obvious, then, that the final pattern shown in Fig. 8C is also a pattern of staggered bars of material (white regions) sitting on top of a substrate (speckled region). Likewise, in Figs. 8A and 8B the white regions represent photoresist material and the speckled regions are the material that the resist is sitting on top of.

47. With this understanding of the meaning of Fig. 8, it will be clear from the discussion below that STC's construction of the claim term "combined mask including parts of said first mask layer and said second photoresist" is compatible with the embodiment shown in Fig. 8, while Intel's claim construction will read out this embodiment.

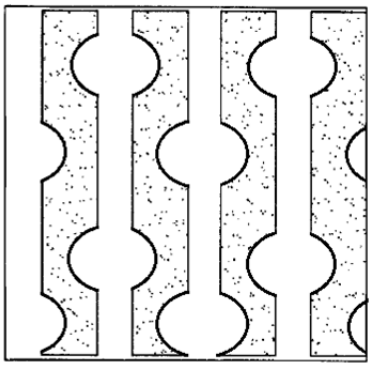
48. Applying the steps of claim 6 to the process of fabricating the final pattern in Fig. 8C, a first photoresist layer is coated, exposed and developed to form the patterns of lines and spaces shown in Fig. 8A (white region is the remaining resist after development). This pattern would then be etched into the underlying hardmask and the photoresist stripped away. Thus, the resulting hardmask pattern would also look like the pattern shown in Fig. 8A with the white regions representing the remaining hardmask material. Then, a second photoresist

would be coated, exposed and developed to form the pattern of Fig. 8B, with white regions representing the photoresist remaining after development. The result at this point would look that shown below, where here the hardmask material is depicted as green and the photoresist material is depicted as orange.



49. The details of the remaining steps are different under the two parties' claim constructions. Under the STC construction, it would be obvious that the final pattern of Fig. 8C would be produced if the second photoresist pattern were etched into the hardmask, resulting in a "multiplying" of the two resist patterns. Only the portions of the hardmask covered by the resist would remain. After the resist is stripped, the resulting pattern would look like Fig. 8C.

50. Under Intel's construction, however, a multiplying of the two patterns would not be possible. Instead, only addition of the two patterns is possible. If the "combined mask" of Intel's construction were transferred into the substrate, the final pattern would look like the image shown below:



51. There is no way to produce the pattern shown in Fig. 8C using Intel's construction. Thus, Intel's construction is not compatible with the embodiment depicted in Fig. 8. In fact, Intel's construction is not compatible with the idea of a combined mask that is the *multiplication* of the two individual patterns. Since the multiplication of patterns is clearly described as an important result of the invention of the '988 Patent, Intel's claim construction is completely incompatible with the intrinsic evidence found in the specification of the '988 patent.

52. Another example of where the Intel construction of the term "combined mask including parts of said first mask layer and said second photoresist" is unnecessarily limiting can be seen in Fig. 7. Here, an "experimental realization" is shown up to the patterning of the second

photoresist layer. First, a wafer is coated with the hardmask material and a first photoresist layer.

> "A Si wafer was coated with a thin Si3N4 film and with a first photoresist layer." ('988 Patent, 13:15-16)

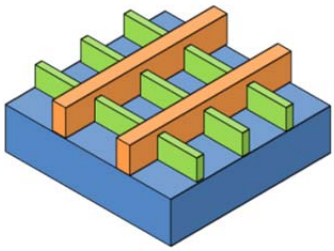
Next a pattern of lines and spaces are printed in the resist and etched into the hardmask.

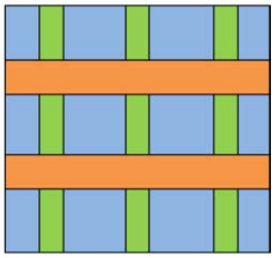
> "A two-beam interferometric exposure was used to define a line:space array in this first photoresist layer. The pattern was developed, transferred into the nitride film, and the remaining photoresist removed." ('988 Patent, 13:16-19)

Next, a second pattern of lines and spaces, perpendicular to the first, is imaged into a second photoresist layer on top of the previously patterned hardmask.

> "A second photoresist layer was then applied to the wafer and a second two-beam interferometric exposure, substantially at right angles to the first exposure pattern, was suitably applied and developed." ('988 Patent, 13:21-24)

53. The resulting pattern at this stage is shown in Fig. 7B. A diagrammatic view is shown below, where the substrate is in blue, the hardmask is green, and the second photoresist is shown in orange.



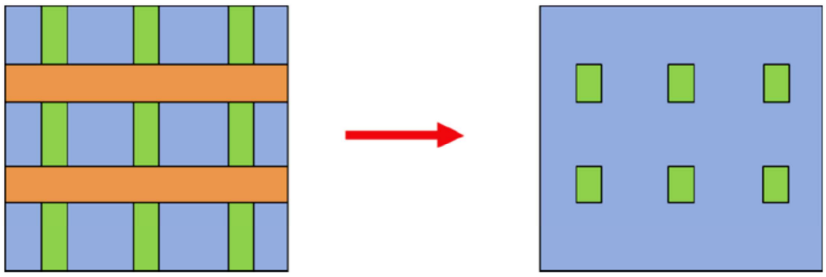


Top Down View

54. Here, the difference in construction between Intel and STC provides very different options as to how the patterns from the first and second photoresist layers can be combined. According to Intel's construction, the patterns can only be added, so that an etching of the "combined mask" into the substrate will result in square holes etched in the regions of the substrate not protected by hard mask *or* the second photoresist layer. Thus, addition of the two patterns produces an "or" pattern as a result – an array of square holes.

55. STC's construction certainly allows for this possibility, but also allows for the multiplication of the two patterns, where only those portions of the substrate protected by both the hardmask *and* the photoresist remain after etching. By etching the second resist pattern into the hard mask, square pillars of hardmask will remain after the second photoresist is

removed. Thus, multiplication of the two patterns produces an "and" pattern as a result – an array of square posts.



56. The '988 Patent clearly envisions both of these possibilities: multiplication as well as addition.

> "Upon suitable development and/or processing the result is a layering of the two lithographic patterns ***in the two layers and/or in the hard mask layer***." ('988 Patent, 9:55-59, emphasis added)

57. If there is a "layering" of two lithographic patterns *in the two layers*, the result is an addition of the patterns producing, in the case of Fig. 7, an array of square holes. If, however, there is a "layering" of two lithographic patterns *in the hard mask*, the result is a multiplication of the patterns, producing, in the case of Fig. 7, an array of square pillars. The clear meaning of the language of the specification envisions both possibilities. STC's claim construction, containing the same language found in the specification, follows the intent of the patent. Intel's construction, on the other hand, purposely limits the way in which the two lithographic patterns may be combined, eliminating the possibility of "layering" the two lithographic patterns in the hard mask.

58. Thus, the proper construction of this term is "layering of the two lithographic patterns in the two layers and/or in the hard mask layer."

Date: June 21, 2011

Dr. Chris Mack