STC.UNM v. Intel Corporation Doc. 133

UNITED STATES DISTRICT COURT
DISTRICT OF NEW MEXICO

STC.UNM, **Plaintiff,** **v.** **INTEL CORPORATION** **Defendant.**	**Civil No. 1:10-cv-01077-RB-WDS**

STC'S RESPONSIVE CLAIM CONSTRUCTION BRIEF

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TABLE OF CONTENTS

TABLE OF AUTHORITIES

CASES

I. Introduction

Intel advances several arguments that violate the basic canons of patent claim construction.

First, completely contrary to these canons, Intel attempts to exclude the "line trimming" embodiment (Figs. 6, 7 & 8) from the '998 patent, which is the very embodiment adopted by Intel in its accused products.

In doing so, Intel attempts to focus the Court on the other embodiment of the invention, "pitch splitting" (Figs. 9 & 10) that is not at issue in this case, and ignores the other relevant patent teachings associated with asserted claim 6. This is plainly seen in the background section of Intel's brief discussing the '998 patent. *See* Intel Br. [Doc. 110], at 9-14. Instead of using the figures of the '998 patent to explain what the patent discloses, Intel resorted to drawing its own figures illustrating the non-asserted "pitch splitting" embodiment.

As explained by STC, the '998 patent covers two basic embodiments of double patterning. The first embodiment, commonly referred to as "line trimming," found in Figures 6-8, is the embodiment STC is asserting against Intel. This embodiment creates raised rectangular bars or submerged rectangular trenches, with sharp corners and denser patterns. As illustrated below, a first pattern of lines is created in a first lithography sequence, and a second pattern is then created at an angle to the first. When those two patterns are combined, the second pattern cuts out, or "trims" a portion of the first pattern resulting in multiple rectangular features with squared off corners, as shown in the "top-down" images of Figure 6B of the patent, reproduced below. Hence, "line trimming."

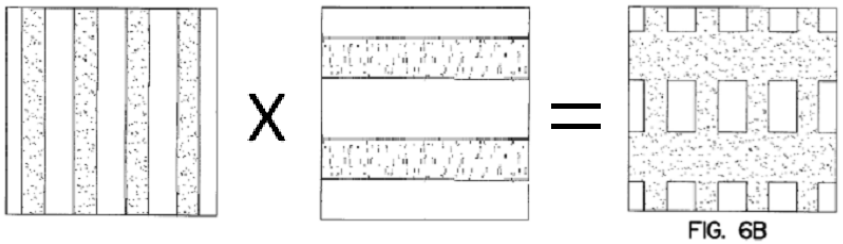
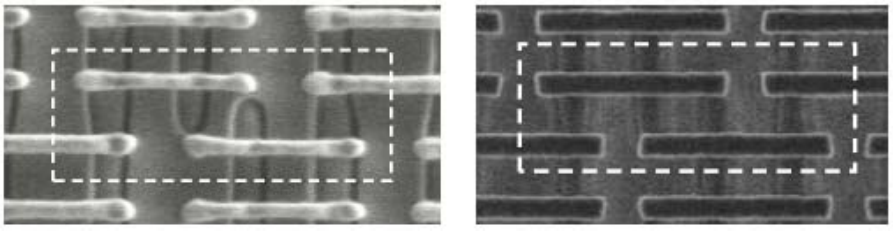


FIG. 6B

Intel's brief – *across the board* – flat out ignores this important embodiment. The reason Intel argues against STC's constructions on this issue is to increase its chances of avoiding infringement. Intel employs double patterning to create lined trimmed dense patterns with sharp corners in its leading edge products. Below are Intel's own SEM (scanning electron microscope) images comparing the resulting rounded corners for its prior 65nm process, and the sharp corners for its double patterned 45nm process.



SEM IMAGE OF INTEL'S 65NM PROCESS (LEFT) AND 45NM PROCESS (RIGHT)

Source: Exh. 3, [*Reducing Variation in Advanced Logic Technologies*, Kelin J. Kuhn, IEDM (2007) (slides 25-28).[1] Intel's attempt to read out of the patent claims the embodiments disclosed in Figures 6, 7 and 8 that teach the fabrication of line trimmed type patterns with sharp corners runs afoul of the basic tenants of claim construction.

Second, Intel's constructions focus on the physical layers of material used to transfer the patterns, and not the patterns themselves. This is in contrast to the plain claim language, and the focus of the patent, which is the combination of *patterns*. By construing the words in isolation, Intel's constructions torture the true meaning of the larger claim terms. In doing so, Intel, again, reads certain embodiments out of the specification.

Third, Intel tries to limit the last portion of claim 6, "combined mask," by again focusing on only one of the two ways taught by the patent specification for forming a combined mask, and

[1] *See also* Exh. 4 [*Intel Takes 45nm Process to IEDM, Shows Variability Data*, Semiconductor International (December 7, 2007)] (announcing use of double patterning).

ignoring the other way. Intel's construction for this term is doubly wrong: it attempts to exclude certain embodiments from the scope of the patent, and to import limitations from the specification into the claims, both of which are violation of the claim construction rules.

II. Argument

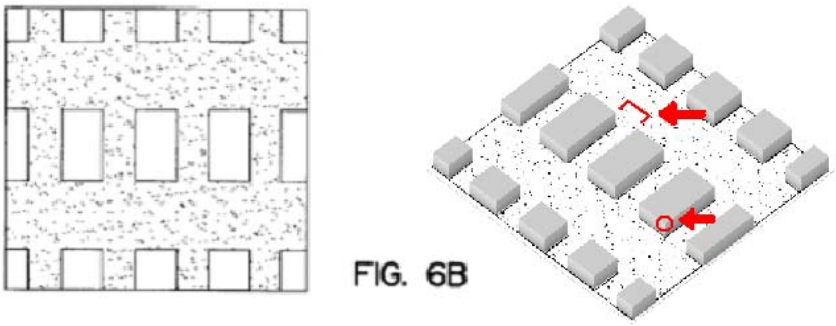
A. *"Spatial Frequencies"*

STC Br. at 11; Intel Br. at 15

STC: A mathematical representation of a pattern. Technically defined, spatial frequencies are the coordinates in the Fourier plane resulting from the Fourier transform of the features that have been patterned.	Intel: a measure of how often components of an image or pattern repeat in a given unit of distance Optional further explanation if the Court desires: "Technically speaking, a mathematical operation called the 'Fourier transform' represents the image or pattern as a series of waves, and 'spatial frequencies' indicate how frequently each of those waves repeats across space.

Intel is less than forthright when it states that the parties "essentially agree on what 'spatial frequencies' are, but differ somewhat on how to explain such a technical term to a lay audience." Intel Br. [Doc. 110], at 15. In fact, Intel's proposed definition is its first attempt to exclude the fabrication of square corners from the scope of claim 6, by limiting spatial frequency to a measure of how often a pattern repeats itself. On the other hand, STC's construction appropriately covers both embodiments of the patent, line trimming (Figures 6-8) and pitch splitting (Figures 9-10).

As explained by Dr. Mack, STC's expert, one of ordinary skill in the art would appreciate that spatial frequencies can be applied to isolated, non-repeating patterns as well as to repeating patterns. Exh. 2 [Mack Dec], at ¶9. In other words, there is spatial frequency information associated with a sharp corner found in a pattern, as well with how often a pattern repeats itself. This is pictorially shown in the below isometric view of Figure 6B.



TOP-DOWN AND ISOMETRIC VIEWS OF FIGURE 6B SHOWING SHARP CORNER AND REPEATING PATTERN

Dr. Mack's explanation is consistent with the teachings of the '998 patent, which specifically states that both a sharp corner of a patterned feature has spatial frequency information as well as the repeating pattern has spatial frequency information. For sharp corners, the patent teaches:

> While the image is significantly closer to the desired pattern than the incoherent imaging results, there is still significant rounding of the corners of the printed features due to the unavailability of the ***spatial frequencies needed to provide sharp corners***. (7:26-30) (emphasis added).

And for repeating pattern, the patent teaches:

> FIGS. 9A-9E show a preferred embodiment for a sequence using subtractive fabrication processes that results in an approximate factor of two increase in the ***spatial period***; i.e. a reduction of a factor of two in the pitch. (15:37-40).

For its part, Intel avoids the teachings of the patent and, instead, cites to extrinsic evidence in the form of general technical articles discussing Fourier theory. Intel Br. [Doc. 110], at 15-16. Oddly, Intel neither quotes from any of these highly technical publications, nor cites to any specific pages or portions thereof from the 21 pages. Where, as here, the teaching of the patent is explanatory, controlling Federal Circuit law cautions against such claim construction analysis. Indeed, the *en banc Phillips* decision clarified that "the specification is the single best guide to the meaning of a disputed term," and that the specification "acts as a dictionary when it expressly

defines terms used in the claims or when it defines terms by implication." *Phillips*, at 1320-21 (*citing Vitronics*, 90 F.3d at 1582).[2] The *Phillips* decision further noted that:

> There is no guarantee that a term is used in the same way in a treatise as it would be by the patentee. In fact, discrepancies between the patent and treatises are apt to be common because the patent by its nature describes something novel. *See Autogiro*, 384 F.2d at 397 ("Often the invention is novel and words do not exist to describe it. The dictionary does not always keep abreast of the inventor. It cannot.").

Finally, *Phillips* holds that when the specification may reveal a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess, the inventor's lexicography governs. *Phillips*, at 1316. Thus, STC's construction, which is consistent with the patent specification, should be adopted.

B. *"A Pattern Wherein the Fourier Transform of Said Pattern Contains High Spatial Frequencies"*

STC Br. at 13; Intel Br. at 17

STC: The final pattern resulting from the below method steps have spatial frequencies (1) that are not present in any of the individual exposures, and (2) whose magnitudes are larger than the limit of the linear optical system response, resulting in sharper corners, smaller features, or higher pattern density.	Intel: a pattern whose density in the x–y plane (the plane of the substrate) is greater than the optical system could produce

1. Intel's Construction Reads the Fabrication of Sharp Corners Out of the Specification

Intel's restrictive definition of this term, limiting it to pattern density, continues its attempt to exclude the fabrication of sharp corners from the scope of the '998 patent.

[2] *See also Irdeto Access, Inc. v. Echostar Satellite Corp.*, 383 F.3d 1295, 1300 (Fed. Cir. 2004) ("Even when guidance is not provided in explicit definitional format, the specification may define claim terms by implication such that the meaning may be found in or ascertained by a reading of the patent documents.") (citations omitted); *Novartis Pharms. Corp. v. Abbott Labs.*, 375 F.3d 1328, 1334-35 (Fed. Cir. 2004) (same); *Bell Atl. Network Servs., Inc. v. Covad Communications Group, Inc.*, 262 F.3d 1258, 1268 (Fed. Cir. 2001) ("[A] claim term may be clearly redefined without an explicit statement of redefinition.").

There can be no doubt that the fabrication of sharp corners that result from the line trimming embodiment is a primary goal of the invention. When describing a prior art method of forming patterns, the '998 patent states:

> … there is still significant rounding of the corners of the printed features due to the unavailability of the spatial frequencies needed to provide sharp corners. That is, the magnitudes of the spatial frequencies necessary to define these ***corners*** are greater than $2/\lambda$, the limit of a linear optical system.

Exh. 1 ['998 Patent], at 7:28-33. Further, the specification describes one of the shortcomings of the prior art is rounded corners:

> Because the intensities are added before the thresholding operation is applied, the resulting shapes exhibit significant rounding of the comers and are substantially elliptical rather than rectangular.

Id., at 9:19-23. Moreover, the specification makes clear that sharp corners are an important goal of the invention:

> In contrast to the prior art methods which typically yield rounded corners on the structures as shown in FIG. 6A, the present invention suitably yields the patterns shown in FIG. 6B, namely rectangles with sharp, ***well-defined corners***.

Id., at 12:56-59.

Since Intel contends that square corners do not contain "high spatial frequencies," as required by the claim (Intel Br. [Doc. 110], at 20), Intel's construction reads out the embodiment illustrated in Figure 6B, as well as other figures as shown below.[3] Exh. 2 [Mack Dec.], at ¶¶14-19.[4] As previously discussed, a claim interpretation that excludes a preferred embodiment from

[3] In general, features with sharper corners can be placed closer together, so that making shaper corners can also be used to improve pattern density. (Note, Figs. 6A & 6B only illustrate increased spatial frequencies from going from round holes to square holes, not the further benefit of increased density.) Exh. 2 [Mack Dec.], at ¶19.

[4] The line trimming embodiment, which fabricates square corners, is also disclosed in Figures 7 & 8.

the scope of the claim is rarely, if ever, correct, and would require "highly persuasive evidentiary support." *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1583 (Fed. Cir. 1996).

2. Intel's Specification Argument is Wrong and Misleading

For its part, Intel argues that because the applicants did not invent the use of developing photoresist to achieve spatial frequencies beyond the limit of the optical system, the scope of the patent should somehow exclude the fabrication of sharp corners. Intel Br. [Doc. 110], at 18-19. The portion of the specification that Intel cites – "*Background of the Invention*" – is a discussion of the deficiencies in the prior art. That is, the inventors were discussing how photoresist development in one resist layer does not result in higher pattern density. Exh. 1 ['998 Patent], at 8:60-63 (discussing the use of one layer of resist).

In the very next concluding paragraph of this patent section, however, the inventors also discussed how corner rounding is another deficiency associated with the prior art. Exh. 1 ['998 Patent], at 9:9-24. Thus, when read in context, the inventors were actually framing two problems overcome by the invention: the achievement of high spatial frequencies to achieve denser patterns, and square corners. Accordingly, Intel's argument that the scope of the patent should exclude the fabrication of sharp corners is wrong.

3. Intel's Prosecution History Argument is Wrong

Intel next makes a long, convoluted argument about statements that the applicants made to the PTO during the prosecution of the '998 patent. Intel Br. [Doc. 110], at 19-20. Although the prosecution history may also be considered, "it often lacks the clarity of the specification and thus is less useful for claim construction purposes." *Phillips*, 415 F.3d, at 1317. For this reason, "[p]recedent requires that the alleged disavowing actions or statements made during prosecution be both clear and unmistakable." *Omega Eng'g*, 334 F.3d, at 1326. As shown below, STC never

made any statements in the prosecution history that disavowed claim coverage for the fabrication of patterns containing high spatial frequencies with sharp corners.

Essentially, Intel contends that STC represented to the PTO that the formation of sharp corners does not result in higher spatial frequencies. Intel Br. [Doc. 110], at 19. This is contrary to the teachings of the specification (outlined above), and simply not true. STC actually explained in the prosecution history that the patent discloses two separate embodiments, to achieve high spatial frequencies:

> The presently claimed invention ***alters the frequency distribution of the final structure*** by (i) ***increasing the pattern density*** in the plane of the wafer to periods less than λ/2 in at least one direction (interpolation of the gratings); and (ii) changing the features of a pattern in a desirable way without increasing the density such as, for example, ***round holes to square holes***.

Exh. 5 [Response and Amendment, January 14, 1999], at 8 (emphasis added); Exh. 7 [Mack Dec], at ¶60. With respect to the embodiments disclosed in Figures 6 and 7, which disclose the fabrication of sharp corners, the applicants actually stated:

> The presently claimed invention ***also changes magnitudes and phases of the Fourier coefficients*** between the process described by (expose, expose, nonlinear) and (expose, nonlinear, expose, nonlinear). ***Figures 6 and 7 exemplify this result by the demonstration of the round hole to square hole transition.*** Both of the patterns have the same spatial frequencies; however, the round (or elliptical) holes have a distribution of frequencies that radiates outward from the center of frequency space, while the square holes have frequencies only in the x and y directions perpendicular to the sides of the holes. The roll-off of the magnitudes of the Fourier coefficients is a more rapid function of the magnitude of the frequency in the round case than in the square case.

Id., at 9; Exh. 7 [Mack Dec], at ¶61. Consistent with STC's construction, the inventors further stated in the prosecution history that the "increase in frequency" results from the increase in the number of the "significant terms" in the Fourier series. *Id.*, at 7; Exh. 7 [Mack Dec], at ¶62. Thus, the applicants did indeed state that the formation of square holes changes the frequency distribution of the final structure. By combining the patterns, the ***magnitudes and phases*** of the

spatial frequencies in the final pattern are increased beyond the limit of a linear optical system, which *as the patent explicitly states*, are the high spatial frequencies necessary to create patterns with sharp corners. Exh. 7 [Mack Dec], at ¶63.

> there is still significant rounding of the corners . . . due to the unavailability of the spatial frequencies needed to provide sharp corners . . . the ***magnitudes*** of the spatial frequencies necessary to define these corners are greater than $2/\lambda$, the limit of a linear optical system.

Exh. 1 ['998 Patent, 7:28-33]; *see also* Exh. 2 [Mack Dec], at ¶15.[5]

On the other hand, Intel's argument hinges upon twisting what was meant by applicants' statements that "both of the patterns have the same spatial frequencies." Intel Br. [Doc. 110], at 19. As explained by Intel's own expert, however,

> The lowest spatial frequency terms for a given pattern represent its basic shape, location, and periodicity. These terms may be sufficient to image the basic structure of a pattern. The higher spatial frequency terms represent the finer feature detail, such as the ***sharp edges***.

Smith Dec. [Doc. 111], at ¶7. (emphasis added). Thus, STC was correct when it stated that the patterns can have the same spatial frequencies (corresponding to basic shape, location and periodicity), but also have higher spatial frequencies present that correspond to "the finer feature detail, such as the sharp edges" (sharp corners). By increasing the magnitude of the higher spatial frequency terms, round corners can become sharp corners. Exh. 7 [Mack Dec], at ¶64-66.

In sum, STC never made any statements during the prosecution of the patent that can serve the basis of a "clear and unmistakable" surrender of claim coverage for high spatial frequency patterns through the fabrication of sharp corners. In fact, the opposite is true. STC specifically

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[5] STC notes that, consistent with its construction, the inventors also defined higher spatial frequencies to correspond to small features sizes: "By obtaining the higher spatial frequencies using the nonlinear process, the presently claim invention can create smaller features because the higher spatial frequencies correspond to the small features." Exh. 6, [Response and Amendment, May 18, 1999], at 6.

said that the changed frequency distribution, *i.e.*, high spatial frequencies, results in sharp corners found in Figure 6 and 7.

4. Intel's Magnitude Argument is Wrong

Next, Intel argues that STC's definition is deficient because it does not define the magnitude of "sharper corners, smaller features, or higher pattern density." This is all unsupported attorney argument, and nonsense. The entire '998 patent is about the achievement of spatial frequencies and corresponding patterns that cannot be fabricated with one lithography sequence. Thus, STC's inclusion of "sharper corners, smaller features, or higher pattern density" in its definition is in reference to corners that are sharper than possible in one lithography sequence, features that are smaller than possible in one lithography sequence, and patterns that are denser than possible in one lithography sequence. This is reflected in the two parameter restrictions explicitly set forth in STC's construction, which were repeated in the Abstract, Field of the Invention, and Summary of the Invention sections of the '998 patent: (1) that are not present in any of the individual exposures, and (2) whose magnitudes are larger than the limit of the linear optical system response. Exh. 2 [Mack Dec], at ¶12; Exh. 1 ['998 Patent], at Abstract; 1:66-2:7; 9:25-35.

5. The Inventors' Lexicography Governs

Finally, as mentioned above, it is a concrete principle of claim construction that when a patentee attributes special meaning to the words that he uses to describe the claimed invention, his or her definition will govern the meaning of the claim term. *Phillips,* 415 F.3d at 1316 ("the inventor's lexicography governs"). In this case, there can be no doubt that, based on the teachings of the specification, and consistent statements in the prosecution history, the inventors defined high spatial frequencies to be those (1) that are not present in any of the individual exposures,

and (2) whose magnitudes are larger than the limit of the linear optical system response, that result in sharper corners, smaller features, or higher pattern density.

C. "Combining Nonlinear Functions of Intensity of at Least Two Exposures Combined With at Least One Nonlinear Processing Step Intermediate Between the Two Exposures"

STC Br. at 15; Intel Br. at 21

STC**:** Combining the patterns that were formed in the two exposed photoresists, and having a non-linear process step, for example, development of the first resist, after the first exposure and before the second exposure.	Intel**:** Combining the response of two exposures of photoresist and at least one non-linear processing step (for example, development of the first photoresist) that occurs after the first exposure and before the second exposure

This issue is clearly drawn: What is combined, "patterns" as STC contends or "responses," as Intel contends?

Intel makes no real attempt to defend its position (other than criticizing STC's). More striking, it does not even inform us what it is referring to by *responses*. The only thing Intel tells us is that the *responses* are not the *patterns:* "The focus is on the response of the photoresist to the two *exposures*, not the patterns that later result." This suggests that the *responses* are something that exist before the patterns are formed. What that is remains a mystery.

Intel's first critique of STC's position is that this claim language "…does not discuss combining *patterns*." Intel Br. [Doc. 110], at 21. But that gets us nowhere since this claim language also does not discuss combining *responses*.

Intel's repeats this faulty analysis when it states: "Second, neither the preamble nor the body of the claim 6 refers to combining patterns *formed in the two photoresist layers*." ***Id.*** But, again, neither do they refer to Intel's suggested construction, *response of two exposures of photoresist*.

Intel then makes what appears to a damning admission: "…the body of the claim makes clear that the ***combination of patterns*** occurs by using a 'combined mask' of the *first mask layer* and

the *second photoresist* to ***transfer both patterns*** to the substrate." *Id.* (emphasis added). Putting aside that Intel is probably getting ahead of itself by putting forth its "combined mask" argument, it is conceding that what is combined are the *patterns*, not *responses*.

This becomes even clearer when the language in question is read in the context of the claim. It appears in the preamble of the claim, giving an overview of the claim: The high spatial frequencies are obtained by combining the defined patterns.

Finally, Intel makes a ridiculous interpretation of STC's construction: "Nowhere does the claim refer to combining the two exposed photoresist layers, as STC's construction would suggest." *Id.* Neither STC nor its construction suggest any such thing. STC's construction means exactly what it says, "combining patterns" means combining patterns.

D. *"[First/Second] Pattern in Said [First/Second] Photoresist Layer"*
STC Br. at 17; Intel Br. at 23[6]

STC: Shape(s) resulting from developing the photoresist	Intel: the configuration of the [first/second] photoresist layer remaining after developing

This issue can be more easily understood if one considers what is done with the *patterns* in the photoresist layers. The patterns are transferred; the first pattern is transferred into the first mask material and both the first and second patterns are then transferred into the substrate. In each case the patterns are transferred into physical things, but patterns themselves are non-physical things.

This gets us to the crux of the parties' disagreement. STC's construction says the patterns are non-physical things, "shapes," which the patent uses as being synonymous with patterns. Exh. 1

[6] Section D and E are reversed in the briefs of the parties, thus the subject of this section D is section E in Intel's brief

['998 Patent], at 9:19-23. Intel's construction says that the patterns are physical things: "the configuration of the photoresist layer remaining after developing." Intel emphasizes the physical nature of the patterns when it argues: "Intel's construction makes clear that the pattern in a photoresist layer is *what remains of that layer after it has been exposed and developed*." Intel Br. [Doc. 110], at 23. Clearly that physical thing -- *what remains of the resist layer after it has been exposed and developed* -- is not what is transferred when the pattern is transferred. What is transferred is non-physical, the "shape." There is no teaching in the patent, or in the art, supporting Intel's construction.

E. *"First Mask Material"*
STC Br. at 18; Intel Br. at 22

STC: A layer of material used to preserve the first pattern for later use in the combined mask.	Intel**:** Material that is not photoresist, and that shields some or all of the underlying layer.

Intel agrees in its brief that STC's construction is accurate and supported by the plain claim language: "Intel agrees that the first mask material is used 'to preserve the first pattern for later use in the combined mask' . . . " Intel Br. [Doc. 110], at 22. Intel primarily argues that STC's original construction is insufficient as it does not specify that the first mask layer is not photoresist. *Id.* at 22-23. But the claim language also makes clear that the "first mask material" and "photoresist layer" are two distinct layers. Specifically, Claim 6 recites: "coating a substrate with a first mask material ***and*** a first photoresist layer;" Exh. 1 ['998 Patent], at Claim 6. Thus, Intel's criticism of STC's construction is baseless.

The real issue comes down to this: Should the construction define what masks are in general, or focus on the first mask taught and claimed in the patent? The Federal Circuit Court of Appeals supplies the answer, thus effectively rejecting Intel's dictionary approach (Intel Br. at 22).

> [G]eneral dictionaries, in particular, strive to collect all uses of particular words, from the common to the obscure. By design, general dictionaries collect the definitions of a term as used not only in a particular art field, but in many different settings. In such circumstances, it is inevitable that the multiple dictionary definitions for a term will extend beyond the construction of the patent [that] is confirmed by the avowed understanding of the patentee, expressed by him, or on his behalf, when his application for the original patent was pending. Thus, the use of the dictionary may extend patent protection beyond what should properly be afforded by the inventor's patent. For that reason, we have stated that a general-usage dictionary cannot overcome art-specific evidence of the meaning" of a claim term.

Phillips, at 1321-22 (citations omitted).

Intel also seems to have difficulty in accepting a construction that informs what the use of the mask is in the patented scheme. But definitions of man-made objects almost always include the use(s) to which the object is put. It is not particularly helpful to define a hammer by just saying "a handle with an attached head," or a pencil as just "a wooden cylinder with a rod of graphite within." One wants to know, and dictionaries will tell us, what it is used for.

So here, the judges and the jury that will rely on these claim constructions will want to know what is the mask and what is it used for. STC's construction answers both questions: *a layer of material used to preserve the first pattern for later use in the combined mask.*

F. *"Parts of Said First Mask Layer"*
STC Br. at 20; Intel Br. at 23

STC: Some or all of the first pattern from the first mask layer.	Intel: the portions of the 'first mask material' that remain after the first 'transferring' step

As previously mentioned, STC submits that the last two claim terms at issue cannot be properly construed in a vacuum, and must be considered in the context of the larger claim limitation set forth below, which discusses a combination of patterns:

> transferring said first pattern and said second pattern into said substrate using a combined mask including parts of said first mask layer and said second photoresist;

Intel's construction for this term is yet another example of how it is attempting to torture the meaning of the claims to fashion a non-infringement defense that focuses on the physical layers of material used to transfer the patterns, and not the patterns themselves.

While the term "all" is not in its proposed construction, Intel argues in its brief that "all" of the first pattern is transferred into the substrate even though the claim says "parts" and not "all." Intel Br. [Doc. 110], at 24. In support of its construction, Intel discusses only one embodiment from the '998 patent found in column 14. The problem with Intel's argument is that the particular embodiment discussed by Intel does not make reference to any of the patent figures, and completely ignores other embodiments in the patent that utilize a first mask layer in a different manner than Intel contends is proper.

For example, in the context of Figure 7, the first pattern is transferred to a hard mask material, *i.e.,* first mask layer. Then, a second pattern of lines and spaces is created at a right angle to the first pattern atop the first mask material, and combined to form the final pattern, as shown in Fig. 7B. Exh. 1 ['988 Patent], at 13:15-31. An isometric view of Figure 7B is shown below, where the substrate is in blue, the hardmask is green, and the second photoresist is shown in orange.

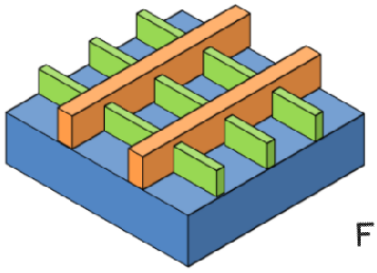
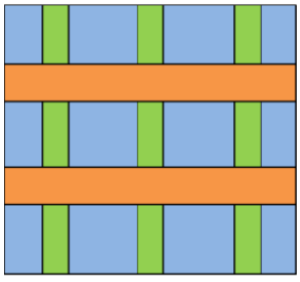


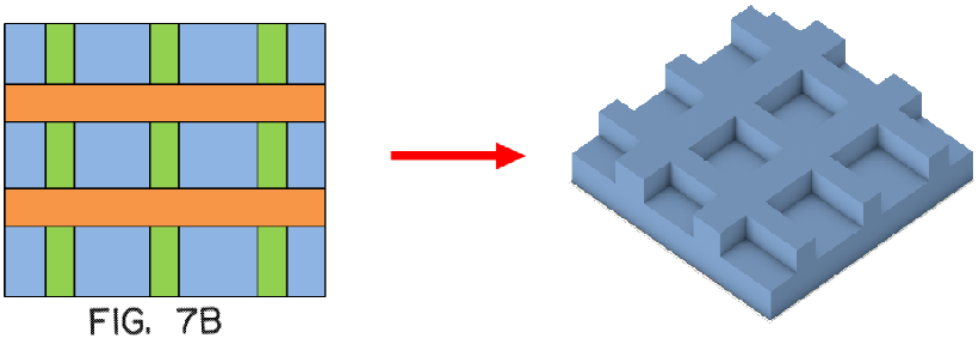
FIG. 7B



Top Down View

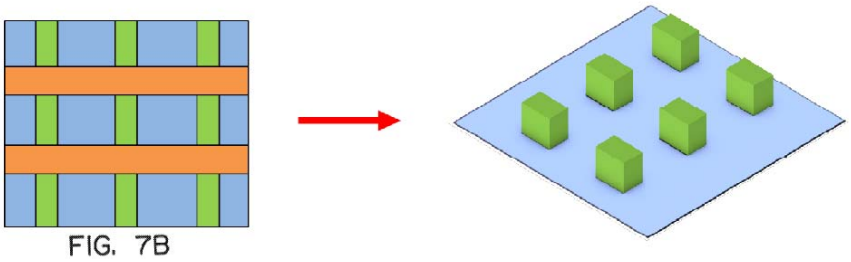
From this point, and as explained by Dr. Mack, there are different options as to how the patterns from the first and second photoresist layers can be combined to create the final pattern in

the blue substrate. Exh. 2 [Mack Dec.], at ¶53-55. As shown, below, the patterns can be added and used as an etch mask to manufacture an array of square holes. In this first scenario, the portion of the first pattern in the green mask layer that is covered by the orange second resist is not used in the combined mask, and thus not transferred to the blue substrate.



ISOMETRIC VIEWS OF FIG. 7 RESULTING IN ARRAY OF SQUARE HOLES

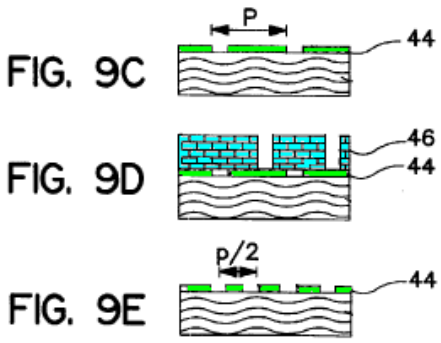
Alternatively, the second orange resist pattern can be multiplied with the patterned hard mask, creating an array of bars that remain after the second photoresist is removed. In this scenario, only the portion of the green mask layer that is protected by the orange second resist is used in the combined mask, and thus transferred. *Id.*



ISOMETRIC VIEWS OF FIG. 7 RESULTING IN ARRAY OF PILLARS

In either case, Figure 7B demonstrates that only a portion of the first pattern is transferred to the substrate. Critically, it is this embodiment of the patent, "line trimming," that Intel uses in its products accused to infringe.

In the other embodiment of the '998 patent, "pitch splitting," "all" of the first pattern is transferred to the substrate. This is because the first and second patterns do not overlap so as to form the closely spaced lines and spaces. Instead, a first pattern of lines and spaces is created, and then a second pattern of lines and spaces is located between the lines of the first pattern. Exh. 1 ['998 Patent], at 15:55-16:10. As shown in the below Figure 9 from the patent, the entirety of both patterns, including the pattern preserved in the first mask material, are transferred to the substrate in the combined mask.



In sum, STC's construction is appropriate because its use of the words "some or all" covers both embodiments, line trimming which creates sharp corners (Fig. 6-8), and pitch splitting which creates closely spaced lines and spaces (Figs. 9-10). In contrast, Intel's construction must be rejected because it reads the sharp corner embodiment out of the specification. As repeated throughout this brief, and Federal Circuit jurisprudence, "a claim interpretation that excludes a preferred embodiment from the scope of the claim 'is rarely, if ever, correct.'" *On-Line Technologies, Inc., v. Bodenseewerk Perkin-Elmer GMBH,* 386 F.3d 1133 (Fed. Cir. 2004) *citing Globetrotter Software, Inc. v. Elan Computer Group, Inc.*, 362 F.3d 1367, 1381 (Fed. Cir. 2004), *see also Int'l Rectifier Corp. v. IXYS Corp.*, 361 F.3d 1363, 1371 (Fed. Cir. 2004); *Modine Mfg. Co. v. U.S. Int'l Trade Comm'n*, 75 F.3d 1545, 1550 (Fed. Cir. 1990).

G. *"Combined Mask Including Parts of Said First Mask Layerand Said Second Photoresist"*
STC Br. at 22; Intel Br. at 26

STC: Layering of the two lithographic patterns in the two layers and/or in the hard mask layer.	Intel: A single mask consisting of (i) parts of said first mask layer (defined above) and (ii) the patterned second photoresist, with each of the two independently shielding some part of the substrate not shielded by the other.

Intel finds itself in a tight spot; STC's construction is lifted verbatim from the patent specification. Not only that, but it is taken from the initial discussion of the embodiment that covers "line trimming," the embodiment at issue in this case. The inventors explicitly teach that the final step of transferring the two patterns to the substrate can be done in either of two ways: 1) use both the second resist and first mask as separate entities, or 2) first transfer the pattern from the second resist into the first mask and then use that combined mask to transfer both patterns to the substrate. The quote is: "…the result is a layering of the two lithographic patterns in the two layers and/or in the hard mask layer." Exh 1 ['998 Patent], 9:57-59.

Read in context, it is absolutely clear that the inventors are saying that there are two ways of transferring the two patterns to the substrate:

> a first lithographic pattern at a first wavelength regime is suitably exposed into the first photosensitive layer and a second lithographic pattern in a second wavelength regime is suitably exposed into the second photosensitive layer. Upon suitable development and/or processing *the result is a layering of the two lithographic patterns in the two layers and/or in the hard mask layer. These layers in combination are used as masks for further processing of the underlying wafer to transfer a pattern that is the product of the two masks into the underlying materials.*

Id. Intel's proposed construction would limit the claim to just the first way (and, of course, Intel is using the second way).

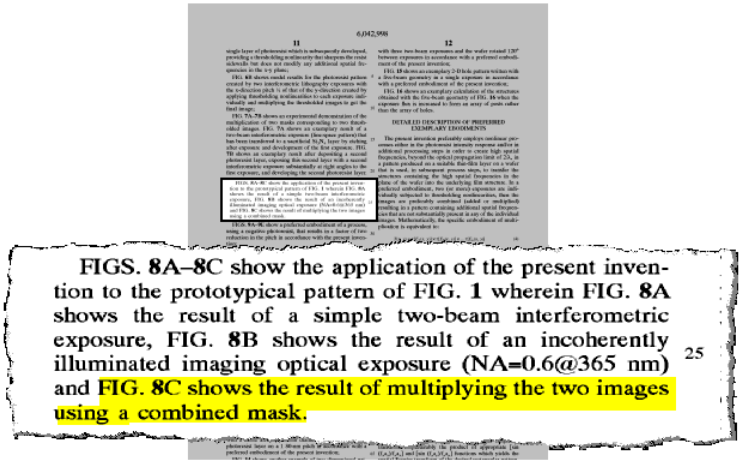
There is a second grave problem with Intel's construction. Certain structures taught by the patent, and crucial to the semiconductor industry, cannot be made unless the second way is used.

As explained by Dr. Mack, Intel's construction is incompatible with embodiments that "multiply" the two patterns to achieve the final pattern.[7] The '998 patent discloses that the two patterns can be mathematically combined in one of two ways: the patterns can be multiplied to achieve a final pattern, or added together to achieve a final pattern.[8] For example, Figure 6, which discloses the line trimming embodiment that creates sharp corners multiplies the first and second pattern to achieve the final pattern. The Fourier equation disclosed in column 13 clearly shows that the two sine functions are multiplied together. Exh. 1 ['998 Patent], 12:64-13:10. Figure 9, on the other hand, discloses the "pitch splitting" embodiment which creates closely spaced lines and spaces, and the Fourier equation disclosed in column 16 clearly shows that the two sine functions are added together. Exh. 1 ['998 Patent], 16:10-27.

Figure 8, which is an embodiment explicitly described by the inventors as using a "combined mask," is an embodiment that discloses a multiplication of the first and second patterns. Exh. 1 ['998 Patent], at 11:22-27; 13:45-45.

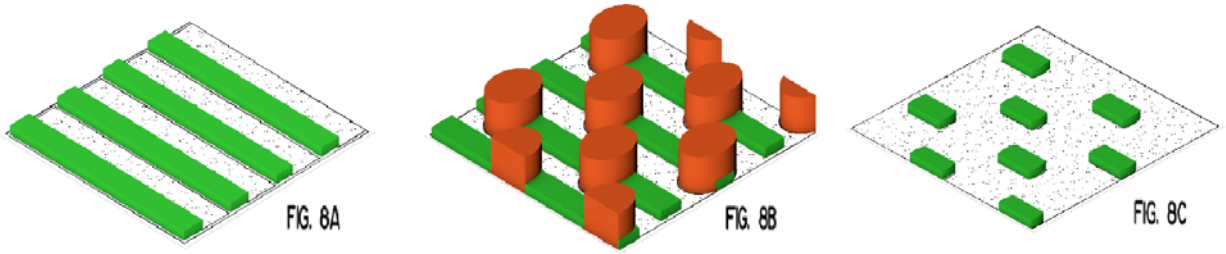
[7] Dr. Mack's explanation of how Intel's construction is incompatible with the idea of a combined mask that is the multiplication of the two individual patterns, is based upon the presence or absence of photoresist. As explained further by Dr. Mack in his declaration filed herewith, Intel's construction is not compatible either the multiplication of patterns, or the addition of patterns, but not both, depending on how the presence or absence of photoresist is defined. Exh. 7 [Mack Dec.], at ¶67.

[8] *See* Exh. 1 ['998 Patent], at 13:26-27; 13:45-47; 14:13-15 (mathematically combining two patterns by multiplication); 15:63-16:10 (mathematically combining two patterns by addition); Exh. 2 [Mack Dec.], at ¶36.



FIGS. 8A–8C show the application of the present invention to the prototypical pattern of FIG. 1 wherein FIG. 8A shows the result of a simple two-beam interferometric exposure, FIG. 8B shows the result of an incoherently illuminated imaging optical exposure (NA=0.6@365 nm) and FIG. 8C shows the result of multiplying the two images using a combined mask.

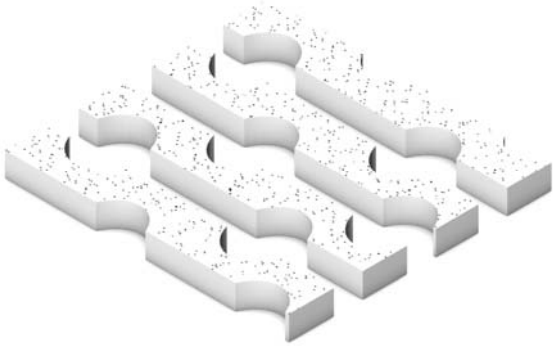
Below are enhanced isometric views of Figures 8A-C, where the green regions represent hard mask material of the first pattern and the speckled regions represents the substrate, the material that the mask is sitting on top of. Exh. 2 [Mack Dec.], at ¶47-48. As shown below, the orange oval patterns in the second layer of resist were transferred to the green mask layer to achieve the results depicted in Figure 8C. In other words, the second layer of orange oval patterns was used as a shield in order to further pattern the green underlying mask layer of lines and spaces. Then, the second layer of orange photoresist was removed, leaving only green combined patterned mask material. The result is shown in Figure 8C. Exh. 2 [Mack Dec.], at ¶49.



ISOMETRIC VIEWS OF FIGS 8A, 8B AND 8C

Under Intel's construction, however, a combining of the two patterns where the second layer of resist is still present when the two patterns are transferred to the substrate, *i.e.*, etched, would result in shapes that are not described in Figure 8. If the "combined mask" of Intel's construction were etched into the substrate, the final pattern would look like the image shown below. Exh. 2

[Mack Dec.], at ¶50; *see also* ¶¶52-58 (explaining how Intel's construction is incompatible with multiplication in Figure 7 embodiment).



ISOMETRIC VIEW OF FIGURE 8C ACCORDING TO INTEL'S CONSTRUCTION

Since Intel's limiting construction is not compatible with several of the embodiments disclosed in the '998 patent, including those in Figure 6, 7, and 8, it must be rejected.[9] *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1583 (Fed. Cir. 1996).

1. Intel's Construction Attempts to Import Limitations From the Specification

Intel's construction also attempts to import limitations from the specification into the claims, which is, again, a cardinal violation of claim construction. In its brief, Intel again couches its entire argument on only one of the several embodiments disclosed in the specification that use a "combined mask." Not surprisingly, it is the same embodiment described in column 14 that Intel relied upon for its construction of "parts of said first mask layer" that does not refer to any of the patent figures. Intel Br. [Doc. 110], at 27. Intel actually asks the Court to not "stretch" the scope of this claim term to cover more than this one embodiment. *Id.* But it is an axiomatic rule of claim construction that limitations from the specification are not to be read into the claims.

[9] Even though STC contends that Intel's construction attempts to exclude certain embodiments taught by the '998 patent, STC submits that it will still be able prove infringement should the Court adopt Intel's construction.

> [T[he line between construing terms and importing limitations can be discerned with reasonable certainty and predictability if the court's focus remains on understanding how a person of ordinary skill in the art would understand the claim terms. For instance, although the specification often describes very specific embodiments of the invention, we have repeatedly warned against confining the claims to those embodiments. In particular, we have expressly rejected the contention that if a patent describes only a single embodiment, the claims of the patent must be construed as being limited to that embodiment. That is not just because *section 112 of the Patent Act* requires that the claims themselves set forth the limits of the patent grant, but also because persons of ordinary skill in the art rarely would confine their definitions of terms to the exact representations depicted in the embodiments.
>
> To avoid importing limitations from the specification into the claims, it is important to keep in mind that the purposes of the specification are to teach and enable those of skill in the art to make and use the invention and to provide a best mode for doing so. One of the best ways to teach a person of ordinary skill in the art how to make and use the invention is to provide an example of how to practice the invention in a particular case. Much of the time, upon reading the specification in that context, it will become clear whether the patentee is setting out specific examples of the invention to accomplish those goals, or whether the patentee instead intends for the claims and the embodiments in the specification to be strictly coextensive. The manner in which the patentee uses a term within the specification and claims usually will make the distinction apparent.

Phillips, 415 F.3d, at 1323 (citations omitted). By asking the Court to not "stretch" the scope of this claim term beyond the embodiment disclosed in column 14, Intel is asking the Court to import those limitations into the claim. In short, limiting the claimed "combined mask" to be that of the "combined etch mask" disclosed in column 14, which, as Intel contends, requires the second layer of resist to be physically present during the transfer step, is prohibited by the precedential rules of claim construction set forth above.

2. Intel's Construction Ignores the Combination of Patterns

As with the previous term, Intel's definition focuses on the physical layers, and not the patterns that are transferred. Since Intel's construction incorporates its erroneous definition for "parts of said first mask layer," the overall construction for this term must be wrong for the same reasons as explained above.

3. Intel's Construction is Fantasy

Intel requests that the Court reject STC's construction, which is copied word for word from the specification, but adopt its litigation-motivated, made-up phraseology: "with each of the two independently shielding some part of the substrate not shielded by the other." This language is not mentioned anywhere in the claim or the specification, nor is there any equivalent teaching. STC's construction, copied verbatim from the patent, should be adopted.

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Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned certifies that on the 25th day of July, 2011 the foregoing was filed electronically through the CM/ECF system, which caused all parties or counsel to be served by electronic means.

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