

Exhibit 3

Reducing Variation in Advanced Logic Technologies, Kelin J. Kuhn, IEDM (2007)

Reducing Variation in Advanced Logic Technologies:

Approaches to Process and Design for
Manufacturability of Nanoscale CMOS

Kelin J. Kuhn

Intel Fellow

Director of Logic Device Technology

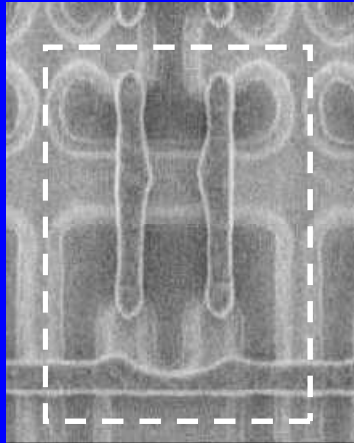
Portland Technology Development

Intel Corporation

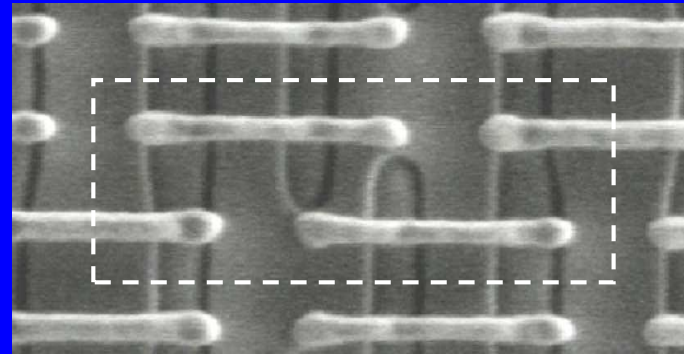
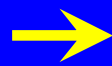
Key messages

- Process variation is not a new problem
- A variety of process, design and layout techniques can be applied to mitigate the impact of random and systematic variation
- Improvements in variation in 45nm illustrate that variation does not pose an insurmountable barrier to Moore's Law, but is simply another challenge to be overcome

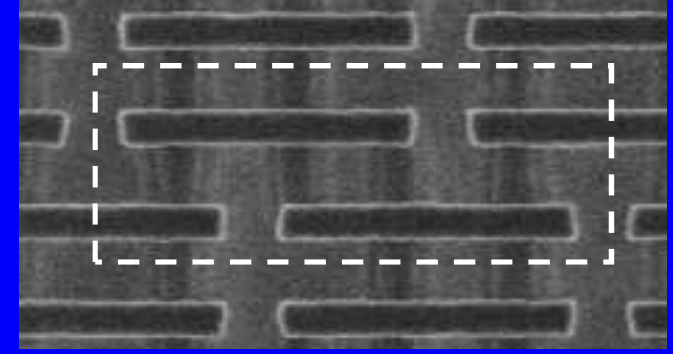
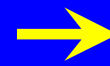
Process-Design Mitigation for Variation Management



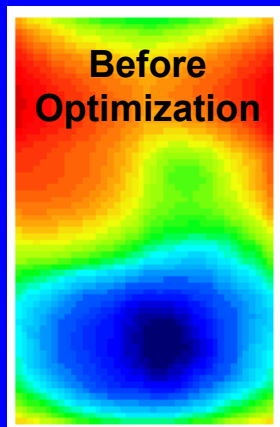
90nm – tall
 $1.0 \mu\text{m}^2$



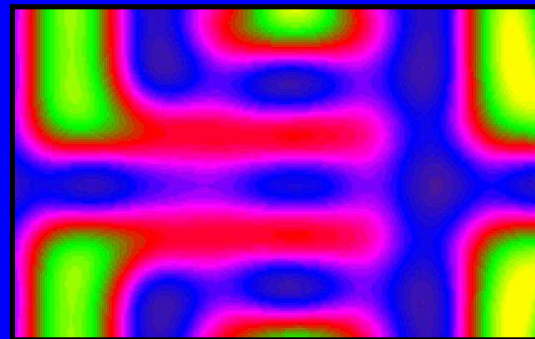
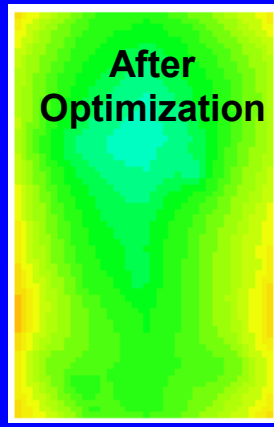
Design mitigation
65nm – wide - $0.57 \mu\text{m}^2$



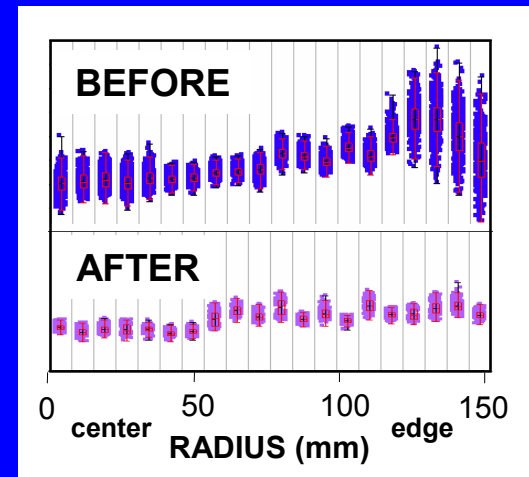
Process mitigation - 45nm – wide
w/ patterning enhancement $0.346 \mu\text{m}^2$



Design mitigation
w/ dummification

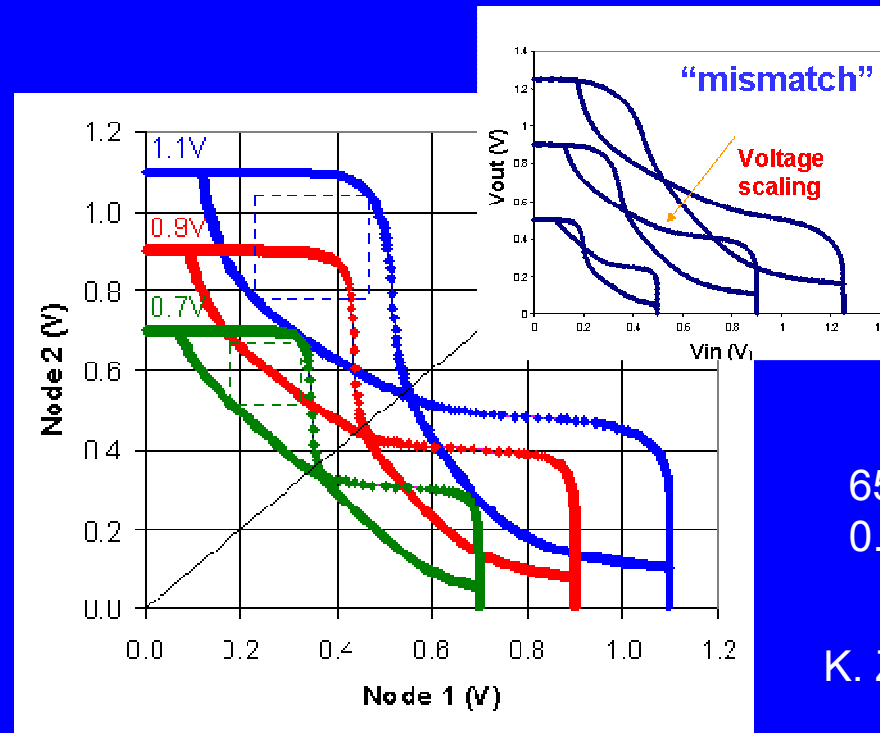


Process/design mitigation with
computational lithography



Process mitigation
w/ CMP improvements

Systematic Mismatch in the SRAM



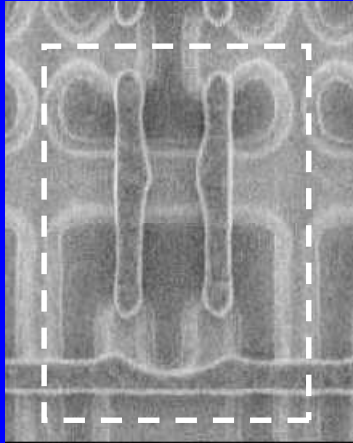
65nm – WIDE
0.57 μm^2

K. Zhang, VLSI 2004

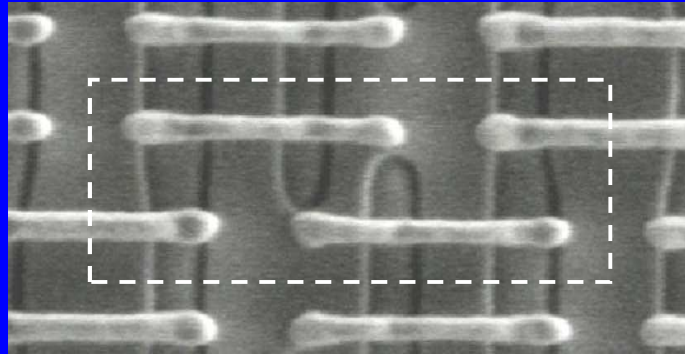
- SRAM circuits exercise the smallest area devices in the technology
- SRAM static noise margin (SNM) is sensitive to device mismatch
- Although RDF is the fundamental limit for mismatch in the SRAM a large variety of systematic issues also contribute to SRAM cell mismatch

→ These systematic issues can be mitigated with design and process changes

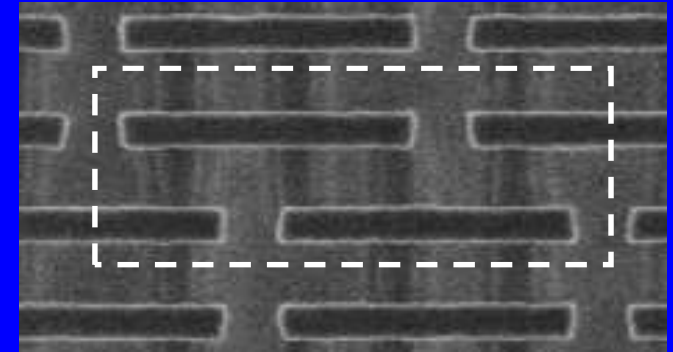
Systematic Variation Mitigation Strategies



90nm – TALL
 $1.0 \mu\text{m}^2$



65nm – WIDE
 $0.57 \mu\text{m}^2$



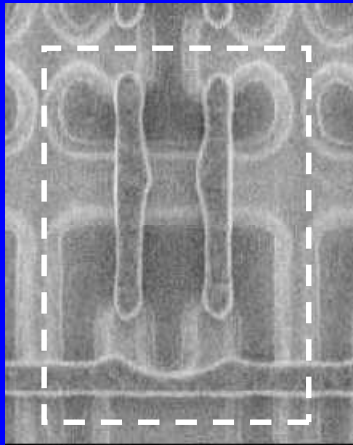
45nm – WIDE
w/ patterning enhancement $0.346 \mu\text{m}^2$

DESIGN MITIGATION

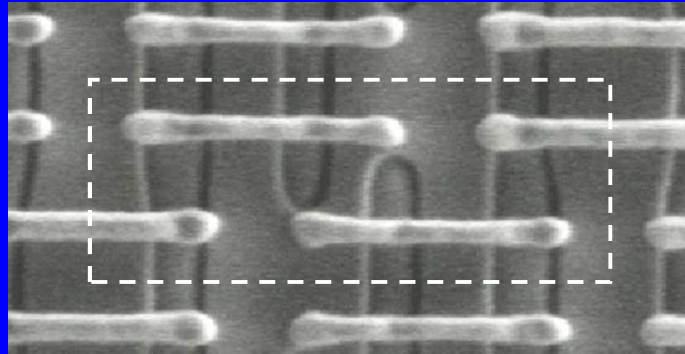
90nm to 65nm: “tall” design to a “wide” design.

- Single direction poly
- Elimination of diffusion corners
- Relaxation of patterning constraints on other critical layers

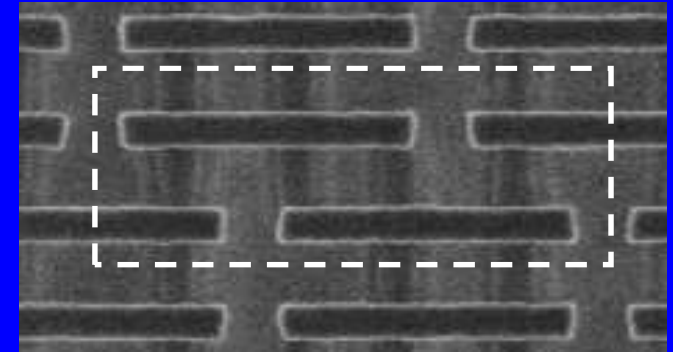
Systematic Variation Mitigation Strategies



90nm – TALL
1.0 μm^2



65nm – WIDE
0.57 μm^2



45nm – WIDE
w/ patterning enhancement 0.346 μm^2

PROCESS MITIGATION

65nm to 45nm: Patterning enhancements

- Square corners (eliminate “dogbone” and “icicle” corners)
- Improved CD uniformity across STI boundaries