Exhibit 4

Intel Takes 45nm Process to IEDM, Shows Variability Data,
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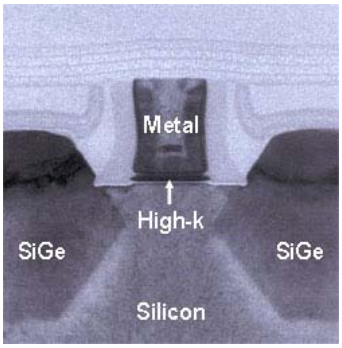
At next week's **International Electron Devices Meeting** (IEDM), held in Washington, D.C., **Intel Corp.** (Hillsboro, Ore.) researchers will discuss the **company's 45 nm gate-last process flow**, which includes trench contacts and a new level of thick "redistribution" interconnect. Intel will discuss the high-k film dimensions, but not the material compositions.

Kaizad Mistry, 45 nm program manager at Intel

"We will be describing for the first time the detailed process flow of how we create these transistors," said Kaizad Mistry, the 45 nm program manager at Intel's technology and manufacturing group.

Intel's early introduction of high-k/metal gate (HKMG) technology is, as Mistry noted, generating "a lot of buzz, but there are other aspects that tend to be overlooked."

Besides the HKMG stack, Intel's 45 nm microprocessors include lead-free packaging and a "a new type of interconnect layer, which we call a redistribution layer. It is very thick, almost a package-like trace on the die," Mistry said.



Intel's 45 nm transistor includes a high-k metal gate (HKMG) stack.

Another major change involves replacing the cylindrical contacts with a trench-style contact, which Mistry described as a long trench that can strap neighboring transistors together. "There are benefits in terms of performance and layout density. The trench contact serves as a form of what you might say is local interconnect. And in terms of patterning, it is easier to pattern lines and spaces than a field of holes."

Also, the silicon germanium regions used to create stress in the pFET transistors has been brought much closer to the channel, enhancing strain, he said.

Variability improvements

Kelin Kuhn, Intel fellow

Intel Fellow Kelin Kuhn, in an invited paper on variability, said she will present data showing that, by employing guidelines on design rules and other architectural changes, as well as process improvements, Intel has been able to keep variability in check.

Despite fears that variability challenges would derail benefits from device scaling, Kuhn said, "The key message is that as devices shrink, we can optimize layout and design styles to keep variation constant, or even improve on it."

Introduction of the HKMG gate stack itself provided some relief, she added.

Mike Mayberry, director of Intel's components research organization

Also, Mike Mayberry, director of Intel's components research organization, said the use of double patterning at one critical layer also provided variability improvement while keeping costs down by delaying the use of more expensive immersion scanners.

Speaking of Intel's ability to control variability, Kuhn said, "To be very blunt, Intel may be the only company left with integrated design and process within the same organization, which allows us to do this sort of thing. The teamwork between process and design allows us to pull off these kinds of improvements."

Kuhn said one measure of Intel's transistor variabity is gained by taking production wafers off the line and sampling ring oscillators at many points in the die. By measuring two adjacent ring oscillators, the difference is the level of variation.

In her presentation, Kuhn said she will show data over the past four technology generations, with 65 to 45 nm variability showing "significant improvement." She said, "45 is looking almost as good as 130."

By restricting design rules to keep poly lines running in a single direction and switching to a wider SRAM architecture, Intel was able to push its SRAM feature size harder, Mistry said, adding that, "Many times, these design changes are beneficial for patterning."

The use of double patterning lithography helped square off the ends of the patterns, reducing rounded ends (dogboning) and irregular shapes (icicles).

InGaAs transistors

Mayberry said Intel will report progress on building enhancement mode indium gallium arsenide (InGaAs) quantum-well transistors on a silicon substrate. The research, to be presented by Intel researcher Mantu Hudait, may be used in commercial products in the ~2015 time frame, as by then transistor scaling may require new material introductions to keep performance and power improvements on track.

The InGaAs transistor was built on a silicon substrate with a thin buffer layer about 1 µm thick and a set of transition layers. The quantum-well device had a relatively large (compared with silicon) 80 nm gate length, but a comparison with silicon devices shows a 10× reduction in power.

Mayberry said enhancement-mode devices present unique challenges, compared with depletion-mode transistors, including developing a III-IV high-k solution, which would be different from the HKMG technology used for silicon. PMOS transistors in III-V materials are difficult. And densities must be optimized to be used in volume products.

"In order to take advantage of the power and performance of these III-V materials, there are a number of things that need to be done for them to be manufacturable. The idea that size doesn't matter is nonsense. The reality is that a lot of functions depend on packing transistors into a small space," Mayberry said.

Intel is still considering whether the III-V transistors would resemble the tri-gate silicon transistors. "Whether they are exactly like a tri-gate or something different, we don't have the answer today, but we are working on it," Mayberry said.

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