STC.UNM v. Intel Corporation

Doc. 146 Att. 4

Exhibit D

Intel Corporation's Amended Responses to Plaintiff STC.UNM's First Set of Interrogatories Nos. 1-21

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UNITED STATES DISTRICT COURT

DISTRICT OF NEW MEXICO

STC.UNM, Plaintiff, v. INTEL CORPORATION, Defendant.	Civil No. 1:10-cv-01077-RB-WDS

INTEL CORPORATION'S AMENDED RESPONSES TO PLAINTIFF STC.UNM'S FIRST SET OF INTERROGATORIES NOS. 1-21

Pursuant to Rules 26 and 33 of the Federal Rules of Civil Procedure and the Local Rules of Civil Procedure of this Court, Defendant Intel Corporation ("Intel") hereby responds to Plaintiff STC.UNM's ("Plaintiff") First Set of Interrogatories Nos. 1-21 ("Interrogatories").

RESERVATION OF RIGHTS

Intel's responses to Plaintiff's Interrogatories shall not constitute an admission by Intel that any interrogatory, or the answer thereto, is admissible as evidence in any trial or other proceeding. Intel reserves the right to object on any ground, at any time, to the admission of any interrogatory, response, or document produced in connection therewith in any trial or other proceeding.

GENERAL OBJECTIONS

1. Intel objects to Plaintiff's Interrogatories to the extent they seek information protected by the attorney-client privilege, the attorney work-product doctrine, the joint-defense privilege, the common-interest privilege, and/or any other applicable doctrine of privilege or immunity.

2. Intel objects to Plaintiff's Interrogatories to the extent they seek information and/or documents subject to an obligation of confidentiality to a third party or that Intel

Subject matter disclosed in the specification of a patent, but falling outside the literal scope of the claims, is dedicated to the public. The subject matter dedicated to the public by the '998 patents includes (a) a process that otherwise satisfies the limitations of claim 6 but does not use the specified transferring steps or the specific "combined mask," and (b) a process that otherwise satisfies the limitations of claim 8 but does not involve any one of: the exposure of a periodic image with a pitch of P_{min} and a line width less than $P_{min}/2$, the formation of a periodic pattern, the transfer a periodic pattern into "said material," the specified "offsetting" step, or the interpolation of new "said pattern midway between said pattern."

Intel does not presently contend that STC's claims are barred by statutory notice requirements, intervening rights, laches, res judicata or collateral estoppel. However, discovery in the case has only just begun, and Intel reserves the right to assert such defenses at a later date.

INTERROGATORY NO. 4:

Explain in detail the factual and legal basis for any contention by Intel that the '998 patent is invalid because the purported inventions claimed therein do not satisfy the requirements of 35 U.S.C. §§ 101, 102, 103, 111, 112, or 256, or judicially created doctrines of invalidity, and the Rules and Regulations of the U.S. PTO, including, but not limited to, an identification of all prior art Intel intends to rely upon along with an element-by-element application of any alleged prior art to each claim Intel alleges is invalid. In addition, for any contention concerning §103 state what Intel contends is the applicable level of skill of one of ordinary skill in the art.

RESPONSE TO INTERROGATORY NO. 4:

Intel objects to the extent that this interrogatory seeks information protected by the attorney-client privilege or the attorney work product doctrine. Intel also objects to this interrogatory as premature because discovery has just begun. Intel objects to the extent

that this interrogatory seeks information protected by the attorney-client privilege or the attorney work product doctrine. This case is in its early stages, and Intel is just beginning to conduct its investigation into the claims and facts relating to this case and has not yet obtained necessary discovery regarding the asserted claims from STC, the named inventors and relevant third parties that would allow Intel to provide full-fledged invalidity contentions. In particular, STC has not yet provided its contentions or any other indication of claim scope that would allow Intel to provide full-fledged invalidity contentions. Subject to and without waiving its general and specific objections, Intel responds as follows:

One or more of the asserted claims of the ’998 patent are invalid under 35 U.S.C. §§ 101, 102, 103, 111, 112, 115 or 256, or judicially created doctrines of invalidity, and the Rules and Regulations of the United States Patent and Trademark Office (PTO) relating thereto.

All asserted claims of the ’998 patent are invalid for failure to comply with the requirements of 35 U.S.C. § 112 due to lack of written description, failure to particularly point out and distinctly claim the subject matter regarded as the alleged invention, and/or failure to set forth a written description sufficient to enable a person skilled in the art to make and use the alleged invention without undue experimentation.

All asserted claims of the ’998 patent are invalid under 35 U.S.C. §§ 102(f) and/or 116 because the named inventors did not invent the subject matter of the patent by themselves.

Intel attaches hereto Exhibits 1 through 6, which contain exemplary claim charts demonstrating the invalidity of the asserted claims of the ‘998 patent, specifically charting where each element of each asserted claim is found in the cited references. In an effort to focus the issues, Intel identifies only limited portions of the cited references and has not identified each and every disclosure of each element in each reference. It should be recognized that a person of ordinary skill in the art would generally read a prior art

reference as a whole and in the context of other publications, literature, and general knowledge in the field. Additionally, where Intel identifies a particular figure (or feature within a figure) in a prior art reference, the identification should be understood to encompass the figure, its caption, and the reference's description and/or explanation of the figure, including any text relating to the figure. Similarly, where Intel identifies a portion of text that refers to a figure or other material, the identification should be understood to also include the referenced figure or other material. Finally, when Intel states that a reference "discloses" a claim element, this statement is intended to mean that the reference expressly, impliedly, or inherently discloses that claim element to a person of ordinary skill in the art.

The chart below lists references that may, depending on the Court's claim construction, render one or more of the asserted claims invalid under one or more provisions of 35 U.S.C. §§ 102 and 103. References identified below as prior art to the '998 patent and published or issued more than one year before the relevant priority date may anticipate under 35 U.S.C. § 102(b). All other publications and references may anticipate under section 102(a) and/or section 102(e). To the extent any reference evidences abandonment of the '998 patent, the patent is invalid under section 102(c). Any devices or products identified as prior art may invalidate under sections 102(a), (b) and/or (g). To the extent any reference evidences invention by another, the reference may invalidate under section 102(f). Each reference or combination of references may also render the relevant claimed subject matter obvious under section 103. Intel further contends that one of ordinary skill in the art would have a reason to combine and/or modify one or more of these references to render each asserted claim obvious.

Publication No.	Author/Inventor	Title
JP-H04-071222	Jinbo et al.	Pattern Forming Method
JP-H04-127150	Okamoto	Production of Semiconductor Integrated Circuit Device, Exposing Device To be Used For This Device And Method For Inspecting Mask

Publication No.	Author/Inventor	Title
JP-H05-055102	Kosemura	Manufacture of Semiconductor Device
JP-H05-067559	Kanazawa	Formation Method of Fine Pattern
JP-H05-090121	Nakagawa	Method of Forming Resist Pattern
JP-H05-160122	Taniguchi et al.	Formation of Resist Pattern
JP-H05-165223	Ikuta	Method for Formation of Fine Resist Pattern
JP-H05-166769	Katayama et al.	Manufacture of Semiconductor Device
JP-H05-198479	Nakagawa et al.	Formation of Resist Pattern
JP-H05-297564	Uchida	Production of Phase Difference Mask
JP-H06-027635	Sugiura	Production of Photomask
JP-H06-222548	Jinbo et al.	Phase Shift Mask and Its Production
JP-H06-317704	Oguri	Formation of Diffraction Grating
JP-H06-317809	Ichimura and Nasu	Production of Thin-Film Transistor Matrix
JP-H06-318541	Kim and Han	Method for Forming Pattern
JP-H06-348032	Tanigawa et al.	Formation of Resist Pattern
JP-H07-074454	Yamaguchi and Masahiro	Manufacture of Printed Wiring Board
JP-H07-225468	Jinbo et al.	Photomask and Pattern Forming Method Using the Same
JP-H07-333396	Katakura and Norihiro	Production of Diffraction Optical Element
JP-H08-045834	Bae	Method for Forming Photoresist Pattern for Semiconductor Device
JP-H08-048037	Terui	Ink Jet Recording Head, Production Thereof and Recording Apparatus
JP-H08-051071	Neisser	Multiple Mask Method for Sharpening Selective Mask Feature
JP-H08-055920	Shirata et al.	Manufacture of Semiconductor Device
JP-H08-234017	Uemi et al.	Production of Color Filter
JP-H09-008240	Hashiguchi	Manufacture of Semiconductor Device
JP-H09-129125	Hosoya	Manufacture of Matrix Substrate Arranged with Electron Emitting Element
JP-S58-127326	Yamasaki and Maeda	Semiconductor Device Fabrication Method
JP-S62-115722	Naoki and Mitsutaka	Fine Pattern Forming Method
JP-S63-170917	Ofuji and Shiba	Fine Pattern Formation Method
JP-S63-181322	Nishimuro	Manufacture of Semiconductor Device

Publication No.	Author/Inventor	Title
JP-S63-216052	Hashimoto	Exposing Method
JP-S64-037017	Chiwata	Removal of Residual Film
JP-A-1986-100753	Takeda and Nakayama	Pattern Formation Method
JP-H01-004019	Kitagawa and Yamaguchi	Manufacturing Method of a Semiconductor Device
JP-H02-265243	Kudo et al.	Multilayer Interconnection and a Formation Method for the same
JP-H04-273245	Kirukawa and Shiroishi	An Exposure Method and Exposure Device
JP-H04-273427	Shiraishi and Hirukawa	Mask, Exposure Method and Aligner
JP-H04-355910	Shiraishi and Hirukawa	Mask and Exposure Method and Aligner
JP-H05-006857	Nagami	Formation Method of Multilayer Resist Layer
JP-H05-110006	Kaneko and Okoda	Manufacture of Semiconductor Integrated Circuit
JP-H05-205990	Watanabe	Pattern Forming Method
JP-H05-206055	Osawa	Manufacture of Semiconductor Device
JP-S61-184831	Fujiwara	Manufacturing Method of a Semiconductor Device
JP-S63-073518	Yamashita and Todokoro	Formation of Pattern
JP-S63-316055	Tsuji et al.	Manufacturing Method of a Semiconductor Device
U.S. Patent No. 36,113 (Reissue)	Brueck et al	Method for Fine-Line Interferometric Lithography
U.S. Patent No. 3,506,441	Gottfried	Double Photoresist Processing
U.S. Patent No. 3,639,185	Colom and Levine	Novel Etchant and Process for Etching Thin Metal Films
U.S. Patent No. 3,823,015	Fassett	Photo-Masking Process
U.S. Patent No. 3,918,997	Mohsen and Sequin	Method for Fabricating Uniphase Charge Coupled Device
U.S. Patent No. 3,930,857	Bendz et al.	Resist Process
U.S. Patent No. 4,155,627	Gale et al.	Color Diffractive Substractive Filter Master Recording Comprising a Plurality of Superposed Two-Level Relief Patterns on the Surface of a Substrate

Publication No.	Author/Inventor	Title
U.S. Patent No. 4,275,144	Buhl	Method of Fabricating Electrodes with Narrow Gap Therebetween
U.S. Patent No. 4,289,845	Bowden and Thompson	Fabrication Based on Radiation Sensitive Resists and Related Products
U.S. Patent No. 4,321,282	Johnson	Surface Gratings and a Method of Increasing Their Spatial Frequency
U.S. Patent No. 4,385,432	Kuo and Tsaur	Closely-Spaced Double Level Conductors for MOS Read Only
U.S. Patent No. 4,402,571	Cowan et al.	Method for Producing a Surface Relief Pattern
U.S. Patent No. 4,478,655	Nagakubo and Momose	Method for Manufacturing Semiconductor Device
U.S. Patent No. 4,496,216	Cowan	Method and Apparatus for Exposing Photosensitive Material
U.S. Patent No. 4,529,860	Robb	Plasma Etching of Organic Materials
U.S. Patent No. 4,560,435	Brown et al.	Composite Back-Etch/Lift-Off Stencil for Proximity Effect Minimization
U.S. Patent No. 4,579,812	Bower	Process for Forming Slots of Different Types in Self-Aligned Relationship Using a Latent Image Mask
U.S. Patent No. 4,591,547	Brownell	Dual Layer Positive Photoresist Process and Devices
U.S. Patent No. 4,857,481	Tam and Granick	Method of Fabricating Airbridge Metal Interconnects
U.S. Patent No. 4,859,548	Heise et al.	Method for Generating a Lattice Structure with a Phase Shift on the Surface of a Substrate
U.S. Patent No. 4,876,217	Zdebel	Method of Forming Semiconductor Structure Isolation Regions
U.S. Patent No. 4,891,094	Waldo	Method of Optimizing Photoresist Contrast
U.S. Patent No. 4,917,759	Fisher and Klein	Method for Forming Self-Aligned Vias in Multi-Level Metal Intergrated Circuits
U.S. Patent No. 5,013,680	Lowrey et al.	Process for Fabricating a DRAM Array Having Feature Widths that Transcend the Resolution Limit of Available Photolithography
U.S. Patent No. 5,017,515	Gill	Process for Minimizing Lateral Distance Between Elements in an Integrated Circuit by Using Sidewall Spacers
U.S. Patent No. 5,067,002	Zdebel et al.	Integrated Circuit Structures Having Polycrystalline Electrode Contacts

Publication No.	Author/Inventor	Title
U.S. Patent No. 5,087,584	Wada and Trudel	Process for Fabricating a Contactless Floating Gate Memory Array Utilizing Wordline Trench Vias
U.S. Patent No. 5,091,339	Carey	Trenching Techniques for Forming Vias and Channels in Multilayer Electrical Interconnects
U.S. Patent No. 5,116,718	Dalton and Micks	Contact Printing Process
U.S. Patent No. 5,126,006	Cronin et al.	Plural Level Chip Masking
U.S. Patent No. 5,126,231	Levy	Process for Multi-Layer Photoresist Etching with Minimal Feature Undercut and Unchanging Photoresist Load During Etch
U.S. Patent No. 5,158,910	Cooper et al.	Process for Forming a Contact Structure
U.S. Patent No. 5,173,442	Carey	Methods of Forming Channels and Vias in Insulating Layers
U.S. Patent No. 5,175,128	Ema et al.	Process for Fabricating an Integrated Circuit by a Repetition of Exposure of a Semiconductor Pattern
U.S. Patent No. 5,179,310	Satoh et al.	Surface-Acoustic-Waver Filter Having a Plurality of Electrodes
U.S. Patent No. 5,216,257	Brueck and Zaidi	Method and Apparatus for Alignment and Overlay of Submicron Lithographic Features
U.S. Patent No. 5,262,335	Streit et al.	Method to Produce Complementary Heterojunction Bipolar Transistors
U.S. Patent No. 5,264,076	Cuthbert and Favreau	Integrated Circuit Process Using a "Hard Mask"
U.S. Patent No. 5,264,718	Gill	EEPROM Cell Array with Tight Erase Distribution
U.S. Patent No. 5,281,550	Ducreux	Method for Etching a Deep Groove in a Silicon Substrate
U.S. Patent No. 5,298,365	Okamoto and Moriuchi	Process for Fabricating Semiconductor Integrated Circuit Device, and Exposing System and Mask Inspecting Method to be Used in the Process
U.S. Patent No. 5,308,741	Kemp	Lithographic Method Using Double Exposure Techniques, Mask Position Shifting and Light Phase Shifting
U.S. Patent No. 5,340,700	Chen and Matthews	Method for Improved Lithographic Patterning in a Semiconductor Fabrication Process
U.S. Patent No. 5,343,292	Brueck and Zaidi	Method and Apparatus for Alignment of Submicron Lithographic Features
U.S. Patent No. 5,364,495	Van Der Tol et al.	Method of Manufacturing Sharp Waveguide Branches in Integrated Optical Components

Publication No.	Author/Inventor	Title
U.S. Patent No. 5,364,716	Nakagawa et al.	Pattern Exposing Method Using Phase Shift and Mask Used Therefor
U.S. Patent No. 5,378,649	Huang	Process for Producing Non-Volatile Memory Devices Having Closely Spaced Buried Bit Lines and Non-Overlapping Code Implant Areas
U.S. Patent No. 5,401,992	Ono	High-Density Nonvolatile Semiconductor Memory
U.S. Patent No. 5,415,835	Brueck et al.	Method for Fine-Line Interferometric Lithography
U.S. Patent No. 5,424,154	Borodovsky	Lithographic Enhancement Method and Apparatus for Randomly Spaced Structures
U.S. Patent No. 5,486,449	Hosono and Takasugi	Photomask, Photoresist and Photolithography for a Monolithic IC
U.S. Patent No. 5,498,579	Borodovsky and Sarangi	Method of Producing Semiconductor Device Layer Layout
U.S. Patent No. 5,523,258	Petti et al.	Method for Avoiding Lithographic Rounding Effects for Semiconductor Fabrication
U.S. Patent No. 5,532,090	Borodovsky	Method and Apparatus for Enhanced Contact and Via Lithography
U.S. Patent No. 5,652,084	Cleeves	Method for Reduced Pitch Lithography
U.S. Patent No. 5,702,868	Kellam and Kedem	High Resolution Mask Programmable Via Selected by Low Resolution Photomasking
U.S. Patent No. 5,705,321	Brueck et al.	Method for Manufacture of Quantum Sized Periodic Structures in SI Materials
U.S. Patent No. 5,717,560	Doyle and Maloney	ESD Protection Device Using Static Capacitance Coupling Between Drain and Gate
U.S. Patent No. 5,741,625	Bae and Moon	Process for Forming Fine Patterns in a Semiconductor Device Utilizing Multiple Photosensitive Film Patterns and Organic Metal-Coupled Material
U.S. Patent No. 5,759,744	Brueck et al.	Methods and Apparatus for Lithography of Sparse Arrays of Sub-Micrometer Features
U.S. Patent No. 5,790,254	Ausschnitt	Monitoring of Minimum Features on a Substrate
U.S. Patent No. 5,801,075	Gardner et al.	Method of Forming Trench Transistor with Metal Spacers
U.S. Patent No. 5,801,821	Borodovsky	Photolithography Method Using Coherence Distance Control
U.S. Patent No. 5,834,355	Doyle	Method for Implanting Halo Structures Using Removable Spacer

Publication No.	Author/Inventor	Title
U.S. Patent No. 5,840,448	Borodovsky and Singh	Phase Shifting Mask Having a Phase Shift That Minimizes Critical Dimension Sensitivity to Manufacturing and Process Variance
U.S. Patent No. 5,858,843	Doyle and Fraser	Low Temperature Method of Forming Gate Electrode and Gate Dielectric
U.S. Patent No. 5,891,805	Cheng and Doyle	Method of Forming Contacts
U.S. Patent No. 5,933,759	Nguyen et al.	Method of Controlling Etch Bias with a Fixed Lithography Pattern for Sub-Micron Critical Dimension Shallow Trench Applications
U.S. Patent No. 5,946,079	Borodovsky	Photolithography Method Using Coherence Distance Control
U.S. Patent No. 5,949,108	Doyle	Semiconductor Device with Reduced Capacitance
U.S. Patent No. 6,021,009	Borodovsky and Troccolo	Method and Apparatus to Improve Across Field Dimensional Control In a Microlithography Tool
U.S. Patent No. 6,022,815	Doyle et al.	Method of Fabricating Next-To-Minimum-Size Transistor Gate Using Mask-Edge Gate Definition Technique
U.S. Patent No. 6,042,998	Brueck and Zaidi	Method and Apparatus for Extending Spatial Frequencies in Photolithography Images
U.S. Patent No. 6,054,370	Doyle	Method of Delaminating a Pre-Fabricated Transistor Layer From a Substrate for Placement on Another Wafer
U.S. Patent No. 6,063,688	Doyle and Cheng	Fabrication of Deep Submicron Structures and Quantum Wire Transistors Using Hard-Mask Transistor Width Definition
U.S. Patent No. 6,069,739	Borodovsky and Krautschik	Method and Lens Arrangement to Improve Imaging Performance of Microlithography Exposure Tool
U.S. Patent No. 6,103,429	Doyle et al.	Technique For Fabricating Phase Shift Masks Using Self-Aligned Spacer Formation
U.S. Patent No. 6,124,185	Doyle	Method for Producing a Semiconductor Device Using Delamination
U.S. Patent No. 6,153,342	Doyle and Schenker	Selective Spacer Methodology for Fabricating Phase Shift Masks
U.S. Patent No. 6,153,357	Okamoto and Moriuchi	Process for Fabricating Semiconductor Integrated Circuit Device, and Exposing System and Mask Inspecting Method to be Used in the Process
U.S. Patent No. 6,162,696	Cheng and Doyle	Method of Fabricating a Feature in an Integrated Circuit Using a Two Mask Process with a Single Edge Definition Layer

Publication No.	Author/Inventor	Title
U.S. Patent No. 6,172,409	Zhou	Buffer Grated Structure for Metrology Mark and Method for Making the Same
U.S. Patent No. 6,187,694	Cheng and Doyle	Method of Fabricating a Feature in an Integrated Circuit Using Two Edge Definition Layers and a Spacer
U.S. Patent No. 6,204,103	Bai and Doyle	Process to Make Complementary Silicide Metal Gates for CMOS Technology
U.S. Patent No. 6,222,254	Liang and Doyle	Thermal Conducting Trench in a Semiconductor Structure and Method for Forming the Same
U.S. Patent No. 6,233,044	Brueck et al.	Methods and Apparatus for Integrating Optical and Inteferometric Lithography to Produce Complex Patterns
U.S. Patent No. 6,423,614	Doyle	Method of Delaminating a Thin Film Using Non-Thermal Techniques
U.S. Patent No. 6,528,856	Bai et al.	High Dielectric Constant Metal Oxide Gate Dielectrics
U.S. Patent No. 6,534,837	Bai and Doyle	Semiconductor Device
U.S. Patent No. 6,570,220	Doyle and Cheng	Fabrication of Deep Submicron Structures and Quantum Wire Transistors Using Hard-Mask Transistor Width Definition
U.S. Patent No. 6,596,609	Cheng and Doyle	Method of Fabricating a Feature in an Integrated Circuit Using Two Edge Definition Layers and a Spacer
IEEE, Symposium on VLSI Technology Digest of Technical Papers, 1992, at 112-13	H. Jinbo & Y. Yamashita	Application of Blind Method to Phase-Shifting Lithography
Microelectronic Engineering, Vol. 3, 1985, at 443-50	A.G. Brown et al.	A Direct-Write Electron Beam Lithographic Process Using Multi-Layer Resists and Its Application to Silicon-On-Sapphire Technology
SPIE Optical Microlithography III: Technology for the Next Decade, Vol. 470, 1984, at 111-121	Robert R. Allen et al.	Implementation of Automatic Alignment Utilizing Electrical Wafer Probe Techniques
Microelectronic Engineering, Vol. 6, 1987, at 407-12	Hiroyuki Hiraoka	Resist Image Enhancement By UV-, Soft Vacuum Pulsed Electron Beams and Organometallic Compounds
AIChE Journal, Vol. 37, No. 12, Dec. 1991, at 1863-74	David H. Ziger & Chris A. Mack	Generalized Approach Toward Modeling Resist Performance

Publication No.	Author/Inventor	Title
IBM Technical Disclosure Bulletin, Aug. 1990, at 62-63	S. Kaszuba et al.	Complementary Selective Writing by Direct-Write E-Beam/Optical Lithography Using Mixed Positive and Negative Resist
CLEO'96, at 390-91	Xiaolan Chen et al.	Multiple Exposure Interfeometric Lithography- A Novel Approach to Nanometer Structures
IEDM 96, at 61-64	Shuji Nakao et al.	0.12 um Hole Pattern Formation by KrF Lithography for Giga Bit DRAM
Integrated Circuit Fabrication Technology, at 85-107, 274-328 (McGraw-Hill, 2d ed. 1989)	David J. Elliott	Chapter 3: Resist Classification
IEEE International Electron Devices Meeting, 1990, at. 825-28, 986	H. Jinbo & Y. Yamashita	0.2 mum or less i-line lithography by phase-shifting-mask technology
Journal of Vacuum Science & Technology B 14(5), Sept/Oct. 1996, at 3339-49	Xiaolan Chen et al.	Interferometric Lithography of Sub-micrometer Sparse Hole Arrays for Field-Emission Display Applications
Journal of Vacuum Science & Technology B 10(6), Nov/Dec. 1992, at 3243-47	Yong Chen et al.	Application of an X-Ray Stepper for Subquarter Micrometer Fabrication
Journal of Vacuum Science & Technology B 11(3), May/June 1993, at 658-66	Saleem H. Zaidi & S.R.J. Brueck	Multiple-Exposure Interfeometric Lithography
SPIE Vol. 2197, at 869-75	Saleem H. Zaidi & S.R.J. Brueck	Multiple-Exposure Interferometric Lithography
Journal of Vacuum Science & Technology B 12(6), Nov/Dec. 1994, at 3600-06	S. Sohail et al.	Diffractive Techniques for Lithographic Process Monitoring and Control
IBM Technical Disclosure Bulletin, Jan. 1990, at 218-19	J.E. Cronin & H.S. Landis	Method to Incorporate Three Sets Pattern Information in Two Photo-Steps
Japanese Journal of Applied Physics, Vol. 31, Dec. 1992, at 4520-24	F. Rousseaux et al.	Recent Developments for Sub-Quarter Micrometer Fabrication

Publication No.	Author/Inventor	Title
Japanese Journal of Applied Physics, Vol. 33, Dec. 1994, at 6923-27	Yong Chen et al.	Improvements of Nanostructure Patterning in X-Ray Mask Making
IBM Technical Disclosure Bulletin, May 1993, at 51-54	Y. Dove & D.B. Kuo	Method for the Fabrication of a Micro-Lithography Mask Incorporating Phase Shifting and Light Absorption Regions
IBM Technical Disclosure Bulletin, May 1984, at 6413-15	Q.K. Rottmann & H.R. Yuan	Method for Lithographic Tool and Process Characterization
Microelectronic Engineering, Vol. 13, 1991, at 357-60	W. Zapka et al.	Mix-and-Match EBP/Optical Lithography of 1MBit Chips
Microelectronic Engineering, Vol. 17, 1992, at 295-98	B. Martin	Bi-Layer Resist Process for Sub-Micron Optical Lithography Using Silicon Containing Resist
Microelectronic Engineering, Vol. 21, 1993, at 29-32	G. Amblard et al.	Advanced i-line Lithography: Processes for Positive and Negative Patterning Using the Same Acid Hardening Resist
Microelectronic Engineering, Vol. 30, 1996, at 235-38	A. Schmidt et al.	Aligned Double Exposure in Deep X-ray Lithography
Microelectronic Engineering, Vol. 6, 1987, at 473-78	H. Willis et al.	A Comparison of Electron Sensitive Single, Bi-, and Tri-Level Resist Schemes for the Fabrication of Sub-Micron Gate Structures in Doped Polysilicon
Microelectronic Engineering, Vol. 6, 1987, at 393-98	Kevin J. Orvek et al.	An Organosilicon Photoresist for Use in Excimer Laser Lithography
Microelectronic Engineering, Vol. 9, 1989, at 225-29	A.G. Brown et al.	A Direct-Write Electron Beam Lithographic Technique for the Fabrication of CMOS-SOS Devices with Sub-Micron Gate Dimensions
Microlithography Process Technology for IC Fabrication, at 138-63 (McGraw-Hill, 1986)	David J. Elliott	8. Multiple Layering of Films (Resist, Oxidize, Other) to Serve as Diffusers, Absorbers, or Collimators of Incident Exposure Energy
Polymer, Vol. 28, Sept. 1987, at 1619-26	R. Jones et al.	Electron-Beam Resists from Langmuir-Blodgett Films of Poly(styrene/maleic anhydride) Derivatives
IBM Technical Disclosure Bulletin, Sept. 1990, at 227-32	N. Dally et al.	Sub-Micron Channel Length CMOS Technology
Solid State Technology, Aug. 1985, at 130-35	E. Reichmanis et al.	Approaches to Resist for Two-Level RIE Pattern Transfer Applications

Publication No.	Author/Inventor	Title
SPIE Electron-Beam, X-Ray, and Ion-Beam Technology: Submicrometer Lithographies IX, Vol. 1263, 1990, at 282-96	S. Tedesco et al.	PRIME Process: An Alternative to Multiple Layer Resist Systems and High Accelerating Voltage for E-beam Lithography
SPIE X-Ray/EUV Optics for Astronomy, Microscopy, Polarimetry, and Projection Lithography Vol. 1343, 1990, at 245-55	Saleem H. Zaidi et al.	Submicrometer Lithographic Alignment and Overlay Strategies
SPIE Advances in Resist Technology and Processing IX, Vol. 1672, 1992, at 74-93	P. Trefonas & M.T. Allen	Acid Diffusion, Standing Waves and Information Theory: A Molecular Scale Model of Chemically Amplified Resist
SPIE Optical/Laser Microlithography V, Vol. 1674, 1992, at 776-82	En S. Wu et al.	Two-Photon Lithography for Microelectronic Application
SPIE Holographics International '92, Vol. 1732, at 172-83	István Bányász	Resolution and Field Range Limitations in Holography Imposed by Film MTF and Nonlinearity
SPIE Vol. 2438, at 486-95	John M. Hutchinson et al.	Characterization and Modeling of a Chemically Amplified Resist for ArF Lithography
SPIE Vol. 2440, at 290-301	Yao-Ting Wang et al.	Automated Design of Halftoned Double-Exposure Phase-Shifting Masks
SPIE Vol. 2440, at 435-47	Edward W. Charrier & Chris A. Mack	Yield Modeling and Enhancement for Optical Lithography
SPIE Vol. 2440, at 816-26	Akihiro Otaka et al.	A New Spatial Frequency Doubling Method for Sub-0.15- um Optical Lithography
SPIE Vol. 2726, at 734-53	Martin van den Brink et al.	Step-And-Scan and Step-And-Repeat, A Technology Comparison
SPIE Semiconductor Microlithography VI, Vol. 275, 1981, at 156-63	Peter S. Gwozdz	Positive Versus Negative: A Photoresist Analysis
SPIE Vol. 2776, at 300-09	Philippe Lalanne & G. Michael Morris	Design, Fabrication and Characterization of Subwavelength Periodic Structures for Semiconductor Anti-Reflection Coating in the Visible Domain
SPIE Vol. 3011, at 194-99	Gaylord E. Moss	Method for Making Balanced Multiple Exposures in Single Layer Holograms

Publication No.	Author/Inventor	Title
SPIE Vol. 3051, at 342-51	Koji Matsuoka & Akio Misaka	Application of Alternating Phase-Shifting Mask to 0.16 um CMOS Logic Gate Patterns
SPIE Vol. 3051, at 85-93	Hiroshi Ooki et al.	Experimental Study on Non-Linear Multiple Exposure Method
VLSI Technology Digest of Technical Papers, 1993, at 65-66	M. Helm et al.	A Low Cost, Microprocessor Compatible, 18.4 um^2, 6-T Bulk Cell Technology for High Speed SRAMS

The list of references above is based on possible claim construction positions that STC may take. By contending that the asserted claims are invalid under possible claim constructions by STC, Intel in no way concedes that those constructions are appropriate, and Intel offers this response without any prejudice to any position it may ultimately take as to any claim construction issues. More generally, the claim construction process in this case has not begun, and Intel reserves its right to modify, amend, or supplement its response based on STC's proposed claim constructions, infringement contentions, production of documents, other evidence, deposition testimony, newly discovered prior art, the outcome of claim construction proceedings, or anything else that sheds light on the meaning, scope, or validity of the asserted claims, or otherwise affects Intel's contentions in this investigation.

Prior art not included in this response, whether known or not known to Intel, may become relevant. In particular, Intel is currently unaware of the extent to which STC will contend that limitations of the asserted claims are not disclosed in the prior art identified herein. To the extent that such an issue arises, Intel reserves the right to identify additional teachings in the same references or in other references that anticipate or would have made the addition of the allegedly missing limitation obvious. Moreover, Intel has subpoenaed a number of third parties believed to have information relevant to this response. Intel expressly reserves the right to amend, supplement, or modify this response as additional information is obtained from third parties.