Exhibit 11

Smith Deposition Exh. 9

United States Patent [19]

Zdebel et al.

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[54] **INTEGRATED CIRCUIT STRUCTURES HAVING POLYCRYSTALLINE ELECTRODE CONTACTS**

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Related U.S. Application Data

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[52] U.S. Cl. **357/59**; 357/234; 357/44; 357/45; 357/46; 357/34

[58] Field of Search ..... 357/23.4, 44, 45, 46, 357/34, 59 H, 59 G

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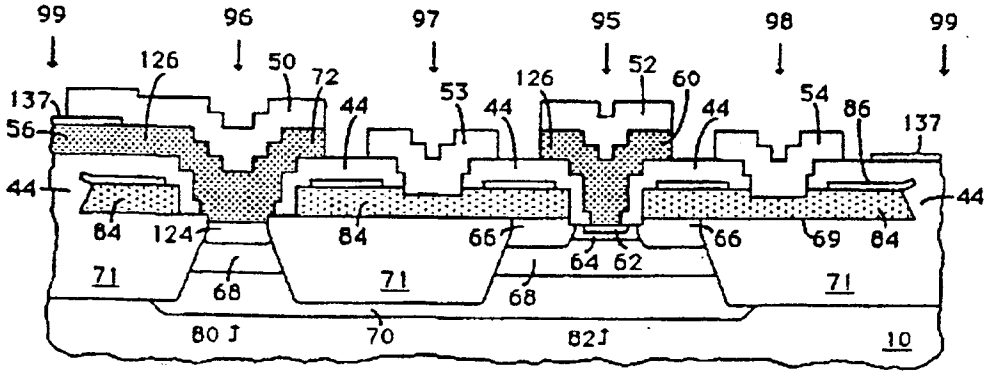
[57] **ABSTRACT**

A process is disclosed for fabricating improved integrated circuit devices. In accordance with one embodiment of the invention integrated devices are fabricated by a process which produces small device areas without relying upon restrictive photolithography tolerances. The process uses four polycrystalline silicon layers to fabricate and contact the device regions, to achieve a relatively planar structure, and to reduce the size of device regions below normal photolithographic tolerances. The process uses a master mask to define the basic footprint of the device in combination with easy to align block-out masks in each lithography step. Means and methods for many types of devices such as complementary lateral and vertical bipolar transistors, JFETs, Sits, MOSFETs, resistors, diodes, capacitors and other devices which can be simultaneously fabricated are also described.

20 Claims, 46 Drawing Sheets



92 = Photoresist

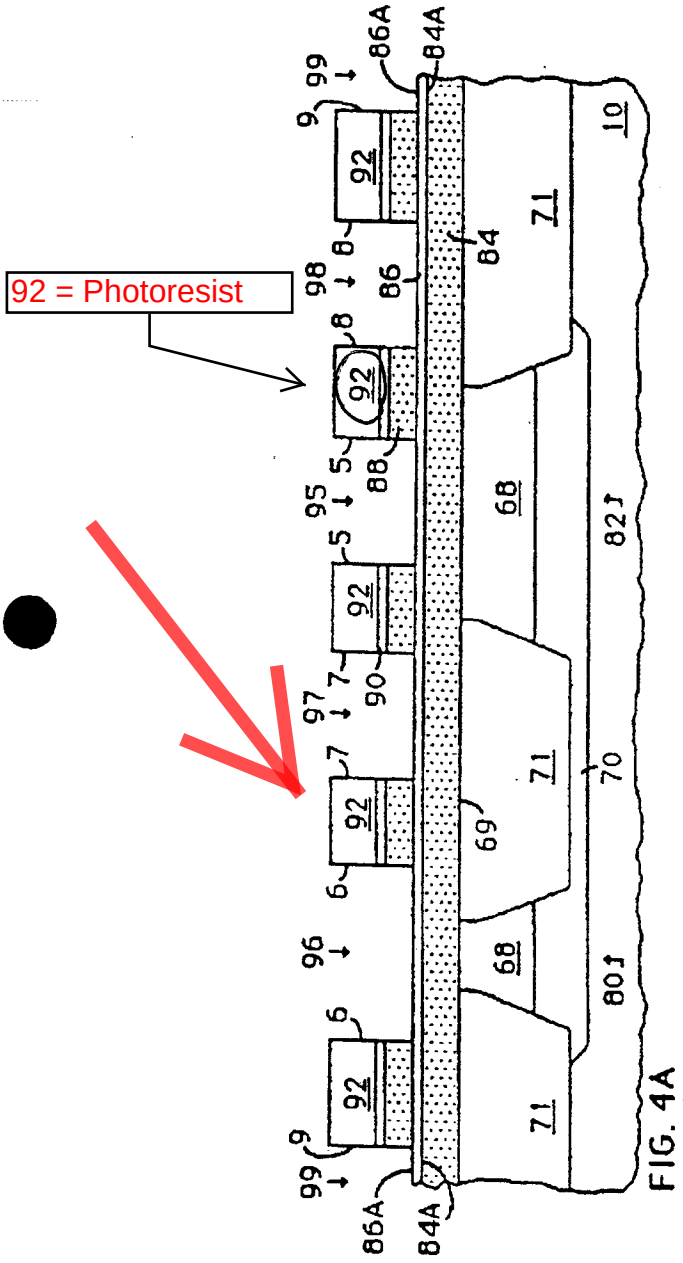


FIG. 4A

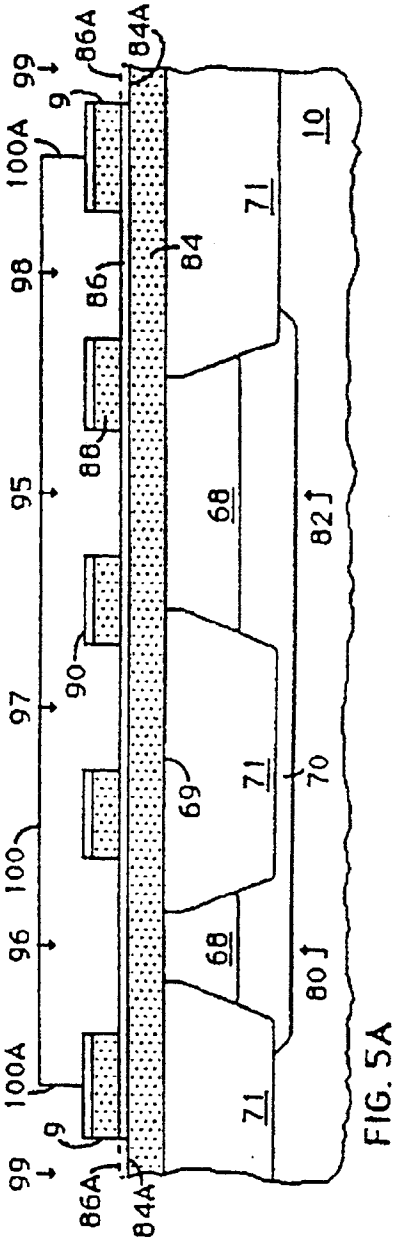


FIG. 5A

the oxidation mask. This portion of the process is well known in the art. Any convenient method of producing isolation walls may be used.

Epi-islands 80 and 82 or equivalent may be used for a variety of device regions besides the collector region and emitter/base regions of the NPN transistor being described here. Examples of the use of such epi-islands for other device regions will be provided later and those of skill in the art will appreciate that the description herein is by way of example and not intended to be limiting.

The surface of epi-region 68 is cleaned to avoid the formation of undesirable interfacial oxide between the epi-layer and layer 84 of polycrystalline semiconductor which will be subsequently deposited. Following cleaning, a series of layers are deposited on surface 69 of epi-region 68 and oxide region 71, as illustrated in FIG. 3. FIG. 3 shows a schematic cross-section corresponding to FIGS. 2, but at an earlier stage of fabrication.

Two layers 84, 86 are conveniently deposited on surface 69 using low pressure chemical vapor deposition (LPCVD). First layer 84 is a layer of polycrystalline semiconductor, preferably silicon having a thickness conveniently of about 385 nanometers. Larger or smaller thicknesses may be used for layer 84 according to relationships with other layers which will be subsequently explained. Second layer 86 is conveniently a layer of silicon nitride or a sandwich of oxide plus nitride or a layer of other oxidation resistant material having a thickness of, for example, about 70–120 nanometers. Poly silicon layer 84 will be used to form poly silicon base contact regions 84 of FIG. 2. Where an NPN transistor is being formed, layer 84 is doped by ion implantation of, for example, boron. The doping may be performed during or anytime after deposition of layer 84, but is conveniently performed after deposition of layers 84 and 86 through nitride layer 86 and before deposition of layers 88 or 90. Poly silicon layer 84 is conveniently doped with singly ionized boron at an energy of about 70 KeV to a dose of about 1×10^{16} cm^{-2}, although other doping levels may also be used depending on the desired device and circuit characteristics. The implantation is preferably arranged so that the relatively high dose of boron is located near the upper surface of polycrystalline silicon layer 84, just below silicon nitride 86.

After the boron implantation, two further layers 88, 90 are deposited, for example by LPCVD, over silicon nitride layer 86. Layer 88 is desirably an undoped layer of polycrystalline silicon having a thickness conveniently of about 180 nanometers. Larger or smaller thicknesses may be used for layer 88, taking into account the thickness of other layers, as will be subsequently explained. Layer 90 is formed overlying poly layer 88. Layer 90 conveniently prevents contamination of poly layer 88 and serves as a hard mask for subsequent lithographic patterning of the underlying layers. Layer 90 may be of any material suitable for such purposes. Layer 90 is conveniently of silicon oxide having a thickness of about 20–40 nanometers.

Processing of the structure continues with the application of layer 92 of photoresist overlying oxide layer 90 as shown schematically in FIG. 4A. The photoresist is patterned using master mask 94, represented by the shaded region in FIG. 4B, containing images 95-99 for locating various device regions. Master mask 94 provides self-alignment of the critical device areas, for example in the case of the vertical NPN transistor, the collector contact, the base contact or contacts, the emitter contact, and the emitter-base active region. In accordance with one embodiment of the invention, master mask 94 defines the master electrode area which includes emitter contact opening 95, collector contact opening 96, and base contact openings 97, 98 located within perimeter 9 and surrounded by external region 99. Region 99 identifies the region, outside perimeter 9 of master mask 94. Openings or windows 95–98 located within perimeters 5–8 respectively are used in the subsequent process to form the "footprints" of the device terminals, and in the case of the vertical bipolar device, the active emitter-base region. Perimeter 5, although referred to generally herein as the emitter opening or emitter contact opening, is used in conjunction with epitaxial island 82 formed within field oxide 71 to locate both the base and emitter of the device as well as the emitter contact. Variations and further embodiments, in addition to the basic NPN transistor, are discussed later. Base contact openings 97, 98 are located within perimeters 7, 8 respectively. Collector contact opening 96 is located within perimeter 6.

Master mask 94 is aligned to epi-islands 80, 82 as shown in FIG. 4B. In a preferred embodiment, the minimum geometry of any feature included in the master mask is a dimension, such as for example, about 1.5 micrometers, which can be processed easily with standard photolithography alignment tools. As will become apparent, fine geometry devices having features less than the minimum geometry size can be readily produced by the inventive process and structure without resorting to more difficult photolithography. The process may be readily scaled to smaller dimensions as lithographic and process resolution improve.

A particular feature of the present invention is that the master mask automatically self-aligns the emitter, base, and collector contacts and outer device periphery, so that, when metal is subsequently applied thereto, only one alignment tolerance (master mask to metal mask) need be accommodated. This allows devices having smaller metal pitch and therefore smaller overall size to be constructed as compared to the prior art processes which do not provide such self-alignment of the emitter, base, and collector contacts and the device periphery. As will be subsequently explained, other device types may be built on the same substrate using the same basic process sequence described herein, and they will also have the same minimum pitch advantage. As will be further explained, part of the self-alignment feature may be sacrificed to gain other advantages. These trade-offs are particularly noted.

Using master mask 94 to expose photoresist layer 92, the process continues by defining master mask pattern 94 in photoresist layer 92 and subsequently in layers 90 and 88, as illustrated schematically in FIG. 4A.

Photoresist is an organic material and has a potential for contaminating other parts of the process. Accordingly, in a preferred process the resist is used only to pattern layer 90 and then is removed. When layer 90 is of oxide it is conveniently patterned using wet chemical etchants such as a 10:1 solution of ammonium fluoride and hydrofluoric acid or by reactive ion etching. Other etching means well known in the art may also be used. For further etching it is desirable to use a differential etching process which attacks polysilicon layer 88 more rapidly than mask layer 90 or underlying nitride layer 86. Polysilicon layer 88 is subsequently patterned by reactive ion etching or other suitable differential etch-