# Exhibit 13

Smith Deposition Exh. 11

US006022815A

# United States Patent [19]

Doyle et al.

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[54] **METHOD OF FABRICATING NEXT-TO-MINIMUM-SIZE TRANSISTOR GATE USING MASK-EDGE GATE DEFINITION TECHNIQUE**

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[51] **Int. Cl.**[7] ..... **H01L 21/3205**

[52] **U.S. Cl.** ..... **438/947**; 438/286; 438/585

[58] **Field of Search** ..... 438/947, 596, 438/587, 585, 286

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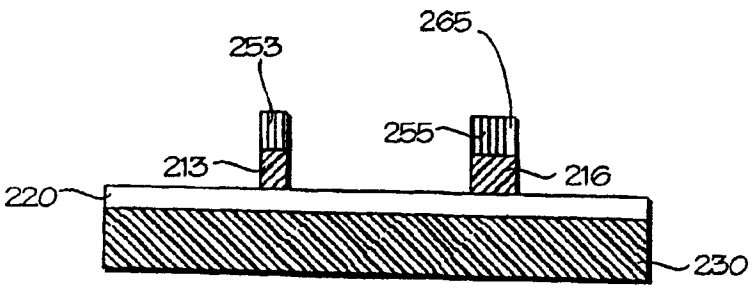
[57] **ABSTRACT**

A method of fabricating minimum size and next-to-minimum size electrically conductive members using a litho-less process is disclosed. A substrate is provided, and a layer of gate dielectric material is formed on the substrate. A layer of electrically conductive material is formed over the gate dielectric material. A first mask is used to form a hard mask. A layer of first spacer material is deposited over the existing structures, and the layer of first spacer material is etched back to form spacers adjacent to the hard mask. The width of the first spacers determines the minimum size gate length. A layer of second spacer material is deposited over the existing structures, including the hard mask and first spacers. The layer of second spacer material is etched back to form a second set of spacers adjacent to the first spacers. The width of the first and second spacers together determine the next-to-minimum size gate length. A second mask is used to protect the portion of the second spacers which are to be used to define next-to-minimum size gates, and the unprotected second spacers and the hard mask are removed. The exposed electrically conductive material is removed. The remaining spacers are then removed, leaving minimum size and next-to-minimum size gates.

**13 Claims, 12 Drawing Sheets**




Cross-sectional view

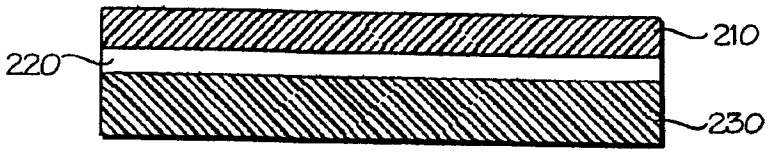



Fig. 2a

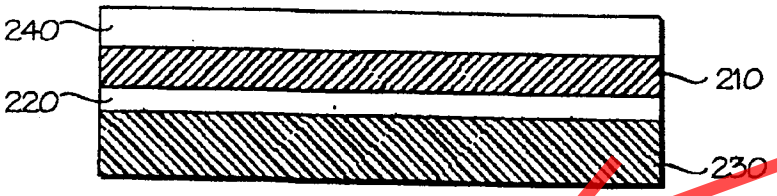
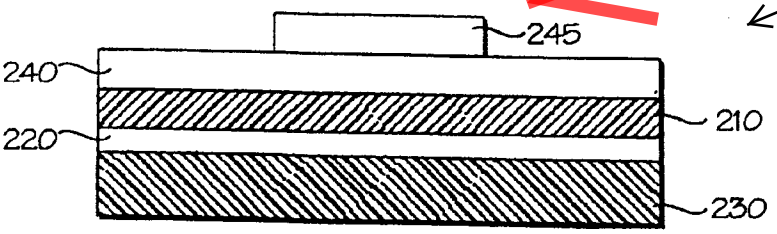



Fig. 2b




245 = Photomask

Fig. 2c

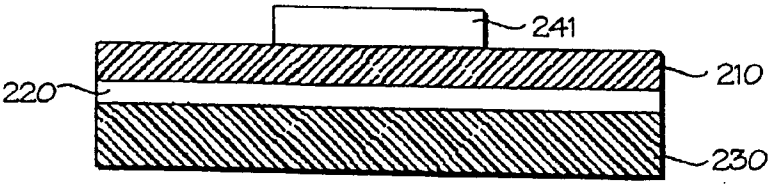



Fig. 2d

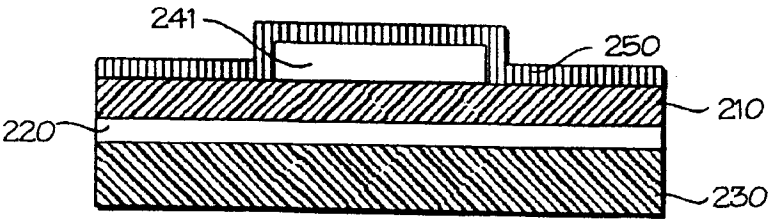



Fig. 2e

gate implemented in accordance with the teachings of the present invention. FIG. 2*a* shows a substrate **230**. In this example, the substrate **230** comprises silicon. Silicon formed on other substrates such as silicon oxide, aluminum oxide, or glass, on which integrated circuits can be built, can be used. A layer of gate dielectric **220**, comprising, for example, silicon dioxide, is formed on the substrate **230**. Examples of other possible gate dielectric materials are lead strontium, barium strontium, aluminum oxide, and tantalum pentoxide. A layer of nitrided oxide may also be used. The gate dielectric layer is preferably deposited to a thickness of between 20–50 angstroms (Å). A layer of electrically conductive material **210** is formed on the gate dielectric **220**. In this example, the electrically conductive material **210** comprises polysilicon. The layer of polysilicon is preferably formed by a blanket deposition (that is, uniformly covering all surfaces) to the thickness of between 1000–3500 Å.

In FIG. 2*b*, a layer of hard mask material **240** is formed over the polysilicon. The preferred hard mask material in this example is silicon dioxide, formed by blanket deposition to the preferred thickness of 1800 Å. Other thicknesses are possible. The hard mask material **240** can be any material that can withstand high temperature processing and can be etched.

The hard mask **240** is typically patterned using a known photoresist lithography and plasma etching process, using the first mask. FIG. 2*c* depicts a photoresist mask **245**. The photoresist mask **245** is used to form a hard mask **241**, as shown in FIG. 2*d*. It is on the sidewalls of the hard mask **241** that the future gate hard mask will be formed, as discussed below. Therefore, it is the patterning of the hard mask material **240** that defines the location of the future gate structures.

Next, a layer of spacer material **250** is formed, as shown in FIG. 2*e*. The spacer material **250** is selected to be one that can withstand high temperature processing and can be etched, but is also different from the hard mask material **241**. The spacer material **250** being different from the hard mask material **241** allows for selective etching of the hard mask material **241** without also etching the spacer material **250**. The preferred spacer material **250** in this instance is silicon nitride. The silicon nitride **250** is blanket deposited, preferably using chemical vapor deposition. The silicon nitride **250** is deposited conformally so that the deposited silicon nitride **250** follows the shape of the hard mask material. The thickness of the deposited silicon nitride **250** will determine the length of the minimum size gate. Preferably, the thickness of the deposited silicon nitride **250** is 1000 Å or more. Smaller thicknesses are also possible.

After the deposition of the spacer material **250**, the spacer material is **250** anisotropically etched. The etching is preferably accomplished using a reactive ion etching (RIE) process. By etching anisotropically, the spacer material will be completely removed from the horizontal surfaces and a portion adjacent to each vertical edge of the hard mask **241** will remain to create spacers **253** and **255**, as shown in FIG. 2*f*-1. FIG. 2*f*-2 shows a top view illustrating the hard mask **241** located between nitride spacers **253** and **255**, the remainder of the hard mask **242**, the remaining nitride **250**, and the underlying polysilicon layer **210**. The gate dielectric layer and the silicon substrate are hidden by the polysilicon layer **210**.

FIG. 2*g* shows that a second layer of spacer material **260** is formed over the existing structures, including the polysilicon layer **210**, the spacers **253** and **255**, and the hard mask **241**. The preferred material for the second layer of spacer material **260** is silicon dioxide. The selection of silicon dioxide for the second spacer material **260** as well as the hard mask **241** allows the removal of the hard mask **241** and the unwanted portions of the second spacer material **260** to be removed in a single step. The silicon dioxide **260** is blanket deposited, preferably using chemical vapor deposition. The silicon dioxide **260** is deposited conformally so that the deposited silicon dioxide **260** follows the shape of the hard mask material **241** and the nitride spacers **253** and **255**. The thickness of the deposited silicon dioxide **260** plus the thickness of the nitride spacers **253** and **255** will determine the length of the next-to-minimum size gate. Preferably, the thickness of the deposited silicon dioxide is between 10–20% of the thickness of the nitride spacers **253** and **255**, or in other words, between 100–200 Å or larger. However, smaller thicknesses are also possible.

The second layer of spacer material **260** is anisotropically etched back to form spacers **263** and **265**, as depicted in FIG. 2*h*-1 and FIG. 2*h*-2. If the preferred material of silicon oxide is used for the second spacer material, then a RIE process is preferred to form spacers **263** and **265**. RIE etching of silicon oxide over silicon layers results in a selectivity ratio of 35:1 where plasma-only etching provides a selectivity ratio of 10:1. Selectivity relates to the preservation of the underlying surface during etching. A high selectivity ratio indicates little or no attack of the underlying surface.

The next step of the present example involves the second mask **290**, as shown in FIG. 2*i*-1 and FIG. 2*i*-2. The second mask is shown in a transparent manner in FIG. 2*j*-2 in order to reveal the underlying structures. The second mask is used to protect spacer **265** while the hard mask **241** and spacer **263** are removed. The second mask must be aligned with the spacer **255**. Note that the second mask also protects the portion of the hard mask that covers the polysilicon contact area **242**. The unprotected silicon dioxide, including portions of the hard mask **241** and the spacer **263**, are removed. Because the first spacer material is chosen to be different from the hard mask material and the second spacer material is chosen to be the same as the hard mask material, the hard mask **241** and spacer **263** can be selectively removed in a single step. The resulting intermediate structure is shown in FIG. 2*j*-1 and FIG. 2*j*-2. Spacer **253** will serve as a hard mask for a minimum size gate and spacers **255** and **265** will serve as a hard mask for a next-to-minimum size gate.

Next, again using the second mask **290**, unmasked portions of the polysilicon layer **210** are removed, leaving polysilicon blocks **213** and **215**, as shown in FIG. 2*k*-i and FIG. 2*k*-2. Polysilicon block **213** is not visible in FIG. 2*k*-2 because it is hidden by spacer **253**. Removing the unmasked portions of the polysilicon layer **210** reveals the gate dielectric **220**.

The second mask **290** is subsequently removed and polysilicon block **215** is reduced to what will be the next-to-minimum size transistor gate **216**, as shown in FIG. 2*l*-1. Although two steps for removing the polysilicon have been described, an alternative implementation is possible whereby all of the polysilicon layer **210** not covered by spacer material or hard mask material is removed in a single step following the removal of the second mask **290**.

FIG. 2*l*-2 shows that all of the exposed polysilicon has been removed. The only polysilicon remaining is located beneath the nitride spacer material **250**, beneath the silicon dioxide spacer material **265**, and beneath the remaining silicon dioxide hard mask **242**.

FIG. 2*l*-1 clearly shows that the thickness of the spacers **253**, **255**, and **265** determine the length of the polysilicon