Exhibit 3

STC.UNM v. Intel

Invalidity Claim Chart Comparing '998 Patent to Petti '258

The following asserted claims of STC.UNM's U.S. Pat. No. 6,042,998 are invalidated pursuant to 35 U.S.C. § 102 and/or § 103, alone or in combination with other references, by the prior art reference U.S. Pat. No. 5,523,258 to Petti et al., entitled "Method for Avoiding Lithographic Rounding Effects for Semiconductor Fabrication," filed Apr. 29, 1994 and issued June 4, 1996 ("Petti '258"). These preliminary invalidity contentions are based on information currently known to Intel, and, as a result, apply interpretations apparently or potentially adopted by STC.UNM. Intel reserves the right to amend its preliminary invalidity contentions in light of developments in the case such as production of discovery, identification of additional prior art, and issuance of an order following any Claim Construction Hearing, as stated in the Scheduling Order (Dkt. 47, dated March 2, 2011).

Asserted Claims of '998 Patent	Petti '258
6. A method for obtaining a pattern wherein the Fourier transform of said pattern contains high spatial frequencies by combining nonlinear functions of intensity of at least two exposures combined with at least one nonlinear processing step intermediate between the two exposures to form three dimensional patterns comprising the steps of:	*See, e.g.*, Abstract: "A layer of material formed over a semiconductor substrate may be patterned in accordance with separate masks. A first mask may have a feature which is substantially perpendicular to a feature of a separate second mask. Where the layer is patterned to form transistor gates, the minimum amount each transistor gate should extend over the edge of its active region under the endcap rule may be reduced. In this regard, a line pattern mask and a gap mask are used to avoid lithographic rounding effects in forming the transistor gates. Semiconductor devices may thus be fabricated with higher packing densities as transistors may be placed closer to one another." *See, e.g.*, figs.5a-5d:

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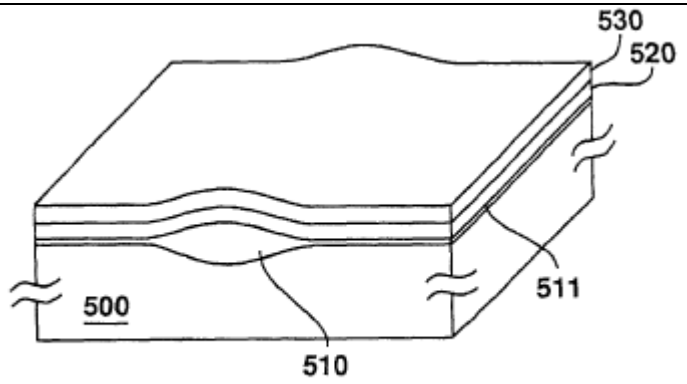
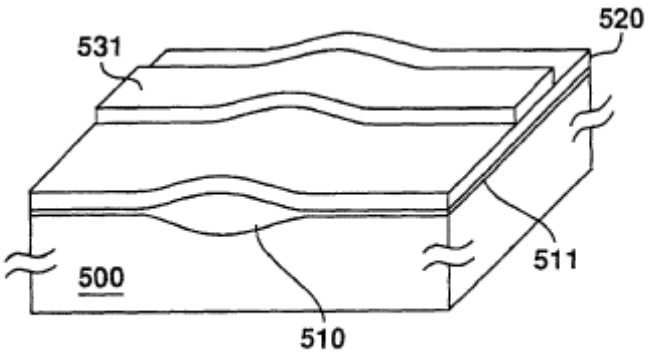
	 FIGURE 5a  FIGURE 5b

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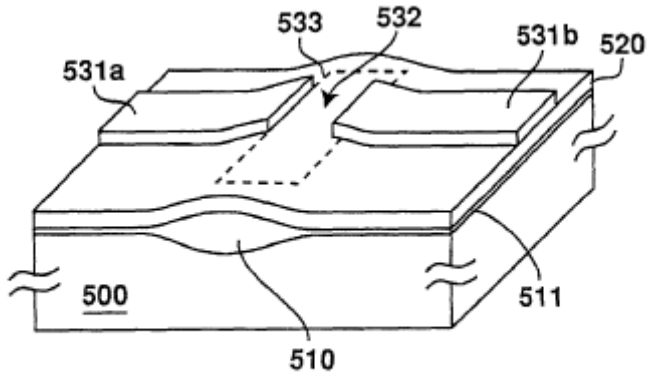
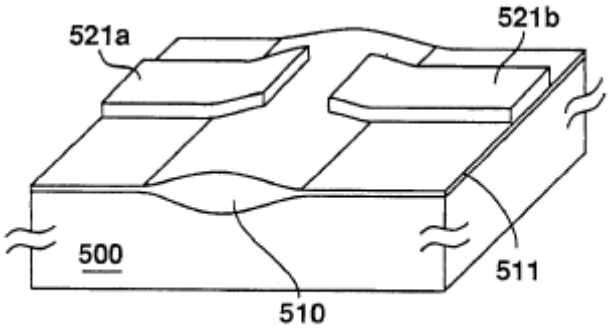
	 FIGURE 5c  FIGURE 5d *See, e.g.*, C7:41 to C9:28: "FIG. 4 illustrates, in the form of a flow diagram, a second exemplary method for patterning a layer formed over a semiconductor substrate in accordance with the present invention. So as to better explain this second exemplary method of the present invention, FIGS. 5a, 5b, 5c, and 5d will be used to illustrate the steps performed in the method of FIG. 4. Steps 400, 405, and 410 of FIG. 4 are similarly performed as steps 200, 205, and 210 of FIG. 2, respectively, discussed above. The above discussion pertaining to steps 200, 205, and 210 therefore similarly applies here as well. Briefly, a field oxide region, gate oxide layer, and polysilicon layer

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	are formed over a semiconductor substrate. This is illustrated in FIG. 5a where field oxide region 510, gate oxide layer 511, and polysilicon layer 520 have been formed over substrate 500. In step 415 of FIG. 4, then, a mask layer is formed over the wafer, as illustrated in FIG. 5a where mask layer 530 has been formed over substrate 500. The mask layer may contain any suitable material or materials which may be patterned to provide for a mask when the underlying polysilicon layer is etched. The mask layer may be a hard mask layer, for example. The mask layer may comprise approximately 200 .ANG. to approximately 2000 .ANG. of silicon dioxide (SiO.sub.2) or of silicon nitride (Si.sub.3 N.sub.4), for example. Other thicknesses of these materials may also be used and may depend, for example, on the deposition technique used to form this mask layer or the etch technique used to etch this mask layer. Furthermore, where the mask layer comprises silicon dioxide (SiO.sub.2), it may be deposited or grown over the polysilicon layer. The mask layer is then patterned in step 420 of FIG. 4 to define the pattern for polysilicon gates to be etched from the underlying polysilicon layer. Here, the mask layer may first be patterned to define a line pattern for the underlying polysilicon layer. This line pattern in the mask crosses over two active regions separated by the field oxide region, as illustrated in FIG. 5b where mask layer 530 of FIG. 5a has been patterned to form line pattern 531 which crosses over two active regions separated by field oxide region 510. In patterning the mask layer here, any suitable patterning process may be used. Where the mask layer is a hard mask layer, for example, a layer of photosensitive material such as photoresist may be formed over the wafer, exposed to radiation such as ultraviolet radiation through a suitable line pattern mask, and developed to define in the photosensitive material the line pattern to be etched from the mask layer. The mask layer may then be etched using a suitable etch technique and chemistry to form the line pattern. Here, a timed etch or an endpoint etch may be used. The etch may be selective to polysilicon to protect the underlying polysilicon layer from any overetch. It is to be appreciated, though, that the etch technique used here does not have to be highly selective to polysilicon because the underlying polysilicon which may be subjected to any overetch will later be removed. The remaining photosensitive material may then be removed following this etch. Once the line pattern has been formed, it may be patterned again to define the polysilicon gates to be etched from the underlying polysilicon layer. That is, a gap may be formed in the line pattern, as illustrated in FIG. 5c where line pattern 531 of FIG. 5b has been patterned into gate patterns 531a and 531b by forming a gap 532 in line pattern 531. In patterning the mask here, any suitable patterning process may be used. Where the mask is a hard mask, for example, a layer of photosensitive material such as photoresist may be formed over the wafer; exposed to radiation such as ultraviolet radiation through a suitable gap mask, and developed to define in the photosensitive material the gap to be etched from the mask line pattern. The shape of the gap pattern in the photosensitive material is illustrated in FIG. 5c by dashed-line rectangle 533. It is to

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	be understood, however, that the gap pattern is not limited to this illustrated shape but rather may be shaped differently in defining the gap to be etched from the mask line pattern. For example, the gap pattern may be shaped so as to extend across more than one mask line pattern so that polysilicon gates may be formed elsewhere over the wafer using this same mask. The gap pattern in the photosensitive material preferably exposes the entire width of the line pattern so as to ensure that the line pattern will be completely separated by the gap to be etched. It is to be appreciated that the gap pattern in the photosensitive material may expose portions of the polysilicon layer which are not covered by the mask line pattern. The gap may then be etched from the mask line pattern using a suitable etch technique and chemistry. For example, a timed or endpoint etch may be used. The etch may be selective to polysilicon to protect portions of the polysilicon layer which are not covered by the mask line pattern and which are exposed by the gap pattern in the photosensitive material. Where the mask layer comprises oxide, for example, the oxide:polysilicon selectivity of this etch may be in the range of approximately 5:1 to approximately 10:1. Other suitable selectivity ratios may also be used, however, and may depend on the thicknesses of the mask layer and the underlying polysilicon layer. It is to be appreciated, though, that the etch technique used here does not have to be highly selective to polysilicon because the underlying polysilicon subjected to this etch will later be removed. Following removal of the remaining photosensitive material, then, the pattern to create polysilicon gates from the underlying polysilicon layer remains, as illustrated in FIG. 5c. The underlying polysilicon layer may now be etched in step 425 of FIG. 4 using the pattern created in the mask layer as a mask to form the polysilicon gates. That is, the polysilicon layer is etched to replicate in the polysilicon layer the pattern of the mask. This is illustrated in FIG. 5d where polysilicon layer 520 of FIGS. 5a-5c has been etched using gate patterns 531a and 531b as a mask to form polysilicon gates 521a and 521b. In etching the polysilicon layer using the mask, any suitable etch technique and chemistry may be used. As an example, a polysilicon:oxide selective etch may be used where the mask layer comprises silicon dioxide (SiO.sub.2). This selective etch would also protect against spiking through the gate oxide layer. As another example, an etch selective to nitride may be used where the mask layer comprises silicon nitride (Si.sub.3 N.sub.4). This etch may be a timed etch or an endpoint etch to minimize any overetch of the underlying gate oxide layer. The remaining mask 531a and 531b is then removed from the wafer in step 430 of FIG. 4." The phrase "the Fourier transform of said pattern contains high spatial frequencies" is an inherent

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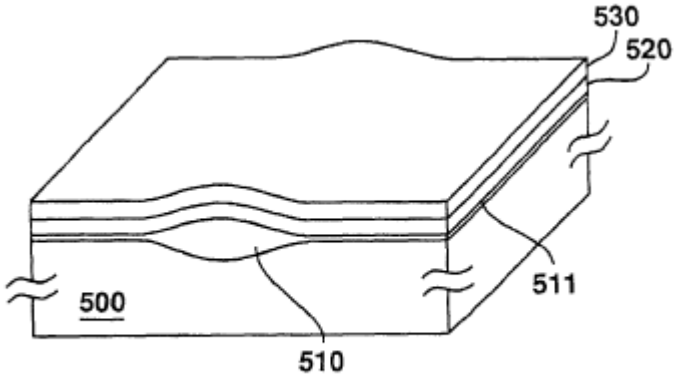
	result of the nonlinear processing step. Also, Admitted Prior Art in the '998 patent itself, Brueck '835, Waldo '094, Ziger, Gwozdz, and Elliott[1] each discloses nonlinear processing, e.g., as explained in "Invalidity Claim Chart Comparing '998 Patent to AAPA, Brueck '835, Waldo '094, Ziger, Gwozdz, and Elliott," served concurrently herewith.
coating a substrate with a first mask material and a first photoresist layer; exposing said first photoresist layer with a first exposure developing said photoresist to form a first pattern in said first photoresist layer, said first pattern containing spatial frequencies greater than those in a two dimensional optical intensity image imposed onto said photoresist layer in said first exposure as a result of a nonlinear response of said first photoresist layer;	*See, e.g.*, figs.5a & 5b:  FIGURE 5a

[1] U.S. Patent No. 5,415,835 to Brueck et al. ("Brueck '835"), U.S. Patent No. 4,891,094 to Waldo III ("Waldo '094"), David H. Ziger, et al., *Generalized Approach Toward Modeling Resist Performance*, ALCHE JOURNAL, Vol. 37, No. 12, Dec. 1991, at 1863-74 ("Ziger"), Peter S. Gwozdz, *Positive Versus Negative: A Photoresist Analysis*, SEMICONDUCTOR LITHOGRAPHY VI, SPIE Vol. 275, 1981 ("Gwozdz"), and/or David J. Elliott, INTEGRATED CIRCUIT FABRICATION TECHNOLOGY, 2d ed., 1989, at 85-106 and 326 ("Elliott").

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	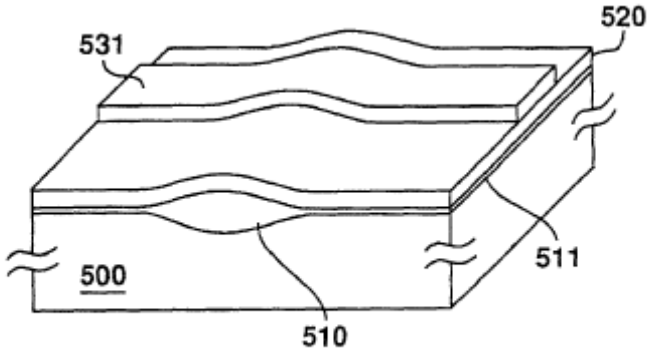 FIGURE 5b *See, e.g.*, C7:58 to C8:31: "In step 415 of FIG. 4, then, a mask layer is formed over the wafer, as illustrated in FIG. 5a where mask layer 530 has been formed over substrate 500. The mask layer may contain any suitable material or materials which may be patterned to provide for a mask when the underlying polysilicon layer is etched. The mask layer may be a hard mask layer, for example. The mask layer may comprise approximately 200 .ANG. to approximately 2000 .ANG. of silicon dioxide (SiO.sub.2) or of silicon nitride (Si.sub.3 N.sub.4), for example. Other thicknesses of these materials may also be used and may depend, for example, on the deposition technique used to form this mask layer or the etch technique used to etch this mask layer. Furthermore, where the mask layer comprises silicon dioxide (SiO.sub.2), it may be deposited or grown over the polysilicon layer. The mask layer is then patterned in step 420 of FIG. 4 to define the pattern for polysilicon gates to be etched from the underlying polysilicon layer. Here, the mask layer may first be patterned to define a line pattern for the underlying polysilicon layer. This line pattern in the mask crosses over two active regions separated by the field oxide region, as illustrated in FIG. 5b where mask layer 530 of FIG. 5a has been patterned to form line pattern 531 which crosses over two active regions separated by field oxide region 510. In patterning the mask layer here, any suitable patterning process may be used. Where the mask layer is a hard mask layer, for example, a layer of photosensitive material such as photoresist may be formed over the wafer, exposed to radiation such as ultraviolet radiation through a suitable line pattern mask, and developed to define in the photosensitive material the line pattern to be etched from the mask layer. The mask layer may then be etched using a suitable etch technique and chemistry to form the line pattern. Here, a timed etch or an endpoint etch may be used. The etch may be selective to polysilicon to protect the underlying

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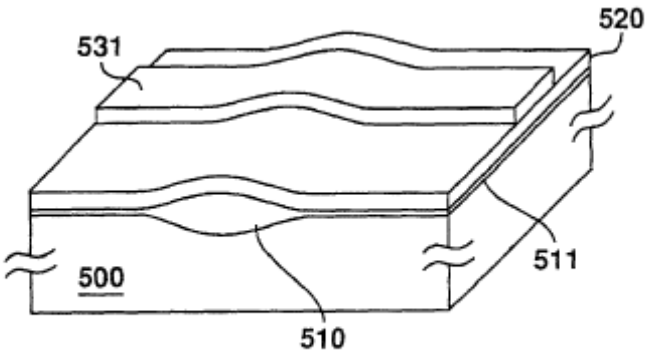
	polysilicon layer from any overetch. It is to be appreciated, though, that the etch technique used here does not have to be highly selective to polysilicon because the underlying polysilicon which may be subjected to any overetch will later be removed. The remaining photosensitive material may then be removed following this etch." The phrase "containing spatial frequencies greater than those in a two dimensional optical intensity image imposed onto said photoresist layer . . . as a result of a nonlinear response of said [photoresist layer]" is inherently disclosed in the above-cited disclosure of photoresist. Also, Admitted Prior Art in the '998 patent itself, Brueck '835, Waldo '094, Ziger, Gwozdz, and Elliott each discloses the nonlinear response of photoresist, e.g., as explained in "Invalidity Claim Chart Comparing '998 Patent to AAPA, Brueck '835, Waldo '094, Ziger, Gwozdz, and Elliott," served concurrently herewith.
transferring said first pattern into said first mask material, said first mask material comprising at least one of SiO.sub.2, Si.sub.3 N.sub.4, a metal, a polysilicon and a polymer;	*See, e.g.*, fig.5b:  FIGURE 5b *See, e.g.*, C7:58 to C8:31: "In step 415 of FIG. 4, then, a mask layer is formed over the wafer, as illustrated in FIG. 5a where mask layer 530 has been formed over substrate 500. The mask layer may contain any suitable material or materials which may be patterned to provide for a mask when the underlying polysilicon layer is etched. The mask layer may be a hard mask layer, for example. The mask layer may comprise approximately 200 .ANG. to approximately 2000 .ANG. of silicon dioxide (SiO.sub.2) or of silicon nitride (Si.sub.3 N.sub.4), for example. Other thicknesses of these materials may also be used and may depend, for example, on the deposition technique used to form

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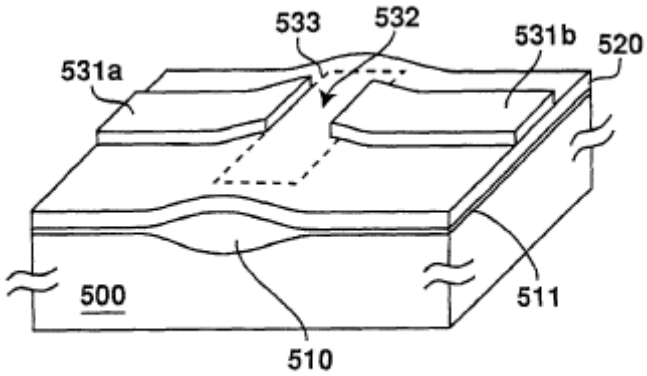
	this mask layer or the etch technique used to etch this mask layer. Furthermore, where the mask layer comprises silicon dioxide (SiO.sub.2), it may be deposited or grown over the polysilicon layer. The mask layer is then patterned in step 420 of FIG. 4 to define the pattern for polysilicon gates to be etched from the underlying polysilicon layer. Here, the mask layer may first be patterned to define a line pattern for the underlying polysilicon layer. This line pattern in the mask crosses over two active regions separated by the field oxide region, as illustrated in FIG. 5b where mask layer 530 of FIG. 5a has been patterned to form line pattern 531 which crosses over two active regions separated by field oxide region 510. In patterning the mask layer here, any suitable patterning process may be used. Where the mask layer is a hard mask layer, for example, a layer of photosensitive material such as photoresist may be formed over the wafer, exposed to radiation such as ultraviolet radiation through a suitable line pattern mask, and developed to define in the photosensitive material the line pattern to be etched from the mask layer. The mask layer may then be etched using a suitable etch technique and chemistry to form the line pattern. Here, a timed etch or an endpoint etch may be used. The etch may be selective to polysilicon to protect the underlying polysilicon layer from any overetch. It is to be appreciated, though, that the etch technique used here does not have to be highly selective to polysilicon because the underlying polysilicon which may be subjected to any overetch will later be removed. The remaining photosensitive material may then be removed following this etch."
coating said substrate with a second photoresist; exposing said second photoresist with a second exposure developing said second photoresist layer to form a second pattern in said second photoresist layer, said second pattern containing spatial frequencies greater than those in a two dimensional optical intensity image imposed onto said photoresist layer in said second exposure as a result of a nonlinear response of said second photoresist layer;	*See, e.g.*, fig.5c:  FIGURE 5c

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	See, e.g., C8:32 to C9:9: "Once the line pattern has been formed, it may be patterned again to define the polysilicon gates to be etched from the underlying polysilicon layer. That is, a gap may be formed in the line pattern, as illustrated in FIG. 5c where line pattern 531 of FIG. 5b has been patterned into gate patterns 531a and 531b by forming a gap 532 in line pattern 531. In patterning the mask here, any suitable patterning process may be used. Where the mask is a hard mask, for example, a layer of photosensitive material such as photoresist may be formed over the wafer; exposed to radiation such as ultraviolet radiation through a suitable gap mask, and developed to define in the photosensitive material the gap to be etched from the mask line pattern. The shape of the gap pattern in the photosensitive material is illustrated in FIG. 5c by dashed-line rectangle 533. It is to be understood, however, that the gap pattern is not limited to this illustrated shape but rather may be shaped differently in defining the gap to be etched from the mask line pattern. For example, the gap pattern may be shaped so as to extend across more than one mask line pattern so that polysilicon gates may be formed elsewhere over the wafer using this same mask. The gap pattern in the photosensitive material preferably exposes the entire width of the line pattern so as to ensure that the line pattern will be completely separated by the gap to be etched. It is to be appreciated that the gap pattern in the photosensitive material may expose portions of the polysilicon layer which are not covered by the mask line pattern. The gap may then be etched from the mask line pattern using a suitable etch technique and chemistry. For example, a timed or endpoint etch may be used. The etch may be selective to polysilicon to protect portions of the polysilicon layer which are not covered by the mask line pattern and which are exposed by the gap pattern in the photosensitive material. Where the mask layer comprises oxide, for example, the oxide:polysilicon selectivity of this etch may be in the range of approximately 5:1 to approximately 10:1. Other suitable selectivity ratios may also be used, however, and may depend on the thicknesses of the mask layer and the underlying polysilicon layer. It is to be appreciated, though, that the etch technique used here does not have to be highly selective to polysilicon because the underlying polysilicon subjected to this etch will later be removed. Following removal of the remaining photosensitive material, then, the pattern to create polysilicon gates from the underlying polysilicon layer remains, as illustrated in FIG. 5c." The phrase "containing spatial frequencies greater than those in a two dimensional optical intensity image imposed onto said photoresist layer . . . as a result of a nonlinear response of said [photoresist layer]" is inherently disclosed in the above-cited disclosure of photoresist. Also, Admitted Prior Art in the '998 patent itself, Brueck '835, Waldo '094, Ziger, Gwozdz, and Elliott each discloses the nonlinear response of photoresist, e.g., as explained in "Invalidity Claim Chart Comparing '998 Patent to AAPA, Brueck '835, Waldo '094, Ziger, Gwozdz, and Elliott," served concurrently herewith.

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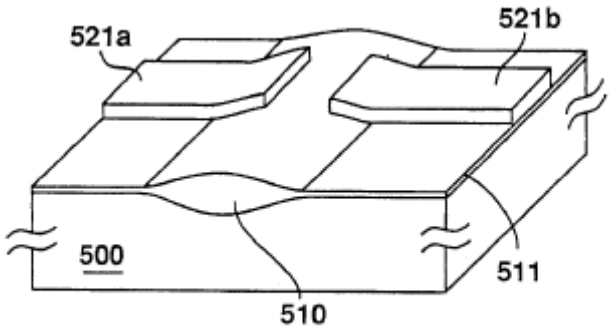
transferring said first pattern and said second pattern into said substrate using a combined mask including parts of said first mask layer and said second photoresist;	*See, e.g.*, fig.5d:  FIGURE 5d *See, e.g.*, C9:10-28: "The underlying polysilicon layer may now be etched in step 425 of FIG. 4 using the pattern created in the mask layer as a mask to form the polysilicon gates. That is, the polysilicon layer is etched to replicate in the polysilicon layer the pattern of the mask. This is illustrated in FIG. 5d where polysilicon layer 520 of FIGS. 5a-5c has been etched using gate patterns 531a and 531b as a mask to form polysilicon gates 521a and 521b. In etching the polysilicon layer using the mask, any suitable etch technique and chemistry may be used. As an example, a polysilicon:oxide selective etch may be used where the mask layer comprises silicon dioxide (SiO.sub.2). This selective etch would also protect against spiking through the gate oxide layer. As another example, an etch selective to nitride may be used where the mask layer comprises silicon nitride (Si.sub.3 N.sub.4). This etch may be a timed etch or an endpoint etch to minimize any overetch of the underlying gate oxide layer. The remaining mask 531a and 531b is then removed from the wafer in step 430 of FIG. 4."
removing said first mask material and said second photoresist.	*See, e.g.*, fig.5d:

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	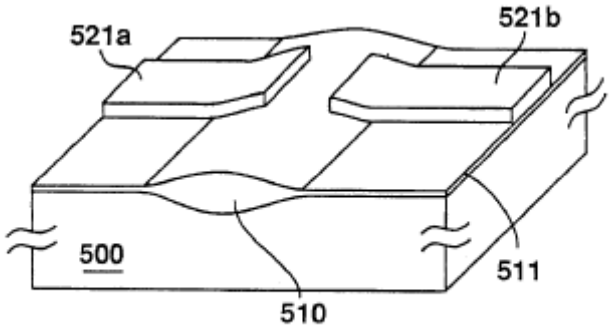 FIGURE 5d *See, e.g.,* C9:10-28: "The underlying polysilicon layer may now be etched in step 425 of FIG. 4 using the pattern created in the mask layer as a mask to form the polysilicon gates. That is, the polysilicon layer is etched to replicate in the polysilicon layer the pattern of the mask. This is illustrated in FIG. 5d where polysilicon layer 520 of FIGS. 5a-5c has been etched using gate patterns 531a and 531b as a mask to form polysilicon gates 521a and 521b. In etching the polysilicon layer using the mask, any suitable etch technique and chemistry may be used. As an example, a polysilicon:oxide selective etch may be used where the mask layer comprises silicon dioxide (SiO.sub.2). This selective etch would also protect against spiking through the gate oxide layer. As another example, an etch selective to nitride may be used where the mask layer comprises silicon nitride (Si.sub.3 N.sub.4). This etch may be a timed etch or an endpoint etch to minimize any overetch of the underlying gate oxide layer. The remaining mask 531a and 531b is then removed from the wafer in step 430 of FIG. 4."
7. The method of claim 6 wherein said transferring step includes at least one of etching, deposition and-lift off, and damascene.	*See, e.g.,* figs.5c & 5d:

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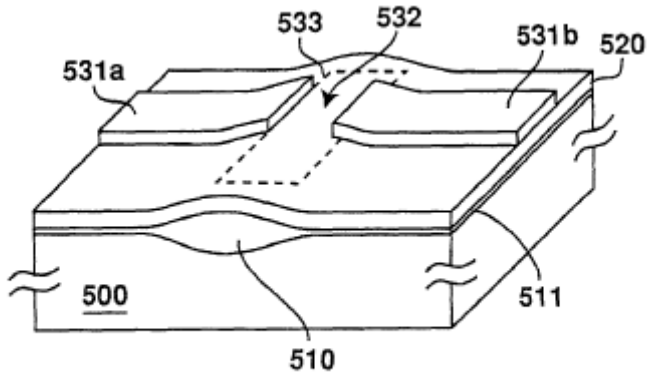
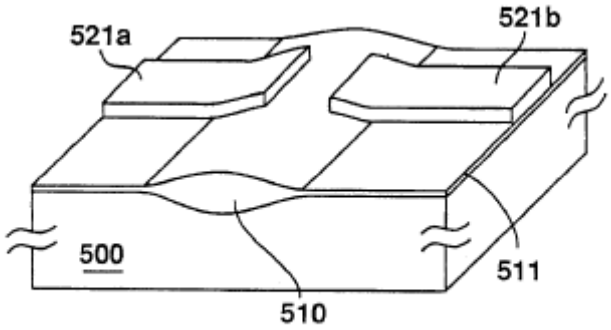
	 FIGURE 5c  FIGURE 5d *See, e.g.*, C8:32 to C9:28: "Once the line pattern has been formed, it may be patterned again to define the polysilicon gates to be etched from the underlying polysilicon layer. That is, a gap may be formed in the line pattern, as illustrated in FIG. 5c where line pattern 531 of FIG. 5b has been patterned into gate patterns 531a and 531b by forming a gap 532 in line pattern 531. In patterning the mask here, any suitable patterning process may be used. Where the mask is a hard mask, for example, a layer of photosensitive material such as photoresist may be formed over the wafer; exposed to radiation such as ultraviolet radiation through a suitable gap mask, and developed to define in the photosensitive material the gap to be etched from the mask line pattern. The shape of the gap

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	pattern in the photosensitive material is illustrated in FIG. 5c by dashed-line rectangle 533. It is to be understood, however, that the gap pattern is not limited to this illustrated shape but rather may be shaped differently in defining the gap to be etched from the mask line pattern. For example, the gap pattern may be shaped so as to extend across more than one mask line pattern so that polysilicon gates may be formed elsewhere over the wafer using this same mask. The gap pattern in the photosensitive material preferably exposes the entire width of the line pattern so as to ensure that the line pattern will be completely separated by the gap to be etched. It is to be appreciated that the gap pattern in the photosensitive material may expose portions of the polysilicon layer which are not covered by the mask line pattern. The gap may then be etched from the mask line pattern using a suitable etch technique and chemistry. For example, a timed or endpoint etch may be used. The etch may be selective to polysilicon to protect portions of the polysilicon layer which are not covered by the mask line pattern and which are exposed by the gap pattern in the photosensitive material. Where the mask layer comprises oxide, for example, the oxide:polysilicon selectivity of this etch may be in the range of approximately 5:1 to approximately 10:1. Other suitable selectivity ratios may also be used, however, and may depend on the thicknesses of the mask layer and the underlying polysilicon layer. It is to be appreciated, though, that the etch technique used here does not have to be highly selective to polysilicon because the underlying polysilicon subjected to this etch will later be removed. Following removal of the remaining photosensitive material, then, the pattern to create polysilicon gates from the underlying polysilicon layer remains, as illustrated in FIG. 5c. The underlying polysilicon layer may now be etched in step 425 of FIG. 4 using the pattern created in the mask layer as a mask to form the polysilicon gates. That is, the polysilicon layer is etched to replicate in the polysilicon layer the pattern of the mask. This is illustrated in FIG. 5d where polysilicon layer 520 of FIGS. 5a-5c has been etched using gate patterns 531a and 531b as a mask to form polysilicon gates 521a and 521b. In etching the polysilicon layer using the mask, any suitable etch technique and chemistry may be used. As an example, a polysilicon:oxide selective etch may be used where the mask layer comprises silicon dioxide (SiO.sub.2). This selective etch would also protect against spiking through the gate oxide layer. As another example, an etch selective to nitride may be used where the mask layer comprises silicon nitride (Si.sub.3 N.sub.4). This etch may be a timed etch or an endpoint etch to minimize any overetch of the underlying gate oxide layer. The remaining mask 531a and 531b is then removed from the wafer in step 430 of FIG. 4."