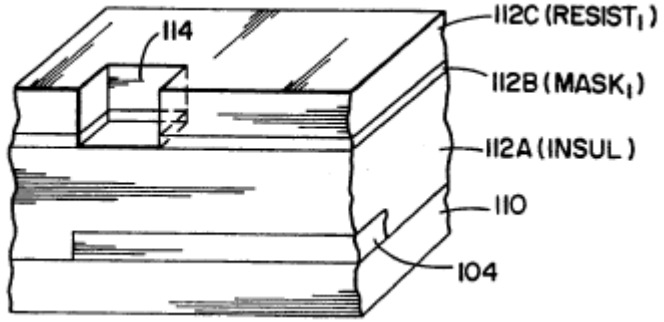
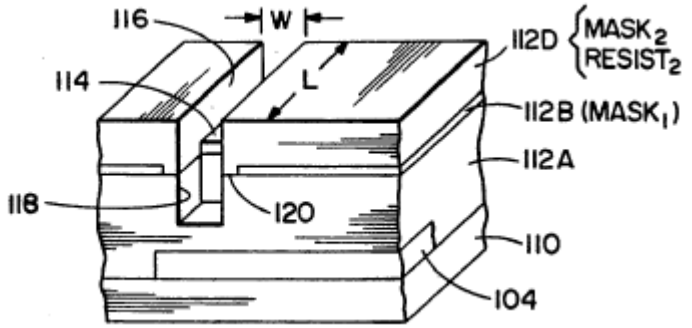
Exhibit 5

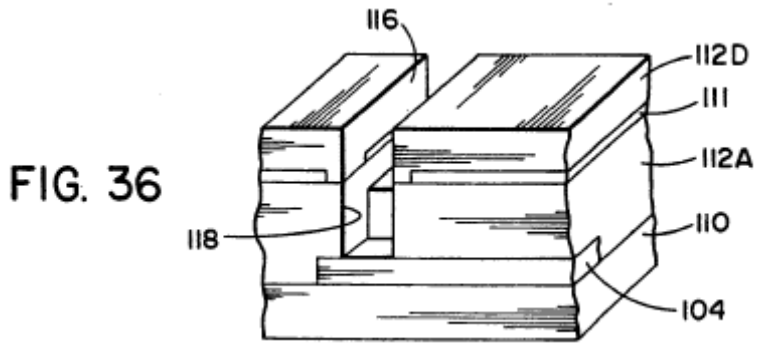
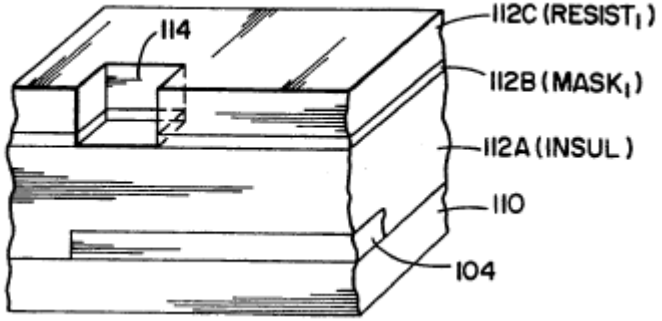
STC.UNM v. Intel

Invalidity Claim Chart Comparing '998 Patent to Cronin '006

The following asserted claims of STC.UNM's U.S. Pat. No. 6,042,998 ("'998 patent") are invalidated pursuant to 35 U.S.C. § 102 and/or § 103, alone or in combination with other references, by the prior art reference U.S. Pat. No. 5,126,006 to Cronin et al., entitled "Plural Level Chip Masking," with issue date June 30, 1992 ("Cronin '006"). These preliminary invalidity contentions are based on information currently known to Intel, and, as a result, apply interpretations apparently or potentially adopted by STC.UNM. Intel reserves the right to amend its preliminary invalidity contentions in light of developments in the case such as production of discovery, identification of additional prior art, and issuance of an order following any Claim Construction Hearing, as stated in the Scheduling Order (Dkt. 47, dated March 2, 2011).

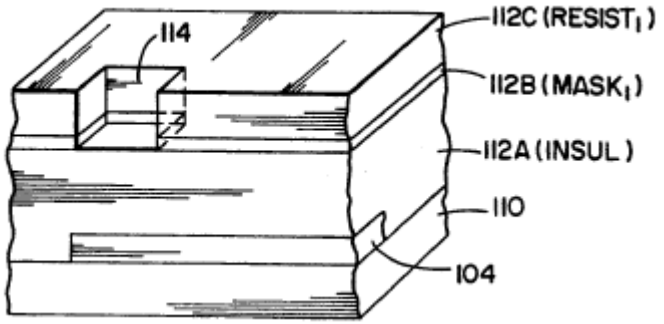
Asserted Claims of '998 Patent	Cronin '006
6. A method for obtaining a pattern wherein the Fourier transform of said pattern contains high spatial frequencies by combining nonlinear functions of intensity of at least two exposures combined with at least one nonlinear processing step intermediate between the two exposures to form three dimensional patterns comprising the steps of:	*See, e.g.*, C12:67 to C13:36: "In FIG. 34, the layer 112B is converted to a first mask. This is accomplished by depositing a first layer 112C of photoresist upon the layer 112B. A void 114 is created in the layers 112C and 112B, the void 114 extending through the layers 112C and 112B down to the top surface of the layer 112A. The void 114 is constructed by masking and etching steps such as those disclosed in FIGS. 5 and 6 for creating the opening 30 in the photoresist layer 24C. Extension of the void 114 through the layer 112B (FIG. 34) is accomplished by a further etch step such as used in describing in FIG. 10. This produces the desired shape or pattern to the layer 112B as shown in FIG. 34. By way of example, in the event that the layer 112B is fabricated of a metal, the etchant source 56 of FIG. 10 may be employed for reactive ion etching (RIE) for a dry plasma etch of chloride ions, or a suitable liquid etch. The portion of the void 114 in the layer 112C is obtained by removing light-exposed area of the photoresist by use of developer. In FIG. 35, the procedure continues by stripping off the first layer 112C of the photoresist, and replacing this layer with a second layer 112D of photoresist. Thereupon, by masking and use of developer, the layer 112D is etched down to the layer 112B to form a horizontal trough 116 at the location of the void 114, the material of the layer 112D extends down to the insulator layer 112A and, accordingly, during the formation of the trough 116, the photoresist of the layer 112D is removed down to the top surface of the layer 112A. Upon constructing the trough 116 within the layer 112D, the layer 112D takes the form of a second etch mask which trims the size of the via 114 in layer 112B. A further RIE employing CHF.sub.3 +O.sub.2 produces an opening 118 within the insulator layer 112A, the etching of the opening 118 extending downward approximately 0.6 microns into the insulator layer 112A. This produces the structure shown in FIG. 35."

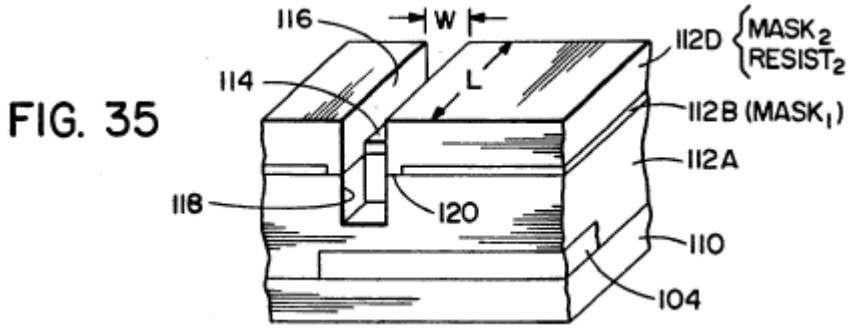
Asserted Claims of '998 Patent	Cronin '006
	See, e.g., C14:5-21: "In FIG. 36, the procedure continues with an etching of the region of the layer 112B disposed along the bottom of the trough 116 in FIG. 35. The same etchant is employed as was employed in the creation of the void 114 in the layer 112B. This exposes the top surface of the insulator layer 112A in the region of the trough 116. Thereupon, in FIG. 36, the etching for creation of the opening 118 is resumed to extend the opening 118 down to the electrically conductive element 104, this being a further etching of approximately 0.3 microns. Since the insulator layer 112A is exposed to the etchant throughout the length of the trough 116, the bottom of the trough 116 is etched to a greater depth, namely, the aforementioned 0.3 microns. During this etching step, the second mask of layer 112D serves to define the pattern which is etched in the insulator layer 112A. There results the structure shown shown in FIG. 36." *See, e.g.*, figs.34-36: FIG. 34  FIG. 35 

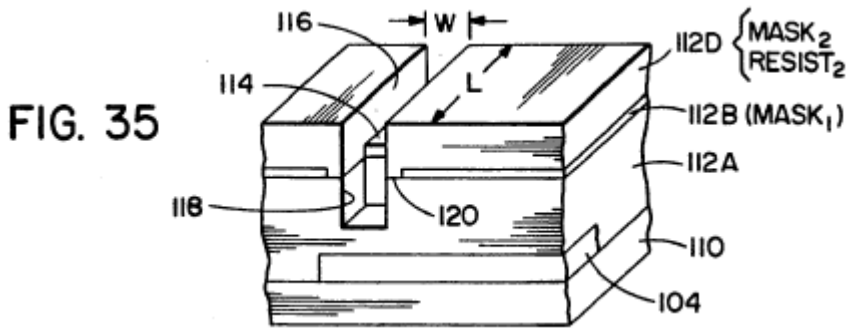
Asserted Claims of '998 Patent	Cronin '006
	 FIG. 36 The phrase "the Fourier transform of said pattern contains high spatial frequencies" is an inherent result of the nonlinear processing step. Also, Admitted Prior Art in the '998 patent itself, Brueck '835, Waldo '094, Ziger, Gwozdz, and Elliott each discloses nonlinear processing, e.g., as explained in "Invalidity Claim Chart Comparing '998 Patent to AAPA, Brueck '835, Waldo '094, Ziger, Gwozdz, and Elliott," served concurrently herewith.
coating a substrate with a first mask material and a first photoresist layer; exposing said first photoresist layer with a first exposure developing said photoresist to form a first pattern in said first photoresist layer, said first pattern containing spatial frequencies greater than those in a two dimensional optical intensity image imposed onto said photoresist layer in said first exposure as a result of a nonlinear response of said first photoresist layer;	*See, e.g.*, fig.34:  FIG. 34 *See, e.g.*, C12:59 to C13:18: "This is followed by deposition of a further layer 112B upon the top surface of the layer 112A. The layer 112B is formed of a material, which has the property of selective resistance to an etch so as to be suitable for use as an etch-stop layer. By way of example, a suitable material is aluminum oxide,

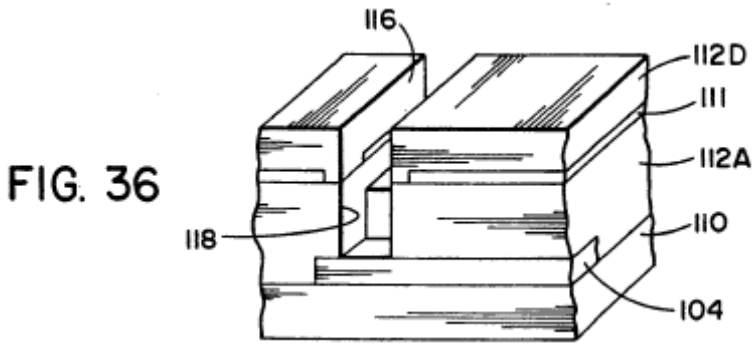
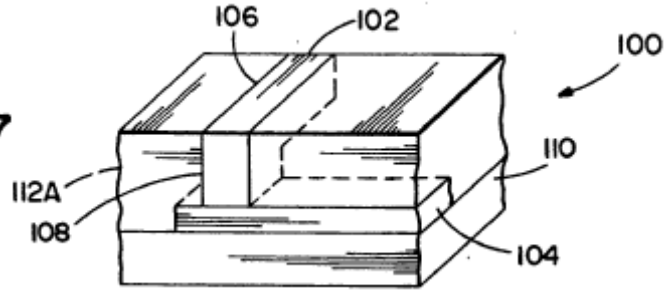
Asserted Claims of '998 Patent	Cronin '006
	or silicon nitride, silicon or a metal. The layer 112B has a thickness typically of 0.2 microns. In FIG. 34, the layer 112B is converted to a first mask. This is accomplished by depositing a first layer 112C of photoresist upon the layer 112B. A void 114 is created in the layers 112C and 112B, the void 114 extending through the layers 112C and 112B down to the top surface of the layer 112A. The void 114 is constructed by masking and etching steps such as those disclosed in FIGS. 5 and 6 for creating the opening 30 in the photoresist layer 24C. Extension of the void 114 through the layer 112B (FIG. 34) is accomplished by a further etch step such as used in describing in FIG. 10. This produces the desired shape or pattern to the layer 112B as shown in FIG. 34. By way of example, in the event that the layer 112B is fabricated of a metal, the etchant source 56 of FIG. 10 may be employed for reactive ion etching (RIE) for a dry plasma etch of chloride ions, or a suitable liquid etch. The portion of the void 114 in the layer 112C is obtained by removing light-exposed area of the photoresist by use of developer." The phrase "containing spatial frequencies greater than those in a two dimensional optical intensity image imposed onto said photoresist layer . . . as a result of a nonlinear response of said [photoresist layer]" is inherently disclosed in the above-cited disclosure of photoresist. Also, Admitted Prior Art in the '998 patent itself, Brueck '835, Waldo '094, Ziger, Gwozdz, and Elliott[1] each discloses the nonlinear response of photoresist, e.g., as explained in "Invalidity Claim Chart Comparing '998 Patent to AAPA, Brueck '835, Waldo '094, Ziger, Gwozdz, and Elliott," served concurrently herewith.
transferring said first pattern into said first mask material, said first mask material comprising at least one of SiO.sub.2, Si.sub.3 N.sub.4, a metal, a polysilicon and a polymer;	*See, e.g.*, fig.34:

[1] Applicant admitted prior art (AAPA), U.S. Patent No. 5,415,835 to Brueck et al. ("Brueck '835"), U.S. Patent No. 4,891,094 to Waldo III ("Waldo '094"), David H. Ziger, et al., *Generalized Approach toward Modeling Resist Performance,* ALCHE JOURNAL, Vol. 37, No. 12, Dec. 1991, at 1863-74 ("Ziger"), Peter S. Gwozdz, *Positive Versus Negative: A Photoresist Analysis,* SEMICONDUCTOR LITHOGRAPHY VI, SPIE Vol. 275, 1981 ("Gwozdz"), and/or David J. Elliott, INTEGRATED CIRCUIT FABRICATION TECHNOLOGY, 2d ed., 1989, at 85-106 and 326 ("Elliott").

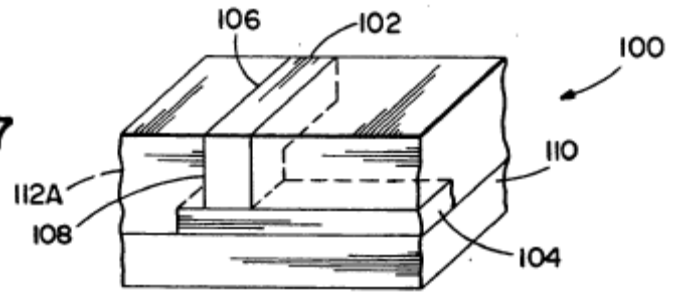
Asserted Claims of '998 Patent	Cronin '006
	FIG. 34  *See, e.g.*, C12:59 to C13:18: "This is followed by deposition of a further layer 112B upon the top surface of the layer 112A. The layer 112B is formed of a material, which has the property of selective resistance to an etch so as to be suitable for use as an etch-stop layer. By way of example, a suitable material is aluminum oxide, or silicon nitride, silicon or a metal. The layer 112B has a thickness typically of 0.2 microns. In FIG. 34, the layer 112B is converted to a first mask. This is accomplished by depositing a first layer 112C of photoresist upon the layer 112B. A void 114 is created in the layers 112C and 112B, the void 114 extending through the layers 112C and 112B down to the top surface of the layer 112A. The void 114 is constructed by masking and etching steps such as those disclosed in FIGS. 5 and 6 for creating the opening 30 in the photoresist layer 24C. Extension of the void 114 through the layer 112B (FIG. 34) is accomplished by a further etch step such as used in describing in FIG. 10. This produces the desired shape or pattern to the layer 112B as shown in FIG. 34. By way of example, in the event that the layer 112B is fabricated of a metal, the etchant source 56 of FIG. 10 may be employed for reactive ion etching (RIE) for a dry plasma etch of chloride ions, or a suitable liquid etch. The portion of the void 114 in the layer 112C is obtained by removing light-exposed area of the photoresist by use of developer."
coating said substrate with a second photoresist; exposing said second photoresist with a second exposure developing said second photoresist layer to form a second pattern in said second photoresist layer, said second pattern containing spatial frequencies greater than those in a two dimensional optical intensity image imposed onto said	*See, e.g.*, fig.35:

Asserted Claims of '998 Patent	Cronin '006
photoresist layer in said second exposure as a result of a nonlinear response of said second photoresist layer;	 FIG. 35 *See, e.g.,* C13:19-14:4: "In FIG. 35, the procedure continues by stripping off the first layer 112C of the photoresist, and replacing this layer with a second layer 112D of photoresist. Thereupon, by masking and use of developer, the layer 112D is etched down to the layer 112B to form a horizontal trough 116 at the location of the void 114, the material of the layer 112D extends down to the insulator layer 112A and, accordingly, during the formation of the trough 116, the photoresist of the layer 112D is removed down to the top surface of the layer 112A. Upon constructing the trough 116 within the layer 112D, the layer 112D takes the form of a second etch mask which trims the size of the via 114 in layer 112B. A further RIE employing CHF.sub.3 +O.sub.2 produces an opening 118 within the insulator layer 112A, the etching of the opening 118 extending downward approximately 0.6 microns into the insulator layer 112A. This produces the structure shown in FIG. 35. A feature of the invention can be noted from FIG. 35. The void 114 may have a circular or elliptical shape, which shape is a part of the first mask in the layer 112B. A cross-sectional dimension, or diameter, of the void 114 in a direction transverse to the trough 116 is preferably greater than the width of the trough 116. This is shown in FIG. 35 wherein a part of the photoresist of the layer 112D extends into side regions of the void 114, such as at the side region 120. The width of the trough 116 is designated by W and the length of the trough 116 is designated by L in FIG. 35. Reduction of the opening 118 is accomplished by use of both the first mask and the second mask. The second mask delimits a width of the opening 118 to be equal to the width W of the trough 116. The first mask delimits the orthogonal cross sectional dimension of the opening 118 by the void 114. It is noted that both of the masks are produced by photolithographic processes and, as is well known, the masks used in photolithography need be aligned with each other. However, there are limits on the tolerance with which masks can be aligned. Accordingly, the oversizing of the transverse dimension of the void 114, in the direction transverse to the trough 116, allows for some misalignment among the masks of the photolithography processes so that, even if the second mask

Asserted Claims of '998 Patent	Cronin '006
	of the layer 112D is not centered along an axis of the void 114, an adequate opening 118 can still be created. With respect to misalignment of the masks of the layers 112B, and 112D in the longitudinal direction of the trough 116, the trough 116 extends for a sufficient distance beyond the void 114 to insure an adequate area of intersection of the trough 116 with the void 114. Thereupon, an adequate opening 118 is created even in the presence of misalignment between the two masks of the layers 112B and 112D in either the longitudinal or the transverse directions of the trough 116." The phrase "containing spatial frequencies greater than those in a two dimensional optical intensity image imposed onto said photoresist layer . . . as a result of a nonlinear response of said [photoresist layer]" is inherently disclosed in the above-cited disclosure of photoresist. Also, Admitted Prior Art in the '998 patent itself, Brueck '835, Waldo '094, Ziger, Gwozdz, and Elliott each discloses the nonlinear response of photoresist, e.g., as explained in "Invalidity Claim Chart Comparing '998 Patent to AAPA, Brueck '835, Waldo '094, Ziger, Gwozdz, and Elliott," served concurrently herewith.
transferring said first pattern and said second pattern into said substrate using a combined mask including parts of said first mask layer and said second photoresist;	*See, e.g.*, figs.35-37: 

Asserted Claims of '998 Patent	Cronin '006
	 FIG. 36  FIG. 37 *See, e.g.*, C13:19 to C14:48: "In FIG. 35, the procedure continues by stripping off the first layer 112C of the photoresist, and replacing this layer with a second layer 112D of photoresist. Thereupon, by masking and use of developer, the layer 112D is etched down to the layer 112B to form a horizontal trough 116 at the location of the void 114, the material of the layer 112D extends down to the insulator layer 112A and, accordingly, during the formation of the trough 116, the photoresist of the layer 112D is removed down to the top surface of the layer 112A. Upon constructing the trough 116 within the layer 112D, the layer 112D takes the form of a second etch mask which trims the size of the via 114 in layer 112B. A further RIE employing CHF.sub.3 +O.sub.2 produces an opening 118 within the insulator layer 112A, the etching of the opening 118 extending downward approximately 0.6 microns into the insulator layer 112A. This produces the structure shown in FIG. 35. A feature of the invention can be noted from FIG. 35. The void 114 may have a circular or elliptical shape, which shape is a part of the first mask in the layer 112B. A cross-sectional dimension, or

Asserted Claims of '998 Patent	Cronin '006
	diameter, of the void 114 in a direction transverse to the trough 116 is preferably greater than the width of the trough 116. This is shown in FIG. 35 wherein a part of the photoresist of the layer 112D extends into side regions of the void 114, such as at the side region 120. The width of the trough 116 is designated by W and the length of the trough 116 is designated by L in FIG. 35. Reduction of the opening 118 is accomplished by use of both the first mask and the second mask. The second mask delimits a width of the opening 118 to be equal to the width W of the trough 116. The first mask delimits the orthogonal cross sectional dimension of the opening 118 by the void 114. It is noted that both of the masks are produced by photolithographic processes and, as is well known, the masks used in photolithography need be aligned with each other. However, there are limits on the tolerance with which masks can be aligned. Accordingly, the oversizing of the transverse dimension of the void 114, in the direction transverse to the trough 116, allows for some misalignment among the masks of the photolithography processes so that, even if the second mask of the layer 112D is not centered along an axis of the void 114, an adequate opening 118 can still be created. With respect to misalignment of the masks of the layers 112B, and 112D in the longitudinal direction of the trough 116, the trough 116 extends for a sufficient distance beyond the void 114 to insure an adequate area of intersection of the trough 116 with the void 114. Thereupon, an adequate opening 118 is created even in the presence of misalignment between the two masks of the layers 112B and 112D in either the longitudinal or the transverse directions of the trough 116. In FIG. 36, the procedure continues with an etching of the region of the layer 112B disposed along the bottom of the trough 116 in FIG. 35. The same etchant is employed as was employed in the creation of the void 114 in the layer 112B. This exposes the top surface of the insulator layer 112A in the region of the trough 116. Thereupon, in FIG. 36, the etching for creation of the opening 118 is resumed to extend the opening 118 down to the electrically conductive element 104, this being a further etching of approximately 0.3 microns. Since the insulator layer 112A is exposed to the etchant throughout the length of the trough 116, the bottom of the trough 116 is etched to a greater depth, namely, the aforementioned 0.3 microns. During this etching step, the second mask of layer 112D serves to define the pattern which is etched in the insulator layer 112A. There results the structure shown shown in FIG. 36. In FIG. 37, the photoresist of the layer 112D has been stripped off by use of plasma or RIE with oxygen. The opening 118 and the trough 116 are then filled, with an electrically-conductive material, preferably, a metal such as that employed in the construction of the element 104. For example, in the event that the element 104 is constructed of aluminum, then the opening 118 and the trough 116 are filled with aluminum by chemical vapor deposition (CVD). Thereupon, the metal in the trough 116 is planarized down to the top surface of the insulator layer 112A, the planarizing removing the material of the layer 112B. This produces the structure of the portion of the chip 100 shown in FIG. 37. The portion of the metal deposited within the opening 118 has become a stud of the via 108 and the portion of the metal deposited in the trough 116 has become the interconnect 106. The foregoing discussion of the oversizing of the void 144 in the first mask of

Asserted Claims of '998 Patent	Cronin '006
	the layer 112B applies also to alignment of the via 108 with the element 104. By way of example, and as shown in FIG. 37, the longitudinal dimension of the element 104 is perpendicular to the longitudinal dimension of the interconnect 102. The foregoing manufacturing process has facilitated alignment of the various masks which delimit and locate the interconnect 106 and the via 108 with the element 104 maximizing the cross-sectional area of their intersection."
removing said first mask material and said second photoresist.	*See, e.g.*, C14:22-33: "In FIG. 37, the photoresist of the layer 112D has been stripped off by use of plasma or RIE with oxygen. The opening 118 and the trough 116 are then filled, with an electrically-conductive material, preferably, a metal such as that employed in the construction of the element 104. For example, in the event that the element 104 is constructed of aluminum, then the opening 118 and the trough 116 are filled with aluminum by chemical vapor deposition (CVD). Thereupon, the metal in the trough 116 is planarized down to the top surface of the insulator layer 112A, the planarizing removing the material of the layer 112B." *See, e.g.*, fig.37: FIG. 37 
7. The method of claim 6 wherein said transferring step includes at least one of etching, deposition and-lift off, and damascene.	*See, e.g.*, C12:67 to C13:36: "In FIG. 34, the layer 112B is converted to a first mask. This is accomplished by depositing a first layer 112C of photoresist upon the layer 112B. A void 114 is created in the layers 112C and 112B, the void 114 extending through the layers 112C and 112B down to the top surface of the layer 112A. The void 114 is constructed by masking and etching steps such as those disclosed in FIGS. 5 and 6 for creating the opening 30 in the photoresist layer 24C. Extension of the void 114 through the layer 112B (FIG. 34) is accomplished by a further etch step such as used in describing in FIG. 10. This produces the desired shape or pattern to the layer 112B as shown in FIG. 34. By way of example, in the event that the layer 112B is fabricated of a metal, the etchant source 56 of FIG. 10

Asserted Claims of '998 Patent	Cronin '006
	may be employed for reactive ion etching (RIE) for a dry plasma etch of chloride ions, or a suitable liquid etch. The portion of the void 114 in the layer 112C is obtained by removing light-exposed area of the photoresist by use of developer. In FIG. 35, the procedure continues by stripping off the first layer 112C of the photoresist, and replacing this layer with a second layer 112D of photoresist. Thereupon, by masking and use of developer, the layer 112D is etched down to the layer 112B to form a horizontal trough 116 at the location of the void 114, the material of the layer 112D extends down to the insulator layer 112A and, accordingly, during the formation of the trough 116, the photoresist of the layer 112D is removed down to the top surface of the layer 112A. Upon constructing the trough 116 within the layer 112D, the layer 112D takes the form of a second etch mask which trims the size of the via 114 in layer 112B. A further RIE employing CHF.sub.3 +O.sub.2 produces an opening 118 within the insulator layer 112A, the etching of the opening 118 extending downward approximately 0.6 microns into the insulator layer 112A. This produces the structure shown in FIG. 35." *See, e.g.*, C14:5-21: "In FIG. 36, the procedure continues with an etching of the region of the layer 112B disposed along the bottom of the trough 116 in FIG. 35. The same etchant is employed as was employed in the creation of the void 114 in the layer 112B. This exposes the top surface of the insulator layer 112A in the region of the trough 116. Thereupon, in FIG. 36, the etching for creation of the opening 118 is resumed to extend the opening 118 down to the electrically conductive element 104, this being a further etching of approximately 0.3 microns. Since the insulator layer 112A is exposed to the etchant throughout the length of the trough 116, the bottom of the trough 116 is etched to a greater depth, namely, the aforementioned 0.3 microns. During this etching step, the second mask of layer 112D serves to define the pattern which is etched in the insulator layer 112A. There results the structure shown shown in FIG. 36."