STC.UNM v. Intel Corporation

# Exhibit 1

## STC.UNM v. Intel

## Invalidity Claim Chart Comparing '998 Patent to Jinbo '222

The following asserted claims of STC.UNM's U.S. Pat. No. 6,042,998 are invalidated pursuant to 35 U.S.C. § 102 and/or § 103, alone or in combination with other references, by the prior art reference Japanese Kokai Publication No. HEI 4[1992]-71222 to Jinbo *et al*., entitled "Pattern Formation Method," with publication date March 5, 1992 ("Jinbo '222"). These preliminary invalidity contentions are based on information currently known to Intel, and, as a result, apply interpretations apparently or potentially adopted by STC.UNM. Intel reserves the right to amend its preliminary invalidity contentions in light of developments in the case such as production of discovery, identification of additional prior art, and issuance of an order following any Claim Construction Hearing, as stated in the Scheduling Order (Dkt. 47, dated March 2, 2011).

EXHIBIT G

| Asserted Claims of '998 Patent | Japanese Kokai Publication No. HEI 4[1992]-71222 to Jinbo et al. (translation) |
|---|---|
| 6. A method for obtaining a pattern wherein the Fourier transform of said pattern contains high spatial frequencies by combining nonlinear functions of intensity of at least two exposures combined with at least one nonlinear processing step intermediate between the two exposures to form three dimensional patterns comprising the steps of: | *See*, *e.g*., Jinbo '222 (translation), fig.1: |



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| --- | --- |
| | 11 : 下地<br>13 : 第1のレジスト<br>13a:第1のレジストパターン<br>13b:不溶化処理済み第1のレジストパターン<br><br>15 : 第2のレジスト<br>15a:第2のレジストパターン<br>17 : レジストパターン<br><br>*See*, *e.g*., <u>Jinbo '222</u> (translation), at 3:<br><br>"[T]he objective of the present invention is to provide a pattern formation method capable of forming a resist pattern [with a size] at or less than the resolution limit of the projection exposure device."<br><br>*See*, *e.g*., <u>Jinbo '222</u> (translation), at 7:<br><br>"As is clear from the aforementioned explanation, by means of the pattern formation method of the present invention, a first resist pattern is formed once on a substrate, after which the next resist pattern can be formed in the region between this first resist pattern on the substrate; therefore, a fine resist pattern that exceeds the resolution limit (is less than the resolution limit) of the projection exposure device can be formed."<br><br>The phrase "the Fourier transform of said pattern contains high spatial frequencies" is an inherent |

| Asserted Claims of '998 Patent | Japanese Kokai Publication No. HEI 4[1992]-71222 to Jinbo et al. (translation) |
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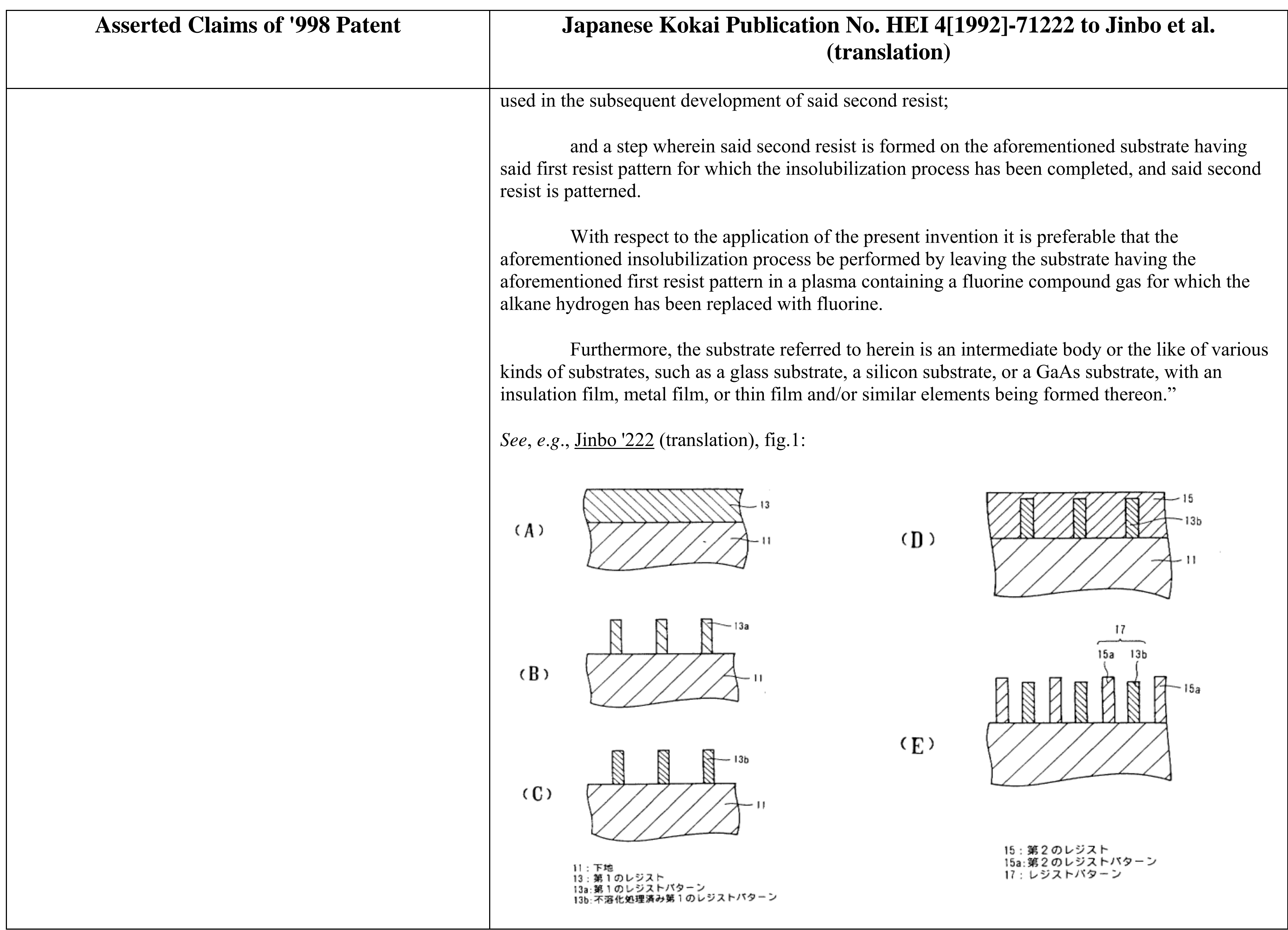
| | result of the nonlinear processing step. Also, Admitted Prior Art in the '998 patent itself, Brueck '835, Waldo '094, Ziger, Gwozdz, and Elliott[1] each discloses nonlinear processing, e.g., as explained in "Invalidity Claim Chart Comparing '998 Patent to AAPA, Brueck '835, Waldo '094, Ziger, Gwozdz, and Elliott," served concurrently herewith. |
| coating a substrate with a first mask material and a first photoresist layer;<br><br>exposing said first photoresist layer with a first exposure<br><br>developing said photoresist to form a first pattern in said first photoresist layer, said first pattern containing spatial frequencies greater than those in a two dimensional optical intensity image imposed onto said photoresist layer in said first exposure as a result of a nonlinear response of said first photoresist layer; | *See*, *e.g.*, Jinbo '222 (translation), at 1:<br><br>"1. Pattern formation method characterized by: a step wherein a first resist is formed on a substrate and said first resist is patterned; a step wherein a first resist pattern obtained by the aforementioned patterning is processed and made insoluble with respect to the solvent used for a second resist that is subsequently formed on the aforementioned substrate having said first resist pattern and with respect to the developer fluid used in the subsequent development of said second resist; and a step wherein said second resist is formed on the aforementioned substrate having said first resist pattern for which the insolubilization process has been completed, and said second resist is patterned."<br><br>*See*, *e.g.*, Jinbo '222 (translation), at 3:<br><br>"[T]he objective of the present invention is to provide a pattern formation method capable of forming a resist pattern [with a size] at or less than the resolution limit of the projection exposure device.<br><br>Means to solve the problem<br><br>To achieve this objective, the pattern formation method of the present invention is characterized by:<br><br>a step wherein a first resist is formed on a substrate and said first resist is patterned;<br><br>a step wherein a first resist pattern obtained by the aforementioned patterning is processed and made insoluble with respect to the solvent for a second resist that is subsequently formed on the aforementioned substrate having said first resist pattern and with respect to the developer fluid |

[1] U.S. Patent No. 5,415,835 to Brueck et al. ("Brueck '835"), U.S. Patent No. 4,891,094 to Waldo III ("Waldo '094"), David H. Ziger, et al., *Generalized Approach Toward Modeling Resist Performance*, ALCHE JOURNAL, Vol. 37, No. 12, Dec. 1991, at 1863-74 ("Ziger"), Peter S. Gwozdz, *Positive Versus Negative: A Photoresist Analysis*, SEMICONDUCTOR LITHOGRAPHY VI, SPIE Vol. 275, 1981 ("Gwozdz"), and/or David J. Elliott, INTEGRATED CIRCUIT FABRICATION TECHNOLOGY, 2d ed., 1989, at 85-106 and 326 ("Elliott").

<table>
<tr><th>Asserted Claims of '998 Patent</th><th>Japanese Kokai Publication No. HEI 4[1992]-71222 to Jinbo et al. (translation)</th></tr>
<tr><td></td><td>used in the subsequent development of said second resist;<br><br>and a step wherein said second resist is formed on the aforementioned substrate having said first resist pattern for which the insolubilization process has been completed, and said second resist is patterned.<br><br>With respect to the application of the present invention it is preferable that the aforementioned insolubilization process be performed by leaving the substrate having the aforementioned first resist pattern in a plasma containing a fluorine compound gas for which the alkane hydrogen has been replaced with fluorine.<br><br>Furthermore, the substrate referred to herein is an intermediate body or the like of various kinds of substrates, such as a glass substrate, a silicon substrate, or a GaAs substrate, with an insulation film, metal film, or thin film and/or similar elements being formed thereon."<br><br>See, e.g., <u>Jinbo '222</u> (translation), fig.1:<br><br></td></tr>
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| Asserted Claims of '998 Patent | Japanese Kokai Publication No. HEI 4[1992]-71222 to Jinbo et al. (translation) |
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| | The phrase "containing spatial frequencies greater than those in a two dimensional optical intensity image imposed onto said photoresist layer . . . as a result of a nonlinear response of said [photoresist layer]" is inherently disclosed in the above-cited disclosure of photoresist. Also, Admitted Prior Art in the '998 patent itself, Brueck '835, Waldo '094, Ziger, Gwozdz, and Elliott each discloses the nonlinear response of photoresist, e.g., as explained in "Invalidity Claim Chart Comparing '998 Patent to AAPA, Brueck '835, Waldo '094, Ziger, Gwozdz, and Elliott," served concurrently herewith. |

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| transferring said first pattern into said first mask material, said first mask material comprising at least one of SiO.sub.2, Si.sub.3 N.sub.4, a metal, a polysilicon and a polymer; | *See*, *e.g.*, Zdebel '002,[2] figs.3 & 4A:<br><br>FIG. 3<br><br>FIG. 4A<br><br>*See*, *e.g.*, Zdebel '002, C7:20 to C8:22:<br><br>"Two layers 84, 86 are conveniently deposited on surface 69 using low pressure chemical vapor deposition (LPCVD). First layer 84 is a layer of polycrystalline semiconductor, preferably silicon having a thickness conveniently of about 385 nanometers. Larger or smaller thicknesses may be used for layer 84 according to relationships with other layers which will be subsequently explained. Second layer 86 is conveniently a layer of silicon nitride or a sandwich of oxide plus nitride or a layer of other oxidation resistant material having a thickness of, for example, about 70-120 nanometers. Poly silicon layer 84 will be used to form poly silicon base contact regions 84 of FIG. 2. Where an NPN transistor is being formed, layer 84 is doped by ion implantation of, for example, boron. The doping may be performed during or anytime after deposition of layer 84, but is conveniently performed after deposition of layers 84 and 86 through nitride layer 86 and before deposition of layers 88 or 90. Poly silicon layer 84 is conveniently doped with singly ionized boron at an energy of about 70 KeV to a dose of about 1.times.10.sup.16 cm.sup.-2, although other |

[2] U.S. Patent No. 5,067,002 to Zdebel et al., entitled "Integrated Circuit Structures Having Polycrystalline Electrode Contacts," issued on Nov. 19, 1991 ("Zdebel '002").

| Asserted Claims of '998 Patent | Japanese Kokai Publication No. HEI 4[1992]-71222 to Jinbo et al. (translation) |
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| | doping levels may also be used depending on the desired device and circuit characteristics. The implantation is preferably arranged so that the relatively high dose of boron is located near the upper surface of polycrystalline silicon layer 84, just below silicon nitride 86.<br><br>After the boron implantation, two further layers 88, 90 are deposited, for example by LPCVD, over silicon nitride layer 86. Layer 88 is desirably an undoped layer of polycrystalline silicon having a thickness conveniently of about 180 nanometers. Larger or smaller thicknesses may be used for layer 88, taking into account the thickness of other layers, as will be subsequently explained. Layer 90 is formed overlying poly layer 88. Layer 90 conveniently prevents contamination of poly layer 88 and serves as a hard mask for subsequent lithographic patterning of the underlying layers. Layer 90 may be of any material suitable for such purposes. Layer 90 is conveniently of silicon oxide having a thickness of about 20-40 nanometers.<br><br>Processing of the structure continues with the application of layer 92 of photoresist overlying oxide layer 90 as shown schematically in FIG. 4A. The photoresist is patterned using master mask 94, represented by the shaded region in FIG. 4B, containing images 95-99 for locating various device regions. Master mask 94 provides self-alignment of the critical device areas, for example in the case of the vertical NPN transistor, the collector contact, the base contact or contacts, the emitter contact, and the emitter-base active region. In accordance with one embodiment of the invention, master mask 94 defines the master electrode area which includes emitter contact opening 95, collector contact opening 96, and base contact openings 97, 98 located within perimeter 9 and surrounded by external region 99. Region 99 identifies the region, outside perimeter 9 of master mask 94. Openings or windows 95-98 located within perimeters 5-8 respectively are used in the subsequent process to form the "footprints" of the device terminals, and in the case of the vertical bipolar device, the active emitter-base region. Perimeter 5, although referred to generally herein as the emitter opening or emitter contact opening, is used in conjunction with epitaxial island 82 formed within field oxide 71 to locate both the base and emitter of the device as well as the emitter contact. Variations and further embodiments, in addition to the basic NPN transistor, are discussed later. Base contact openings 97, 98 are located within perimeters 7, 8 respectively. Collector contact opening 96 is located within perimeter 6.” |

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| | *See*, *e.g.*, Cuthbert '076,[3] figs.2 & 3: FIG. 2 FIG. 3 *See*, *e.g.*, Cuthbert '076, C2:66 to C3:25: "A layer of spin-on-glass(SOG) 7 and a layer of photoresist 9 are now deposited to form the structure depicted in FIG. 2. The term "spin-on-glass" is well known to those skilled in the art and need not be defined. As can be seen, the SOG has a relatively planar surface and has smoothed out the topography of the underlying substrate. By relatively planar, it is meant that the surface is locally planar, although the surface may not be planar over the entire substrate surface. The SOG is put on with conventional techniques. The planarity of the surface depends upon the topography of the underlying material and the thickness of the SOG layer. Those skilled in the art will readily select a thickness for the SOG that is sufficient for it to act as an etch mask for the underlying gate. |

[3] U.S. Patent No. 5,264,076 to Cuthbert et al., entitled "Integrated Circuit Process Using a 'Hard Mask'," issued on Nov. 23, 1993, filed on Dec. 17, 1992 ("Cuthbert '076").

| Asserted Claims of '998 Patent | Japanese Kokai Publication No. HEI 4[1992]-71222 to Jinbo et al. (translation) |
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| | A thermal treatment or cure is desirably used to densify and flow the SOG. This process step also reduces the topography of the SOG and reduces variations in the resist layer thickness.<br><br>Lithographic techniques are now used to pattern the photoresist. The photoresist is then used as a mask for the etching of the SOG. The etching desirably produces vertical sidewalls in the SOG. The resulting structure is depicted in FIG. 3. Those skilled in the art will readily select appropriate etching techniques and fabricate the structure. The pattern has, for example, gate structures of field effect transistors."<br><br>*See*, *e.g*., Jinbo '222 (translation), at 1:<br><br>"1. Pattern formation method characterized by: a step wherein a first resist is formed on a substrate and said first resist is patterned; a step wherein a first resist pattern obtained by the aforementioned patterning is processed and made insoluble with respect to the solvent used for a second resist that is subsequently formed on the aforementioned substrate having said first resist pattern and with respect to the developer fluid used in the subsequent development of said second resist; and a step wherein said second resist is formed on the aforementioned substrate having said first resist pattern for which the insolubilization process has been completed, and said second resist is patterned."<br><br>*See*, *e.g*., Jinbo '222 (translation), at 3:<br><br>"[T]he objective of the present invention is to provide a pattern formation method capable of forming a resist pattern [with a size] at or less than the resolution limit of the projection exposure device.<br><br>Means to solve the problem<br><br>To achieve this objective, the pattern formation method of the present invention is characterized by:<br><br>a step wherein a first resist is formed on a substrate and said first resist is patterned;<br><br>a step wherein a first resist pattern obtained by the aforementioned patterning is processed and made insoluble with respect to the solvent for a second resist that is subsequently formed on the aforementioned substrate having said first resist pattern and with respect to the developer fluid used in the subsequent development of said second resist; |

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| | and a step wherein said second resist is formed on the aforementioned substrate having said first resist pattern for which the insolubilization process has been completed, and said second resist is patterned.<br><br>With respect to the application of the present invention it is preferable that the aforementioned insolubilization process be performed by leaving the substrate having the aforementioned first resist pattern in a plasma containing a fluorine compound gas for which the alkane hydrogen has been replaced with fluorine.<br><br>Furthermore, the substrate referred to herein is an intermediate body or the like of various kinds of substrates, such as a glass substrate, a silicon substrate, or a GaAs substrate, with an insulation film, metal film, or thin film and/or similar elements being formed thereon."<br><br>*See*, *e.g*., Jinbo '222 (translation), at 7:<br><br>"Furthermore, in the aforementioned embodiment, the same resist was used for the first resist and the second resist, but when necessary they could be different resists.<br><br>Furthermore, the present invention could also be applied so as to make the second resist pattern insoluble with respect to the solvent and developer fluid of a third resist, with the third resist pattern being formed on [the second resist], if necessary." |
| coating said substrate with a second photoresist;<br><br>exposing said second photoresist with a second exposure<br><br>developing said second photoresist layer to form a second pattern in said second photoresist layer, said second pattern containing spatial frequencies greater than those in a two dimensional optical intensity image imposed onto said photoresist layer in said second exposure as a result of a nonlinear response of said second photoresist layer; | *See*, *e.g*., Jinbo '222 (translation), at 1:<br><br>"1. Pattern formation method characterized by: a step wherein a first resist is formed on a substrate and said first resist is patterned; a step wherein a first resist pattern obtained by the aforementioned patterning is processed and made insoluble with respect to the solvent used for a second resist that is subsequently formed on the aforementioned substrate having said first resist pattern and with respect to the developer fluid used in the subsequent development of said second resist; and a step wherein said second resist is formed on the aforementioned substrate having said first resist pattern for which the insolubilization process has been completed, and said second resist is patterned."<br><br>*See*, *e.g*., Jinbo '222 (translation), at 3:<br><br>"[T]he objective of the present invention is to provide a pattern formation method capable of |

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| | forming a resist pattern [with a size] at or less than the resolution limit of the projection exposure device.<br><br>Means to solve the problem<br><br>To achieve this objective, the pattern formation method of the present invention is characterized by:<br><br>a step wherein a first resist is formed on a substrate and said first resist is patterned;<br><br>a step wherein a first resist pattern obtained by the aforementioned patterning is processed and made insoluble with respect to the solvent for a second resist that is subsequently formed on the aforementioned substrate having said first resist pattern and with respect to the developer fluid used in the subsequent development of said second resist;<br><br>and a step wherein said second resist is formed on the aforementioned substrate having said first resist pattern for which the insolubilization process has been completed, and said second resist is patterned.<br><br>With respect to the application of the present invention it is preferable that the aforementioned insolubilization process be performed by leaving the substrate having the aforementioned first resist pattern in a plasma containing a fluorine compound gas for which the alkane hydrogen has been replaced with fluorine.<br><br>Furthermore, the substrate referred to herein is an intermediate body or the like of various kinds of substrates, such as a glass substrate, a silicon substrate, or a GaAs substrate, with an insulation film, metal film, or thin film and/or similar elements being formed thereon."<br><br>*See*, *e.g.*, Jinbo '222 (translation), at 7:<br><br>"Furthermore, in the aforementioned embodiment, the same resist was used for the first resist and the second resist, but when necessary they could be different resists.<br><br>Furthermore, the present invention could also be applied so as to make the second resist pattern insoluble with respect to the solvent and developer fluid of a third resist, with the third resist pattern being formed on [the second resist], if necessary." |

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| | *See*, *e.g.*, Jinbo '222 (translation), fig.1:<br><br>(A) 13 11<br>(B) 13a 11<br>(C) 13b 11<br>(D) 15 13b 11<br>(E) 17 15a 13b 15a<br><br>11：下地<br>13：第１のレジスト<br>13a:第１のレジストパターン<br>13b:不溶化処理済み第１のレジストパターン<br>15：第２のレジスト<br>15a:第２のレジストパターン<br>17：レジストパターン<br><br>The phrase "containing spatial frequencies greater than those in a two dimensional optical intensity image imposed onto said photoresist layer . . . as a result of a nonlinear response of said [photoresist layer]" is inherently disclosed in the above-cited disclosure of photoresist. Also, Admitted Prior Art in the '998 patent itself, Brueck '835, Waldo '094, Ziger, Gwozdz, and Elliott each discloses the nonlinear response of photoresist, e.g., as explained in "Invalidity Claim Chart Comparing '998 Patent to AAPA, Brueck '835, Waldo '094, Ziger, Gwozdz, and Elliott," served concurrently herewith. |
| transferring said first pattern and said second pattern into said substrate using a combined mask including parts of said first mask layer and said second photoresist; | *See*, *e.g.*, Jinbo '222 (translation), at 1:<br><br>"1. Pattern formation method characterized by: a step wherein a first resist is formed on a substrate and said first resist is patterned; a step wherein a first resist pattern obtained by the aforementioned patterning is processed and made insoluble with respect to the solvent used for a second resist that is subsequently formed on the aforementioned substrate having said first resist pattern and with respect to the developer fluid used in the subsequent development of said second resist; and a step |

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| | wherein said second resist is formed on the aforementioned substrate having said first resist pattern for which the insolubilization process has been completed, and said second resist is patterned."<br><br>*See*, *e.g.*, Jinbo '222 (translation), at 3:<br><br>"[T]he objective of the present invention is to provide a pattern formation method capable of forming a resist pattern [with a size] at or less than the resolution limit of the projection exposure device.<br><br>Means to solve the problem<br><br>To achieve this objective, the pattern formation method of the present invention is characterized by:<br><br>a step wherein a first resist is formed on a substrate and said first resist is patterned;<br><br>a step wherein a first resist pattern obtained by the aforementioned patterning is processed and made insoluble with respect to the solvent for a second resist that is subsequently formed on the aforementioned substrate having said first resist pattern and with respect to the developer fluid used in the subsequent development of said second resist;<br><br>and a step wherein said second resist is formed on the aforementioned substrate having said first resist pattern for which the insolubilization process has been completed, and said second resist is patterned.<br><br>With respect to the application of the present invention it is preferable that the aforementioned insolubilization process be performed by leaving the substrate having the aforementioned first resist pattern in a plasma containing a fluorine compound gas for which the alkane hydrogen has been replaced with fluorine.<br><br>Furthermore, the substrate referred to herein is an intermediate body or the like of various kinds of substrates, such as a glass substrate, a silicon substrate, or a GaAs substrate, with an insulation film, metal film, or thin film and/or similar elements being formed thereon."<br><br>*See*, *e.g.*, Jinbo '222 (translation), at 7:<br><br>"Furthermore, in the aforementioned embodiment, the same resist was used for the first resist and |

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| | the second resist, but when necessary they could be different resists.<br><br>Furthermore, the present invention could also be applied so as to make the second resist pattern insoluble with respect to the solvent and developer fluid of a third resist, with the third resist pattern being formed on [the second resist], if necessary.”<br><br>*See*, *e.g.*, <u>Jinbo '222</u> (translation), fig.1:<br><br>11：下地<br>13：第１のレジスト<br>13a：第１のレジストパターン<br>13b：不溶化処理済み第１のレジストパターン<br>15：第２のレジスト<br>15a：第２のレジストパターン<br>17：レジストパターン<br><br>*See*, *e.g.*, <u>Cuthbert '076</u>, C2:66 to C3:25:<br><br>“A layer of spin-on-glass(SOG) 7 and a layer of photoresist 9 are now deposited to form the structure depicted in FIG. 2. The term "spin-on-glass" is well known to those skilled in the art and need not be defined. As can be seen, the SOG has a relatively planar surface and has smoothed out the topography of the underlying substrate. By relatively planar, it is meant that the surface is locally planar, although the surface may not be planar over the entire substrate surface. The SOG is put on with conventional techniques. The planarity of the surface depends upon the topography of the underlying material and the thickness of the SOG layer. Those skilled in the art will readily |

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| | select a thickness for the SOG that is sufficient for it to act as an etch mask for the underlying gate. A thermal treatment or cure is desirably used to densify and flow the SOG. This process step also reduces the topography of the SOG and reduces variations in the resist layer thickness.<br><br>Lithographic techniques are now used to pattern the photoresist. The photoresist is then used as a mask for the etching of the SOG. The etching desirably produces vertical sidewalls in the SOG. The resulting structure is depicted in FIG. 3. Those skilled in the art will readily select appropriate etching techniques and fabricate the structure. The pattern has, for example, gate structures of field effect transistors." |
| removing said first mask material and said second photoresist. | *See*, *e.g.*, Zdebel '002, C9:50-57:<br><br>"Subsequently, photoresist 100 is removed with, for example, organic photoresist stripper, oxygen plasma, or other suitable means. Thereafter the remainder of oxide layer 90 is removed by, for example, dip etching in a dilute hydrofluoric acid etchant solution. Other suitable etching or removal techniques known in the art may also be used."<br><br>*See*, *e.g.*, Cuthbert '076, C3:26 to C4:2:<br><br>"The photoresist is now removed. Conventional techniques may be used. The underlying polysilicon of layer is now etched using the SOG as an etch mask. After the polysilicon has been etched, the SOG is removed using, for example, an HF solution. Such a removal process may be used because of the relative etch rates of SOG to thermal oxide. Depending upon the precise technique used to cure the SOG, etch rate differentials of 15:1 or greater may be obtained. The high etch rates differential makes it possible to remove the SOG without a significant attack on either the gate (thermal) or field oxides. The resulting structure is depicted in FIG. 4."<br><br>*See*, *e.g.*, Cuthbert '076, fig.4: |

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| | FIG. 4<br><br>*See*, *e.g.*, Jinbo '222 (translation), fig.1: |
| 7. The method of claim 6 wherein said transferring step includes at least one of etching, deposition and-lift off, and damascene. | *See*, *e.g.*, Zdebel '002, C9:50-57:<br><br>"Subsequently, photoresist 100 is removed with, for example, organic photoresist stripper, oxygen plasma, or other suitable means. Thereafter the remainder of oxide layer 90 is removed by, for example, dip etching in a dilute hydrofluoric acid etchant solution. Other suitable etching or |

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| | removal techniques known in the art may also be used."<br><br>*See*, *e.g.*, Cuthbert '076, C2:66 to C3:25:<br><br>"A layer of spin-on-glass(SOG) 7 and a layer of photoresist 9 are now deposited to form the structure depicted in FIG. 2. The term "spin-on-glass" is well known to those skilled in the art and need not be defined. As can be seen, the SOG has a relatively planar surface and has smoothed out the topography of the underlying substrate. By relatively planar, it is meant that the surface is locally planar, although the surface may not be planar over the entire substrate surface. The SOG is put on with conventional techniques. The planarity of the surface depends upon the topography of the underlying material and the thickness of the SOG layer. Those skilled in the art will readily select a thickness for the SOG that is sufficient for it to act as an etch mask for the underlying gate. A thermal treatment or cure is desirably used to densify and flow the SOG. This process step also reduces the topography of the SOG and reduces variations in the resist layer thickness.<br><br>Lithographic techniques are now used to pattern the photoresist. The photoresist is then used as a mask for the etching of the SOG. The etching desirably produces vertical sidewalls in the SOG. The resulting structure is depicted in FIG. 3. Those skilled in the art will readily select appropriate etching techniques and fabricate the structure. The pattern has, for example, gate structures of field effect transistors."<br><br>*See*, *e.g.*, Cuthbert '076, C3:26 to C4:2:<br><br>"The photoresist is now removed. Conventional techniques may be used. The underlying polysilicon of layer is now etched using the SOG as an etch mask. After the polysilicon has been etched, the SOG is removed using, for example, an HF solution. Such a removal process may be used because of the relative etch rates of SOG to thermal oxide. Depending upon the precise technique used to cure the SOG, etch rate differentials of 15:1 or greater may be obtained. The high etch rates differential makes it possible to remove the SOG without a significant attack on either the gate (thermal) or field oxides. The resulting structure is depicted in FIG. 4."<br><br>*See*, *e.g.*, Cuthbert '076, fig.4: |

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|---|---|
| | FIG. 4 |
| 8. A method for increasing spatial frequency content of lithographic patterns comprising the steps of: | *See*, *e.g*., <u>Jinbo '222</u> (translation), at 3:<br><br>"[T]he objective of the present invention is to provide a pattern formation method capable of forming a resist pattern [with a size] at or less than the resolution limit of the projection exposure device."<br><br>*See*, *e.g*., <u>Jinbo '222</u> (translation), at 7:<br><br>"As is clear from the aforementioned explanation, by means of the pattern formation method of the present invention, a first resist pattern is formed once on a substrate, after which the next resist pattern can be formed in the region between this first resist pattern on the substrate; therefore, a fine resist pattern that exceeds the resolution limit (is less than the resolution limit) of the projection exposure device can be formed."<br><br>*See*, *e.g*., <u>Jinbo '222</u> (translation), fig.1: |

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| depositing a material;<br><br>depositing a photoresist on said material;<br><br>exposing a periodic image in said photoresist, said periodic image having a pitch p.sub.min and a linewidth less than p.sub.min /2;<br><br>developing said periodic image to form a periodic pattern in said photoresist; | *See*, *e.g.*, fig.1: |

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| | (A) (B) (C) (D) (E)<br>11：下地<br>13：第１のレジスト<br>13a:第１のレジストパターン<br>13b:不溶化処理済み第１のレジストパターン<br>15：第２のレジスト<br>15a:第２のレジストパターン<br>17：レジストパターン<br><br>*See*, *e.g*., Jinbo '222 (translation), at 1:<br><br>"1. Pattern formation method characterized by: a step wherein a first resist is formed on a substrate and said first resist is patterned; a step wherein a first resist pattern obtained by the aforementioned patterning is processed and made insoluble with respect to the solvent used for a second resist that is subsequently formed on the aforementioned substrate having said first resist pattern and with respect to the developer fluid used in the subsequent development of said second resist; and a step wherein said second resist is formed on the aforementioned substrate having said first resist pattern for which the insolubilization process has been completed, and said second resist is patterned."<br><br>*See*, *e.g*., Jinbo '222 (translation), at 3:<br><br>"[T]he objective of the present invention is to provide a pattern formation method capable of forming a resist pattern [with a size] at or less than the resolution limit of the projection exposure device. |

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| | Means to solve the problem<br><br>To achieve this objective, the pattern formation method of the present invention is characterized by:<br><br>a step wherein a first resist is formed on a substrate and said first resist is patterned;<br><br>a step wherein a first resist pattern obtained by the aforementioned patterning is processed and made insoluble with respect to the solvent for a second resist that is subsequently formed on the aforementioned substrate having said first resist pattern and with respect to the developer fluid used in the subsequent development of said second resist;<br><br>and a step wherein said second resist is formed on the aforementioned substrate having said first resist pattern for which the insolubilization process has been completed, and said second resist is patterned.<br><br>With respect to the application of the present invention it is preferable that the aforementioned insolubilization process be performed by leaving the substrate having the aforementioned first resist pattern in a plasma containing a fluorine compound gas for which the alkane hydrogen has been replaced with fluorine.<br><br>Furthermore, the substrate referred to herein is an intermediate body or the like of various kinds of substrates, such as a glass substrate, a silicon substrate, or a GaAs substrate, with an insulation film, metal film, or thin film and/or similar elements being formed thereon."<br><br>*See*, *e.g.*, Jinbo '222 (translation), at 5-6:<br><br>"Next, by a spin-coating method, a second resist 15 – in this case, the TSMR-365iR used as the first resist – was applied with a film thickness of 1.0 µm to substrate 11 having the first resist pattern 13b which had undergone insolubilization processing (Figure 1(D).<br><br>As described above, first resist pattern 13b which has undergone insolubilization processing is insoluble with respect to the solvent of second resist 15, so when first resist pattern 13b is covered by second resist pattern 15 the pattern of the first resist pattern itself does not break down, nor does it intermix with the second resist.<br><br>Next, second resist pattern 15 was baked under the same baking conditions as for the first |

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| | resist.<br><br>Next, substrate 11 having this baked second resist was placed on a wafer stage in the previously used projection exposure device, after which substrate 11 was aligned with respect to a mask installed in this projection exposure device. Next, the wafer stage was shifted 0.3 µm in the X direction – in other words, the wafer stage was shifted such that the line potions of the mask were projected on the space portions of first resist pattern 13b, which had undergone insolubilization processing – and then second resist 15 was exposed with an exposure amount of 300 mJ/cm2.<br><br>Next, the exposed second resist was developed under the same developing conditions as for the first resist, obtaining second resist pattern 15a (Figure 1(E)). Because first resist pattern 13b had undergone insolubilization processing as described previously so as to be insoluble with respect to the NMD-W developer fluid, no pattern breakdown occurred when the second resist pattern was developed.<br><br>After the second resist was developed, a resist pattern 17 comprised of insolubilization-processed first resist pattern 13b and second resist pattern 15a was formed on substrate 11 (Figure 1(E)). When this resist pattern 17 was observed with an S-6000 SEM measurement device, it was found that a pattern for which line portions with a width of 0.3 µm were aligned with a pitch of 0.6 µm – in other words, a 0.3 µm line-and-space pattern – had been resolved."<br><br>*See*, *e.g.*, <u>Jinbo '222</u> (translation), at 7:<br><br>"Furthermore, in the aforementioned embodiment, the same resist was used for the first resist and the second resist, but when necessary they could be different resists.<br><br>Furthermore, the present invention could also be applied so as to make the second resist pattern insoluble with respect to the solvent and developer fluid of a third resist, with the third resist pattern being formed on [the second resist], if necessary."<br><br>*See*, *e.g.*, <u>Jinbo '222</u> (translation), at 7:<br><br>"As is clear from the aforementioned explanation, by means of the pattern formation method of the present invention, a first resist pattern is formed once on a substrate, after which the next resist pattern can be formed in the region between this first resist pattern on the substrate; therefore, a fine resist pattern that exceeds the resolution limit (is less than the resolution limit) of the |

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| | projection exposure device can be formed." |
| transferring said periodic pattern to said material; | *See*, *e.g.*, Zdebel '002, figs.3 & 4A:<br><br>FIG. 3<br><br>FIG. 4A<br><br>*See*, *e.g.*, Zdebel '002, C7:20 to C8:22:<br><br>"Two layers 84, 86 are conveniently deposited on surface 69 using low pressure chemical vapor deposition (LPCVD). First layer 84 is a layer of polycrystalline semiconductor, preferably silicon having a thickness conveniently of about 385 nanometers. Larger or smaller thicknesses may be used for layer 84 according to relationships with other layers which will be subsequently explained. Second layer 86 is conveniently a layer of silicon nitride or a sandwich of oxide plus nitride or a layer of other oxidation resistant material having a thickness of, for example, about 70-120 nanometers. Poly silicon layer 84 will be used to form poly silicon base contact regions 84 of FIG. 2. Where an NPN transistor is being formed, layer 84 is doped by ion implantation of, for example, boron. The doping may be performed during or anytime after deposition of layer 84, but is conveniently performed after deposition of layers 84 and 86 through nitride layer 86 and before deposition of layers 88 or 90. Poly silicon layer 84 is conveniently doped with singly ionized boron at an energy of about 70 KeV to a dose of about 1.times.10.sup.16 cm.sup.-2, although other doping levels may also be used depending on the desired device and circuit characteristics. The |

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| | implantation is preferably arranged so that the relatively high dose of boron is located near the upper surface of polycrystalline silicon layer 84, just below silicon nitride 86.<br><br>After the boron implantation, two further layers 88, 90 are deposited, for example by LPCVD, over silicon nitride layer 86. Layer 88 is desirably an undoped layer of polycrystalline silicon having a thickness conveniently of about 180 nanometers. Larger or smaller thicknesses may be used for layer 88, taking into account the thickness of other layers, as will be subsequently explained. Layer 90 is formed overlying poly layer 88. Layer 90 conveniently prevents contamination of poly layer 88 and serves as a hard mask for subsequent lithographic patterning of the underlying layers. Layer 90 may be of any material suitable for such purposes. Layer 90 is conveniently of silicon oxide having a thickness of about 20-40 nanometers.<br><br>Processing of the structure continues with the application of layer 92 of photoresist overlying oxide layer 90 as shown schematically in FIG. 4A. The photoresist is patterned using master mask 94, represented by the shaded region in FIG. 4B, containing images 95-99 for locating various device regions. Master mask 94 provides self-alignment of the critical device areas, for example in the case of the vertical NPN transistor, the collector contact, the base contact or contacts, the emitter contact, and the emitter-base active region. In accordance with one embodiment of the invention, master mask 94 defines the master electrode area which includes emitter contact opening 95, collector contact opening 96, and base contact openings 97, 98 located within perimeter 9 and surrounded by external region 99. Region 99 identifies the region, outside perimeter 9 of master mask 94. Openings or windows 95-98 located within perimeters 5-8 respectively are used in the subsequent process to form the "footprints" of the device terminals, and in the case of the vertical bipolar device, the active emitter-base region. Perimeter 5, although referred to generally herein as the emitter opening or emitter contact opening, is used in conjunction with epitaxial island 82 formed within field oxide 71 to locate both the base and emitter of the device as well as the emitter contact. Variations and further embodiments, in addition to the basic NPN transistor, are discussed later. Base contact openings 97, 98 are located within perimeters 7, 8 respectively. Collector contact opening 96 is located within perimeter 6."<br><br>*See*, *e.g*., Cuthbert '076, figs.2 & 3: |

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| | FIG. 2 <br> FIG. 3 <br><br> *See*, *e.g.*, Cuthbert '076, C2:66 to C3:25: <br><br> "A layer of spin-on-glass(SOG) 7 and a layer of photoresist 9 are now deposited to form the structure depicted in FIG. 2. The term "spin-on-glass" is well known to those skilled in the art and need not be defined. As can be seen, the SOG has a relatively planar surface and has smoothed out the topography of the underlying substrate. By relatively planar, it is meant that the surface is locally planar, although the surface may not be planar over the entire substrate surface. The SOG is put on with conventional techniques. The planarity of the surface depends upon the topography of the underlying material and the thickness of the SOG layer. Those skilled in the art will readily select a thickness for the SOG that is sufficient for it to act as an etch mask for the underlying gate. A thermal treatment or cure is desirably used to densify and flow the SOG. This process step also reduces the topography of the SOG and reduces variations in the resist layer thickness. <br><br> Lithographic techniques are now used to pattern the photoresist. The photoresist is then used as a mask for the etching of the SOG. The etching desirably produces vertical sidewalls in the SOG. |

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| | The resulting structure is depicted in FIG. 3. Those skilled in the art will readily select appropriate etching techniques and fabricate the structure. The pattern has, for example, gate structures of field effect transistors."<br><br>*See*, *e.g.*, Jinbo '222 (translation), at 7:<br><br>"As is clear from the aforementioned explanation, by means of the pattern formation method of the present invention, a first resist pattern is formed once on a substrate, after which the next resist pattern can be formed in the region between this first resist pattern on the substrate; therefore, a fine resist pattern that exceeds the resolution limit (is less than the resolution limit) of the projection exposure device can be formed."<br><br>Accordingly, the pattern formation method of the present invention easily manufactures highly integrated LSIs and the like."<br><br>*See*, *e.g.*, Jinbo '222 (translation), at 2:<br><br>"Projection exposure devices are widely used in the fabrication of semiconductor devices such as ICs and LSIs.<br><br>Conventionally, when a resist pattern is formed using a projection exposure device, a procedure is typically used in which a substrate such as a silicon wafer is coated with a resist, and this resist is exposed with the projection exposure device, after which this resist is developed to obtain the final resist pattern.<br><br>. . .<br><br>In other words, these projection exposure devices are capable of patterning on the order of 0.5 µm, and capable of manufacturing a 16 Mbit DRAM or the like." |
| depositing a second photoresist layer on said material;<br><br>offsetting said periodic pattern by p.sub.min /2;<br><br>repeating said exposing, developing and transferring steps, thereby interpolating new said pattern midway between | *See*, *e.g.*, fig.1: |

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| said pattern. | 11：下地<br>13：第１のレジスト<br>13a:第１のレジストパターン<br>13b:不溶化処理済み第１のレジストパターン<br>15：第２のレジスト<br>15a:第２のレジストパターン<br>17：レジストパターン<br><br>*See*, *e.g*., Jinbo '222 (translation), at 1:<br><br>"1. Pattern formation method characterized by: a step wherein a first resist is formed on a substrate and said first resist is patterned; a step wherein a first resist pattern obtained by the aforementioned patterning is processed and made insoluble with respect to the solvent used for a second resist that is subsequently formed on the aforementioned substrate having said first resist pattern and with respect to the developer fluid used in the subsequent development of said second resist; and a step wherein said second resist is formed on the aforementioned substrate having said first resist pattern for which the insolubilization process has been completed, and said second resist is patterned."<br><br>*See*, *e.g*., Jinbo '222 (translation), at 3:<br><br>"[T]he objective of the present invention is to provide a pattern formation method capable of forming a resist pattern [with a size] at or less than the resolution limit of the projection exposure device. |

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| | Means to solve the problem<br><br>To achieve this objective, the pattern formation method of the present invention is characterized by:<br><br>a step wherein a first resist is formed on a substrate and said first resist is patterned;<br><br>a step wherein a first resist pattern obtained by the aforementioned patterning is processed and made insoluble with respect to the solvent for a second resist that is subsequently formed on the aforementioned substrate having said first resist pattern and with respect to the developer fluid used in the subsequent development of said second resist;<br><br>and a step wherein said second resist is formed on the aforementioned substrate having said first resist pattern for which the insolubilization process has been completed, and said second resist is patterned.<br><br>With respect to the application of the present invention it is preferable that the aforementioned insolubilization process be performed by leaving the substrate having the aforementioned first resist pattern in a plasma containing a fluorine compound gas for which the alkane hydrogen has been replaced with fluorine.<br><br>Furthermore, the substrate referred to herein is an intermediate body or the like of various kinds of substrates, such as a glass substrate, a silicon substrate, or a GaAs substrate, with an insulation film, metal film, or thin film and/or similar elements being formed thereon."<br><br>*See*, *e.g.*, Jinbo '222 (translation), at 5-6:<br><br>"Next, by a spin-coating method, a second resist 15 – in this case, the TSMR-365iR used as the first resist – was applied with a film thickness of 1.0 μm to substrate 11 having the first resist pattern 13b which had undergone insolubilization processing (Figure 1(D).<br><br>As described above, first resist pattern 13b which has undergone insolubilization processing is insoluble with respect to the solvent of second resist 15, so when first resist pattern 13b is covered by second resist pattern 15 the pattern of the first resist pattern itself does not break down, nor does it intermix with the second resist.<br><br>Next, second resist pattern 15 was baked under the same baking conditions as for the first |

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| | resist.<br><br>Next, substrate 11 having this baked second resist was placed on a wafer stage in the previously used projection exposure device, after which substrate 11 was aligned with respect to a mask installed in this projection exposure device. Next, the wafer stage was shifted 0.3 µm in the X direction – in other words, the wafer stage was shifted such that the line potions of the mask were projected on the space portions of first resist pattern 13b, which had undergone insolubilization processing – and then second resist 15 was exposed with an exposure amount of 300 mJ/cm2.<br><br>Next, the exposed second resist was developed under the same developing conditions as for the first resist, obtaining second resist pattern 15a (Figure 1(E)). Because first resist pattern 13b had undergone insolubilization processing as described previously so as to be insoluble with respect to the NMD-W developer fluid, no pattern breakdown occurred when the second resist pattern was developed.<br><br>After the second resist was developed, a resist pattern 17 comprised of insolubilization-processed first resist pattern 13b and second resist pattern 15a was formed on substrate 11 (Figure 1(E)). When this resist pattern 17 was observed with an S-6000 SEM measurement device, it was found that a pattern for which line portions with a width of 0.3 µm were aligned with a pitch of 0.6 µm – in other words, a 0.3 µm line-and-space pattern – had been resolved."<br><br>*See*, *e.g.*, Jinbo '222 (translation), at 7:<br><br>"Furthermore, in the aforementioned embodiment, the same resist was used for the first resist and the second resist, but when necessary they could be different resists.<br><br>Furthermore, the present invention could also be applied so as to make the second resist pattern insoluble with respect to the solvent and developer fluid of a third resist, with the third resist pattern being formed on [the second resist], if necessary."<br><br>See, e.g., Jinbo '222 (translation), at 7:<br><br>"As is clear from the aforementioned explanation, by means of the pattern formation method of the present invention, a first resist pattern is formed once on a substrate, after which the next resist pattern can be formed in the region between this first resist pattern on the substrate; therefore, a fine resist pattern that exceeds the resolution limit (is less than the resolution limit) of the |

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| | projection exposure device can be formed." |
| 10. The method of claim 8, wherein said material includes an SiO.sub.2 overlayer configured to act as a hardmask during said etching step. | See, e.g., Zdebel '002, figs.3 & 4A:<br><br>FIG. 3<br><br>FIG. 4A<br><br>See, e.g., Zdebel '002, C7:20 to C8:22:<br><br>"Two layers 84, 86 are conveniently deposited on surface 69 using low pressure chemical vapor deposition (LPCVD). First layer 84 is a layer of polycrystalline semiconductor, preferably silicon having a thickness conveniently of about 385 nanometers. Larger or smaller thicknesses may be used for layer 84 according to relationships with other layers which will be subsequently explained. Second layer 86 is conveniently a layer of silicon nitride or a sandwich of oxide plus nitride or a layer of other oxidation resistant material having a thickness of, for example, about 70-120 nanometers. Poly silicon layer 84 will be used to form poly silicon base contact regions 84 of FIG. 2. Where an NPN transistor is being formed, layer 84 is doped by ion implantation of, for example, boron. The doping may be performed during or anytime after deposition of layer 84, but is conveniently performed after deposition of layers 84 and 86 through nitride layer 86 and before deposition of layers 88 or 90. Poly silicon layer 84 is conveniently doped with singly ionized boron at an energy of about 70 KeV to a dose of about 1.times.10.sup.16 cm.sup.-2, although other doping levels may also be used depending on the desired device and circuit characteristics. The |

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| | implantation is preferably arranged so that the relatively high dose of boron is located near the upper surface of polycrystalline silicon layer 84, just below silicon nitride 86.<br><br>After the boron implantation, two further layers 88, 90 are deposited, for example by LPCVD, over silicon nitride layer 86. Layer 88 is desirably an undoped layer of polycrystalline silicon having a thickness conveniently of about 180 nanometers. Larger or smaller thicknesses may be used for layer 88, taking into account the thickness of other layers, as will be subsequently explained. Layer 90 is formed overlying poly layer 88. Layer 90 conveniently prevents contamination of poly layer 88 and serves as a hard mask for subsequent lithographic patterning of the underlying layers. Layer 90 may be of any material suitable for such purposes. Layer 90 is conveniently of silicon oxide having a thickness of about 20-40 nanometers.<br><br>Processing of the structure continues with the application of layer 92 of photoresist overlying oxide layer 90 as shown schematically in FIG. 4A. The photoresist is patterned using master mask 94, represented by the shaded region in FIG. 4B, containing images 95-99 for locating various device regions. Master mask 94 provides self-alignment of the critical device areas, for example in the case of the vertical NPN transistor, the collector contact, the base contact or contacts, the emitter contact, and the emitter-base active region. In accordance with one embodiment of the invention, master mask 94 defines the master electrode area which includes emitter contact opening 95, collector contact opening 96, and base contact openings 97, 98 located within perimeter 9 and surrounded by external region 99. Region 99 identifies the region, outside perimeter 9 of master mask 94. Openings or windows 95-98 located within perimeters 5-8 respectively are used in the subsequent process to form the "footprints" of the device terminals, and in the case of the vertical bipolar device, the active emitter-base region. Perimeter 5, although referred to generally herein as the emitter opening or emitter contact opening, is used in conjunction with epitaxial island 82 formed within field oxide 71 to locate both the base and emitter of the device as well as the emitter contact. Variations and further embodiments, in addition to the basic NPN transistor, are discussed later. Base contact openings 97, 98 are located within perimeters 7, 8 respectively. Collector contact opening 96 is located within perimeter 6."<br><br>See, e.g., <u>Cuthbert '076</u>, figs.2 & 3: |

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| | FIG. 2 9 7 5 3 3 1<br><br>FIG. 3 9 7 5 3 3 1<br><br>See, e.g., Cuthbert '076, C2:66 to C3:25:<br><br>“A layer of spin-on-glass(SOG) 7 and a layer of photoresist 9 are now deposited to form the structure depicted in FIG. 2. The term "spin-on-glass" is well known to those skilled in the art and need not be defined. As can be seen, the SOG has a relatively planar surface and has smoothed out the topography of the underlying substrate. By relatively planar, it is meant that the surface is locally planar, although the surface may not be planar over the entire substrate surface. The SOG is put on with conventional techniques. The planarity of the surface depends upon the topography of the underlying material and the thickness of the SOG layer. Those skilled in the art will readily select a thickness for the SOG that is sufficient for it to act as an etch mask for the underlying gate. A thermal treatment or cure is desirably used to densify and flow the SOG. This process step also reduces the topography of the SOG and reduces variations in the resist layer thickness.<br><br>Lithographic techniques are now used to pattern the photoresist. The photoresist is then used as a mask for the etching of the SOG. The etching desirably produces vertical sidewalls in the SOG. |

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| | The resulting structure is depicted in FIG. 3. Those skilled in the art will readily select appropriate etching techniques and fabricate the structure. The pattern has, for example, gate structures of field effect transistors."<br><br>*See*, *e.g*., Jinbo '222 (translation), fig.1:<br><br>11：下地<br>13：第１のレジスト<br>13a：第１のレジストパターン<br>13b：不溶化処理済み第１のレジストパターン<br>15：第２のレジスト<br>15a：第２のレジストパターン<br>17：レジストパターン |
| 11. The method of claim 8, wherein said step of depositing a photoresist includes depositing at least one of a negative photoresist, a positive photoresist and a positive photoresist with an image reversal step. | *See*, *e.g*., Jinbo '222 (translation), at 7:<br><br>"For example, with the aforementioned embodiment, TSMR-365iR was used as the resist, but the resist used with the present invention is not limited thereto; other resists (regardless of whether it is a negative resist or positive resist) are acceptable. However, when the insolubilization process is performed with a gas plasma that includes a fluorine compound gas for which the alkane hydrogen had been replaced with fluorine gas, it is preferable that the resist be a so-called novolac resist (both positive and negative resists are acceptable), because the effect of the insolubilization process can be clearly obtained." |

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| | *See*, *e.g.*, Jinbo '222 (translation), at 7:<br><br>"Furthermore, in the aforementioned embodiment, the same resist was used for the first resist and the second resist, but when necessary they could be different resists.<br><br>Furthermore, the present invention could also be applied so as to make the second resist pattern insoluble with respect to the solvent and developer fluid of a third resist, with the third resist pattern being formed on [the second resist], if necessary."<br><br>*See*, *e.g.*, fig.1:<br><br>11：下地<br>13：第1のレジスト<br>13a：第1のレジストパターン<br>13b：不溶化処理済み第1のレジストパターン<br>15：第2のレジスト<br>15a：第2のレジストパターン<br>17：レジストパターン |
| 16. The method of claim 8, wherein said step of developing said periodic pattern includes etching said pattern into a hardmask. | *See*, *e.g.*, Zdebel '002, figs.3 & 4A: |

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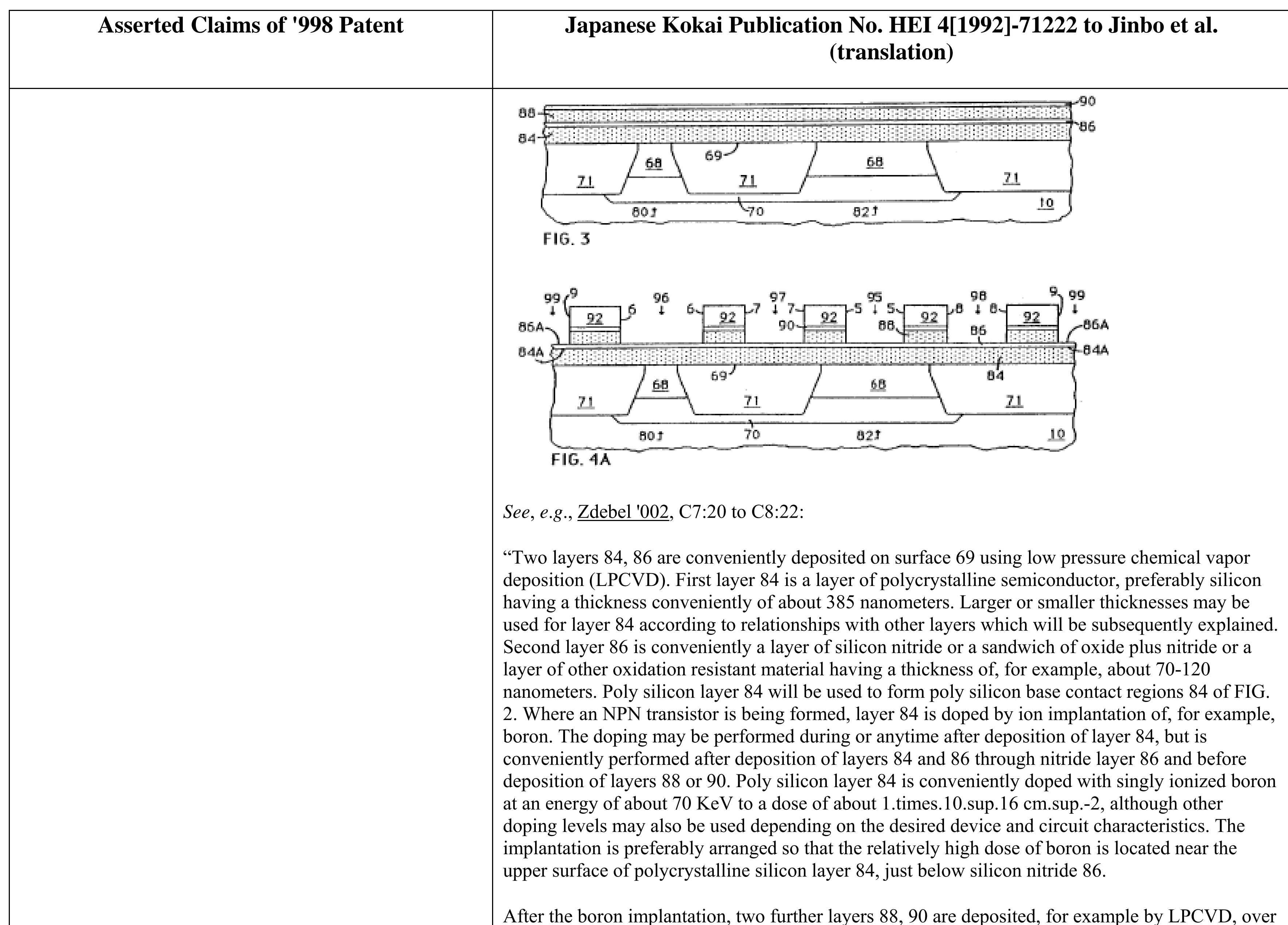
| | <br>FIG. 3<br>FIG. 4A<br><br>*See*, *e.g.*, Zdebel '002, C7:20 to C8:22:<br><br>"Two layers 84, 86 are conveniently deposited on surface 69 using low pressure chemical vapor deposition (LPCVD). First layer 84 is a layer of polycrystalline semiconductor, preferably silicon having a thickness conveniently of about 385 nanometers. Larger or smaller thicknesses may be used for layer 84 according to relationships with other layers which will be subsequently explained. Second layer 86 is conveniently a layer of silicon nitride or a sandwich of oxide plus nitride or a layer of other oxidation resistant material having a thickness of, for example, about 70-120 nanometers. Poly silicon layer 84 will be used to form poly silicon base contact regions 84 of FIG. 2. Where an NPN transistor is being formed, layer 84 is doped by ion implantation of, for example, boron. The doping may be performed during or anytime after deposition of layer 84, but is conveniently performed after deposition of layers 84 and 86 through nitride layer 86 and before deposition of layers 88 or 90. Poly silicon layer 84 is conveniently doped with singly ionized boron at an energy of about 70 KeV to a dose of about 1.times.10.sup.16 cm.sup.-2, although other doping levels may also be used depending on the desired device and circuit characteristics. The implantation is preferably arranged so that the relatively high dose of boron is located near the upper surface of polycrystalline silicon layer 84, just below silicon nitride 86.<br><br>After the boron implantation, two further layers 88, 90 are deposited, for example by LPCVD, over |

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| | silicon nitride layer 86. Layer 88 is desirably an undoped layer of polycrystalline silicon having a thickness conveniently of about 180 nanometers. Larger or smaller thicknesses may be used for layer 88, taking into account the thickness of other layers, as will be subsequently explained. Layer 90 is formed overlying poly layer 88. Layer 90 conveniently prevents contamination of poly layer 88 and serves as a hard mask for subsequent lithographic patterning of the underlying layers. Layer 90 may be of any material suitable for such purposes. Layer 90 is conveniently of silicon oxide having a thickness of about 20-40 nanometers.<br><br>Processing of the structure continues with the application of layer 92 of photoresist overlying oxide layer 90 as shown schematically in FIG. 4A. The photoresist is patterned using master mask 94, represented by the shaded region in FIG. 4B, containing images 95-99 for locating various device regions. Master mask 94 provides self-alignment of the critical device areas, for example in the case of the vertical NPN transistor, the collector contact, the base contact or contacts, the emitter contact, and the emitter-base active region. In accordance with one embodiment of the invention, master mask 94 defines the master electrode area which includes emitter contact opening 95, collector contact opening 96, and base contact openings 97, 98 located within perimeter 9 and surrounded by external region 99. Region 99 identifies the region, outside perimeter 9 of master mask 94. Openings or windows 95-98 located within perimeters 5-8 respectively are used in the subsequent process to form the "footprints" of the device terminals, and in the case of the vertical bipolar device, the active emitter-base region. Perimeter 5, although referred to generally herein as the emitter opening or emitter contact opening, is used in conjunction with epitaxial island 82 formed within field oxide 71 to locate both the base and emitter of the device as well as the emitter contact. Variations and further embodiments, in addition to the basic NPN transistor, are discussed later. Base contact openings 97, 98 are located within perimeters 7, 8 respectively. Collector contact opening 96 is located within perimeter 6."<br><br>*See*, *e.g*., Cuthbert '076, figs.2 & 3: |

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| | FIG. 2 <br> FIG. 3 <br><br> *See*, *e.g.*, Cuthbert '076, C2:66 to C3:25: <br><br> "A layer of spin-on-glass(SOG) 7 and a layer of photoresist 9 are now deposited to form the structure depicted in FIG. 2. The term "spin-on-glass" is well known to those skilled in the art and need not be defined. As can be seen, the SOG has a relatively planar surface and has smoothed out the topography of the underlying substrate. By relatively planar, it is meant that the surface is locally planar, although the surface may not be planar over the entire substrate surface. The SOG is put on with conventional techniques. The planarity of the surface depends upon the topography of the underlying material and the thickness of the SOG layer. Those skilled in the art will readily select a thickness for the SOG that is sufficient for it to act as an etch mask for the underlying gate. A thermal treatment or cure is desirably used to densify and flow the SOG. This process step also reduces the topography of the SOG and reduces variations in the resist layer thickness. <br><br> Lithographic techniques are now used to pattern the photoresist. The photoresist is then used as a mask for the etching of the SOG. The etching desirably produces vertical sidewalls in the SOG. |

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| | The resulting structure is depicted in FIG. 3. Those skilled in the art will readily select appropriate etching techniques and fabricate the structure. The pattern has, for example, gate structures of field effect transistors."<br><br>*See*, *e.g.*, Jinbo '222 (translation), fig.1: |
| 18. The method of claim 8, wherein said step of depositing a material includes depositing a material on at least one of a textured substrate, a quantum structure, a flux pinning site for high-T.sub.c superconductors, a birefringent material, a reflective optical coating, a photonic bandgap, an electronic device, an optical storage media, a magnetic storage media, an array of field emitters and a Dynamic Random Access Memory capacitor. | *See*, *e.g.*, Jinbo '222 (translation), at 2:<br><br>"Projection exposure devices are widely used in the fabrication of semiconductor devices such as ICs and LSIs.<br><br>Conventionally, when a resist pattern is formed using a projection exposure device, a procedure is typically used in which a substrate such as a silicon wafer is coated with a resist, and this resist is exposed with the projection exposure device, after which this resist is developed to obtain the final resist pattern. |

| Asserted Claims of '998 Patent | Japanese Kokai Publication No. HEI 4[1992]-71222 to Jinbo et al. (translation) |
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| | . . .<br><br>In other words, these projection exposure devices are capable of patterning on the order of 0.5 µm, and capable of manufacturing a 16 Mbit DRAM or the like." |

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