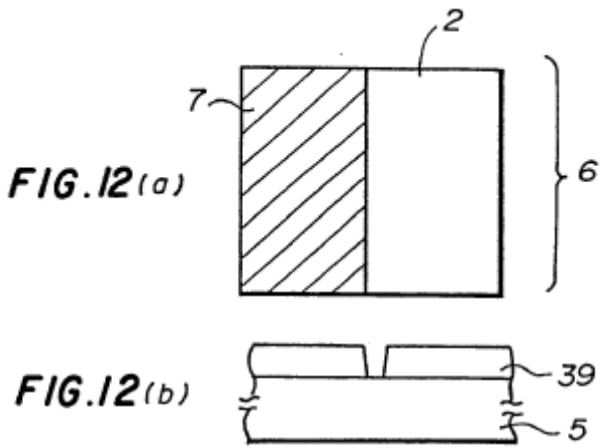
STC.UNM v. Intel Corporation

Exhibit 2

STC.UNM v. Intel

Invalidity Claim Chart Comparing '998 Patent to Nakagawa '716, Zdebel '002, and Cuthbert '076

The following asserted claims of STC.UNM's U.S. Pat. No. 6,042,998 are invalidated pursuant to 35 U.S.C. § 102 and/or § 103, alone or in combination with other references, by the prior art references U.S. Patent No. 5,364,716 to Nakagawa et al., entitled "Pattern Exposing Method Using Phase Shift and Mask Used Therefor," issued on Nov. 15, 1994, filed on Sept. 3, 1994, and claiming a foreign priority date of Sept. 27, 1991 ("Nakagawa '716"), U.S. Patent No. 5,067,002 to Zdebel et al., entitled "Integrated Circuit Structures Having Polycrystalline Electrode Contacts," issued on Nov. 19, 1991 ("Zdebel '002"), and U.S. Patent No. 5,264,076 to Cuthbert et al., entitled "Integrated Circuit Process Using a 'Hard Mask'," issued on Nov. 23, 1993, filed on Dec. 17, 1992 ("Cuthbert '076"). These preliminary invalidity contentions are based on information currently known to Intel, and, as a result, apply interpretations apparently or potentially adopted by STC.UNM. Intel reserves the right to amend its preliminary invalidity contentions in light of developments in the case such as production of discovery, identification of additional prior art, and issuance of an order following any Claim Construction Hearing, as stated in the Scheduling Order (Dkt. 47, dated March 2, 2011).

Asserted Claims of '998 Patent	Nakagawa '716, Zdebel '002, and Cuthbert '076
6. A method for obtaining a pattern wherein the Fourier transform of said pattern contains high spatial frequencies by combining nonlinear functions of intensity of at least two exposures combined with at least one nonlinear processing step intermediate between the two exposures to form three dimensional patterns comprising the steps of:	*See, e.g.*, Nakagawa '716, figs.12(a)-12(e): 

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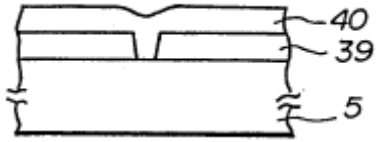
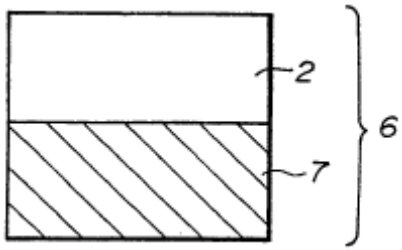
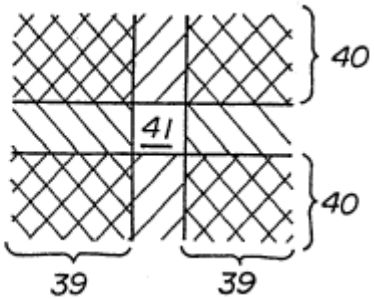
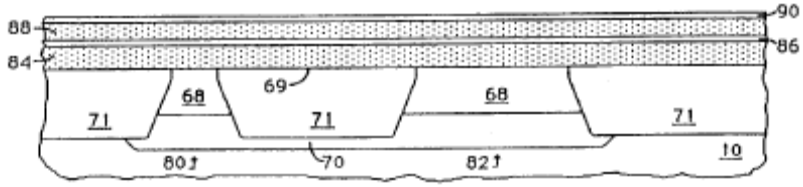
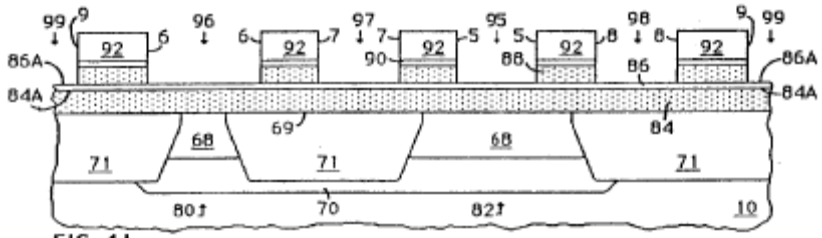
Asserted Claims of '998 Patent	Nakagawa '716, Zdebel '002, and Cuthbert '076
	FIG.12(c)  FIG.12(d)  FIG.12(e)  *See, e.g.*, Nakagawa '716, C8:59 to C9:47: "Next, a description will be given of a fourth embodiment of the pattern exposing method according to the present invention, by referring to FIG. 12. In this embodiment, a resist pattern is formed for use in forming an extremely fine hole of the semiconductor device. More particularly, this embodiment uses the phase shift reticle 6 to form on a negative resist a resist pattern having a fine rectangular hole. FIG. 12(a) shows a plan view of the phase shift reticle 6 which has the phase shift layer 7 formed on the glass substrate 2. This phase shift reticle 6 may be the phase shift reticle 6 shown in FIG. 4, for example.

Asserted Claims of '998 Patent	Nakagawa '716, Zdebel '002, and Cuthbert '076
	In FIG. 12(b) which shows a partial cross section of the wafer 5, a negative resist 39 is formed on the wafer 5 and a first demagnification projection exposure is made using the phase shift reticle 6 shown in FIG. 12(a). The negative resist 39 is developed after the first exposure, and a fine space pattern shown in FIG. 12(b) is formed in the negative resist 39 by the edge pattern of the phase shift layer 7 of the phase shift reticle 6 shown in FIG. 12(a). Then, a negative resist 40 is formed on the entire top surface of the wafer 5 as shown in FIG. 12(c). Next, a phase shift reticle 6 shown in FIG. 12(d) having a pattern which is rotated by 90.degree. with respect to the phase shift reticle shown in FIG. 12(a) is used to make a second demagnification projection exposure. By developing the negative resist 40 after the second exposure, a fine space pattern is formed in the negative resist 40 by the edge pattern of the phase shift layer 7 of the phase shift reticle 6 shown in FIG. 12(d) . As a result, the fine space pattern formed in the negative resist 39 and the fine space pattern formed in the negative resist 40 intersect perpendicularly to each other, and a fine rectangular hole 41 shown in FIG. 12(e) is formed at the intersection. For example, if the exposure light is the i-line and the numerical aperture of the optical system is 0.5, it is possible to make each side of the fine rectangular hole 41 approximately 0.2 .mu.m. Therefore, by enabling the formation of such a fine hole, it becomes possible to further improve the integration density of semiconductor devices. According to this embodiment, it is possible to sharpen the negative peak of the light intensity distribution on the resist by using the phase shift reticles 6 and making the first and second exposures. In other words, the line-and-space having a satisfactory resolution and contrast in the X direction and the line-and-space having a satisfactory resolution and contrast in the Y direction are formed by two independent exposures, and it is possible to form at the intersection of the two line-and-spaces a fine rectangular hole which cannot be formed by the existing technique using only one exposure. Therefore, the fine rectangular hole which is formed has sharp edges and the corners of the hole do not become rounded." The phrase "the Fourier transform of said pattern contains high spatial frequencies" is an inherent result of the nonlinear processing step. Also, Admitted Prior Art in the '998 patent itself, Brueck '835, Waldo '094, Ziger, Gwozdz, and Elliott[1] each discloses nonlinear processing, e.g., as

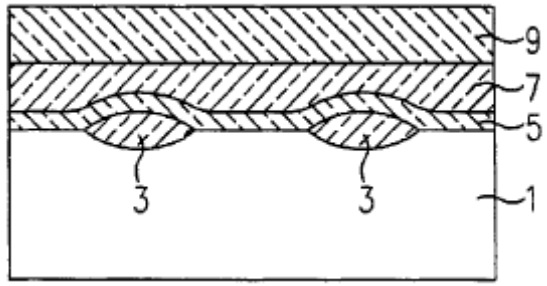
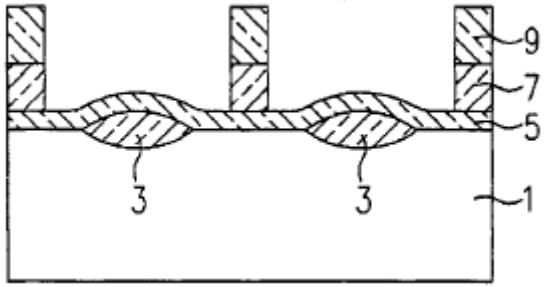
[1] U.S. Patent No. 5,415,835 to Brueck et al. ("Brueck '835"), U.S. Patent No. 4,891,094 to Waldo III ("Waldo '094"), David H. Ziger, et al., *Generalized Approach Toward Modeling Resist Performance*, ALCHE JOURNAL, Vol. 37, No. 12, Dec. 1991, at 1863-74 ("Ziger"), Peter S. Gwozdz, *Positive Versus Negative: A Photoresist*

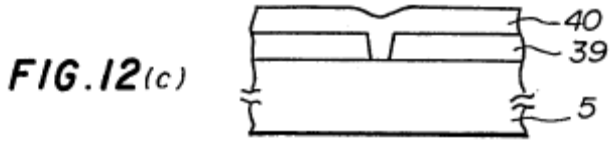
Asserted Claims of '998 Patent	Nakagawa '716, Zdebel '002, and Cuthbert '076
	explained in "Invalidity Claim Chart Comparing '998 Patent to AAPA, Brueck '835, Waldo '094, Ziger, Gwozdz, and Elliott," served concurrently herewith.
coating a substrate with a first mask material and a first photoresist layer; exposing said first photoresist layer with a first exposure developing said photoresist to form a first pattern in said first photoresist layer, said first pattern containing spatial frequencies greater than those in a two dimensional optical intensity image imposed onto said photoresist layer in said first exposure as a result of a nonlinear response of said first photoresist layer;	*See, e.g.*, Nakagawa '716, fig.12(b): *See, e.g.*, Nakagawa '716, C9:2-11: "In FIG. 12(b) which shows a partial cross section of the wafer 5, a negative resist 39 is formed on the wafer 5 and a first demagnification projection exposure is made using the phase shift reticle 6 shown in FIG. 12(a). The negative resist 39 is developed after the first exposure, and a fine space pattern shown in FIG. 12(b) is formed in the negative resist 39 by the edge pattern of the phase shift layer 7 of the phase shift reticle 6 shown in FIG. 12(a)." *See, e.g.*, Nakagawa '716, C13:16-30: "Therefore, according to the fourth through ninth embodiments, it is possible to form an extremely fine hole which exceeds the resolution limit of the imaging optical system and could not be formed by the conventional techniques. The contrast is particularly good according to these embodiments, because one resist layer is formed exclusively for each exposure. In other words, if a single resist layer were subjected to both the first and second exposures, the contrast of the hole which is formed would deteriorate by approximately 50%, and the edges of the formed hole would become rounded. However, such a contrast deterioration will not occur according to these embodiments, and it is possible to form a fine hole having the designed shape with a high accuracy." The phrase "containing spatial frequencies greater than those in a two dimensional optical intensity image imposed onto said photoresist layer . . . as a result of a nonlinear response of said [photoresist layer]" is inherently disclosed in the above-cited disclosure of photoresist. Also, Admitted Prior Art in the '998 patent itself, Brueck '835, Waldo '094, Ziger, Gwozdz, and Elliott each discloses the nonlinear response of photoresist, e.g., as explained in "Invalidity Claim Chart Comparing '998 Patent to AAPA, Brueck '835, Waldo '094, Ziger, Gwozdz, and Elliott," served

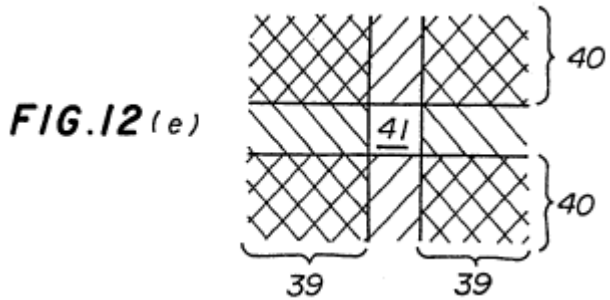
Analysis, SEMICONDUCTOR LITHOGRAPHY VI, SPIE Vol. 275, 1981 ("Gwozdz"), and/or David J. Elliott, INTEGRATED CIRCUIT FABRICATION TECHNOLOGY, 2d ed., 1989, at 85-106 and 326 ("Elliott").

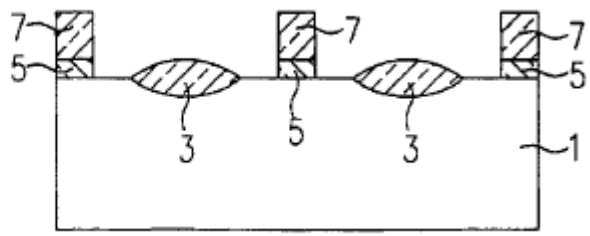
Asserted Claims of '998 Patent	Nakagawa '716, Zdebel '002, and Cuthbert '076
	concurrently herewith.
transferring said first pattern into said first mask material, said first mask material comprising at least one of SiO.sub.2, Si.sub.3 N.sub.4, a metal, a polysilicon and a polymer;	*See, e.g.*, Zdebel '002, figs.3 & 4A:  FIG. 3  FIG. 4A *See, e.g.*, Zdebel '002, C7:20 to C8:22: "Two layers 84, 86 are conveniently deposited on surface 69 using low pressure chemical vapor deposition (LPCVD). First layer 84 is a layer of polycrystalline semiconductor, preferably silicon having a thickness conveniently of about 385 nanometers. Larger or smaller thicknesses may be used for layer 84 according to relationships with other layers which will be subsequently explained. Second layer 86 is conveniently a layer of silicon nitride or a sandwich of oxide plus nitride or a layer of other oxidation resistant material having a thickness of, for example, about 70-120 nanometers. Poly silicon layer 84 will be used to form poly silicon base contact regions 84 of FIG. 2. Where an NPN transistor is being formed, layer 84 is doped by ion implantation of, for example, boron. The doping may be performed during or anytime after deposition of layer 84, but is conveniently performed after deposition of layers 84 and 86 through nitride layer 86 and before deposition of layers 88 or 90. Poly silicon layer 84 is conveniently doped with singly ionized boron at an energy of about 70 KeV to a dose of about 1.times.10.sup.16 cm.sup.-2, although other doping levels may also be used depending on the desired device and circuit characteristics. The implantation is preferably arranged so that the relatively high dose of boron is located near the

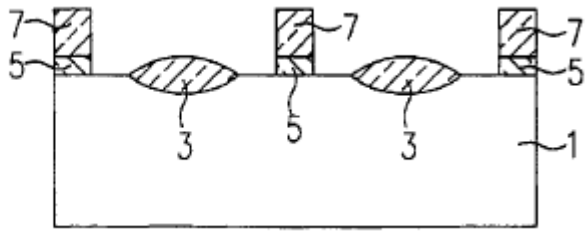
Asserted Claims of '998 Patent	Nakagawa '716, Zdebel '002, and Cuthbert '076
	upper surface of polycrystalline silicon layer 84, just below silicon nitride 86. After the boron implantation, two further layers 88, 90 are deposited, for example by LPCVD, over silicon nitride layer 86. Layer 88 is desirably an undoped layer of polycrystalline silicon having a thickness conveniently of about 180 nanometers. Larger or smaller thicknesses may be used for layer 88, taking into account the thickness of other layers, as will be subsequently explained. Layer 90 is formed overlying poly layer 88. Layer 90 conveniently prevents contamination of poly layer 88 and serves as a hard mask for subsequent lithographic patterning of the underlying layers. Layer 90 may be of any material suitable for such purposes. Layer 90 is conveniently of silicon oxide having a thickness of about 20-40 nanometers. Processing of the structure continues with the application of layer 92 of photoresist overlying oxide layer 90 as shown schematically in FIG. 4A. The photoresist is patterned using master mask 94, represented by the shaded region in FIG. 4B, containing images 95-99 for locating various device regions. Master mask 94 provides self-alignment of the critical device areas, for example in the case of the vertical NPN transistor, the collector contact, the base contact or contacts, the emitter contact, and the emitter-base active region. In accordance with one embodiment of the invention, master mask 94 defines the master electrode area which includes emitter contact opening 95, collector contact opening 96, and base contact openings 97, 98 located within perimeter 9 and surrounded by external region 99. Region 99 identifies the region, outside perimeter 9 of master mask 94. Openings or windows 95-98 located within perimeters 5-8 respectively are used in the subsequent process to form the "footprints" of the device terminals, and in the case of the vertical bipolar device, the active emitter-base region. Perimeter 5, although referred to generally herein as the emitter opening or emitter contact opening, is used in conjunction with epitaxial island 82 formed within field oxide 71 to locate both the base and emitter of the device as well as the emitter contact. Variations and further embodiments, in addition to the basic NPN transistor, are discussed later. Base contact openings 97, 98 are located within perimeters 7, 8 respectively. Collector contact opening 96 is located within perimeter 6." *See, e.g.*, Cuthbert '076, figs.2 & 3:

Asserted Claims of '998 Patent	Nakagawa '716, Zdebel '002, and Cuthbert '076
	FIG. 2  FIG. 3  *See, e.g.*, Cuthbert '076, C2:66 to C3:25: "A layer of spin-on-glass(SOG) 7 and a layer of photoresist 9 are now deposited to form the structure depicted in FIG. 2. The term "spin-on-glass" is well known to those skilled in the art and need not be defined. As can be seen, the SOG has a relatively planar surface and has smoothed out the topography of the underlying substrate. By relatively planar, it is meant that the surface is locally planar, although the surface may not be planar over the entire substrate surface. The SOG is put on with conventional techniques. The planarity of the surface depends upon the topography of the underlying material and the thickness of the SOG layer. Those skilled in the art will readily select a thickness for the SOG that is sufficient for it to act as an etch mask for the underlying gate. A thermal treatment or cure is desirably used to densify and flow the SOG. This process step also reduces the topography of the SOG and reduces variations in the resist layer thickness. Lithographic techniques are now used to pattern the photoresist. The photoresist is then used as a mask for the etching of the SOG. The etching desirably produces vertical sidewalls in the SOG. The resulting structure is depicted in FIG. 3. Those skilled in the art will readily select appropriate etching techniques and fabricate the structure. The pattern has, for example, gate structures of field

Asserted Claims of '998 Patent	Nakagawa '716, Zdebel '002, and Cuthbert '076
	effect transistors."
coating said substrate with a second photoresist; exposing said second photoresist with a second exposure developing said second photoresist layer to form a second pattern in said second photoresist layer, said second pattern containing spatial frequencies greater than those in a two dimensional optical intensity image imposed onto said photoresist layer in said second exposure as a result of a nonlinear response of said second photoresist layer;	*See, e.g.*, Nakagawa '716, fig.12(c):  *See, e.g.*, Nakagawa '716, C9:12-21: "Then, a negative resist 40 is formed on the entire top surface of the wafer 5 as shown in FIG. 12(c). Next, a phase shift reticle 6 shown in FIG. 12(d) having a pattern which is rotated by 90.degree. with respect to the phase shift reticle shown in FIG. 12(a) is used to make a second demagnification projection exposure. By developing the negative resist 40 after the second exposure, a fine space pattern is formed in the negative resist 40 by the edge pattern of the phase shift layer 7 of the phase shift reticle 6 shown in FIG. 12(d) ." *See, e.g.*, Nakagawa '716, C13:16-30: "Therefore, according to the fourth through ninth embodiments, it is possible to form an extremely fine hole which exceeds the resolution limit of the imaging optical system and could not be formed by the conventional techniques. The contrast is particularly good according to these embodiments, because one resist layer is formed exclusively for each exposure. In other words, if a single resist layer were subjected to both the first and second exposures, the contrast of the hole which is formed would deteriorate by approximately 50%, and the edges of the formed hole would become rounded. However, such a contrast deterioration will not occur according to these embodiments, and it is possible to form a fine hole having the designed shape with a high accuracy." The phrase "containing spatial frequencies greater than those in a two dimensional optical intensity image imposed onto said photoresist layer . . . as a result of a nonlinear response of said [photoresist layer]" is inherently disclosed in the above-cited disclosure of photoresist. Also, Admitted Prior Art in the '998 patent itself, Brueck '835, Waldo '094, Ziger, Gwozdz, and Elliott each discloses the nonlinear response of photoresist, e.g., as explained in "Invalidity Claim Chart Comparing '998 Patent to AAPA, Brueck '835, Waldo '094, Ziger, Gwozdz, and Elliott," served

Asserted Claims of '998 Patent	Nakagawa '716, Zdebel '002, and Cuthbert '076
	concurrently herewith.
transferring said first pattern and said second pattern into said substrate using a combined mask including parts of said first mask layer and said second photoresist;	*See, e.g.*, Nakagawa '716, fig.12(e):  *See, e.g.*, Nakagawa '716, C9:22-47: "As a result, the fine space pattern formed in the negative resist 39 and the fine space pattern formed in the negative resist 40 intersect perpendicularly to each other, and a fine rectangular hole 41 shown in FIG. 12(e) is formed at the intersection. For example, if the exposure light is the i-line and the numerical aperture of the optical system is 0.5, it is possible to make each side of the fine rectangular hole 41 approximately 0.2 .mu.m. Therefore, by enabling the formation of such a fine hole, it becomes possible to further improve the integration density of semiconductor devices. According to this embodiment, it is possible to sharpen the negative peak of the light intensity distribution on the resist by using the phase shift reticles 6 and making the first and second exposures. In other words, the line-and-space having a satisfactory resolution and contrast in the X direction and the line-and-space having a satisfactory resolution and contrast in the Y direction are formed by two independent exposures, and it is possible to form at the intersection of the two line-and-spaces a fine rectangular hole which cannot be formed by the existing technique using only one exposure. Therefore, the fine rectangular hole which is formed has sharp edges and the corners of the hole do not become rounded."
removing said first mask material and said second photoresist.	*See, e.g.*, Zdebel '002, C9:50-57: "Subsequently, photoresist 100 is removed with, for example, organic photoresist stripper, oxygen plasma, or other suitable means. Thereafter the remainder of oxide layer 90 is removed by, for

Asserted Claims of '998 Patent	Nakagawa '716, Zdebel '002, and Cuthbert '076
	example, dip etching in a dilute hydrofluoric acid etchant solution. Other suitable etching or removal techniques known in the art may also be used." *See, e.g.*, Cuthbert '076, C3:26 to C4:2: "The photoresist is now removed. Conventional techniques may be used. The underlying polysilicon of layer is now etched using the SOG as an etch mask. After the polysilicon has been etched, the SOG is removed using, for example, an HF solution. Such a removal process may be used because of the relative etch rates of SOG to thermal oxide. Depending upon the precise technique used to cure the SOG, etch rate differentials of 15:1 or greater may be obtained. The high etch rates differential makes it possible to remove the SOG without a significant attack on either the gate (thermal) or field oxides. The resulting structure is depicted in FIG. 4." *See, e.g.*, Cuthbert '076, fig.4: FIG. 4 
7. The method of claim 6 wherein said transferring step includes at least one of etching, deposition and-lift off, and damascene.	*See, e.g.*, Zdebel '002, C9:50-57: "Subsequently, photoresist 100 is removed with, for example, organic photoresist stripper, oxygen plasma, or other suitable means. Thereafter the remainder of oxide layer 90 is removed by, for example, dip etching in a dilute hydrofluoric acid etchant solution. Other suitable etching or removal techniques known in the art may also be used." *See, e.g.*, Cuthbert '076, C2:66 to C3:25: "A layer of spin-on-glass(SOG) 7 and a layer of photoresist 9 are now deposited to form the structure depicted in FIG. 2. The term "spin-on-glass" is well known to those skilled in the art and need not be defined. As can be seen, the SOG has a relatively planar surface and has smoothed out the topography of the underlying substrate. By relatively planar, it is meant that the surface is locally planar, although the surface may not be planar over the entire substrate surface. The SOG is put on with conventional techniques. The planarity of the surface depends upon the topography of

Asserted Claims of '998 Patent	Nakagawa '716, Zdebel '002, and Cuthbert '076
	the underlying material and the thickness of the SOG layer. Those skilled in the art will readily select a thickness for the SOG that is sufficient for it to act as an etch mask for the underlying gate. A thermal treatment or cure is desirably used to densify and flow the SOG. This process step also reduces the topography of the SOG and reduces variations in the resist layer thickness. Lithographic techniques are now used to pattern the photoresist. The photoresist is then used as a mask for the etching of the SOG. The etching desirably produces vertical sidewalls in the SOG. The resulting structure is depicted in FIG. 3. Those skilled in the art will readily select appropriate etching techniques and fabricate the structure. The pattern has, for example, gate structures of field effect transistors." *See, e.g.*, Cuthbert '076, C3:26 to C4:2: "The photoresist is now removed. Conventional techniques may be used. The underlying polysilicon of layer is now etched using the SOG as an etch mask. After the polysilicon has been etched, the SOG is removed using, for example, an HF solution. Such a removal process may be used because of the relative etch rates of SOG to thermal oxide. Depending upon the precise technique used to cure the SOG, etch rate differentials of 15:1 or greater may be obtained. The high etch rates differential makes it possible to remove the SOG without a significant attack on either the gate (thermal) or field oxides. The resulting structure is depicted in FIG. 4." *See, e.g.*, Cuthbert '076, fig.4: FIG. 4 

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