STC.UNM v. Intel Corporation
Doc. 55 Att. 4

Exhibit D

Excerpts from
Lithography 2009, Overview of Opportunities, Y. Borodovsky

Dockets.Justia.com

Lithography 2009
Overview of Opportunities

Yan Borodovsky

Intel Sr.Fellow

Portland Technology Development

Intel Corp.

Moore's Law– 2009-2011

Intel 22nm Node - 2011 HVM

- 193 Immersion is the only HVM worthy option available to pattern CL during 2009-2010 Development.
- Advancements in Tooling, Computational Lithography, Materials and Mask Making made Patterning Logic possible with Single Exposure around k_1~0.30 for 0.50x area density scaling
- 22nm Logic node Development at Intel in full swing for 2011 HVM, thus …..

Moore's Law in Action – 2009-2011

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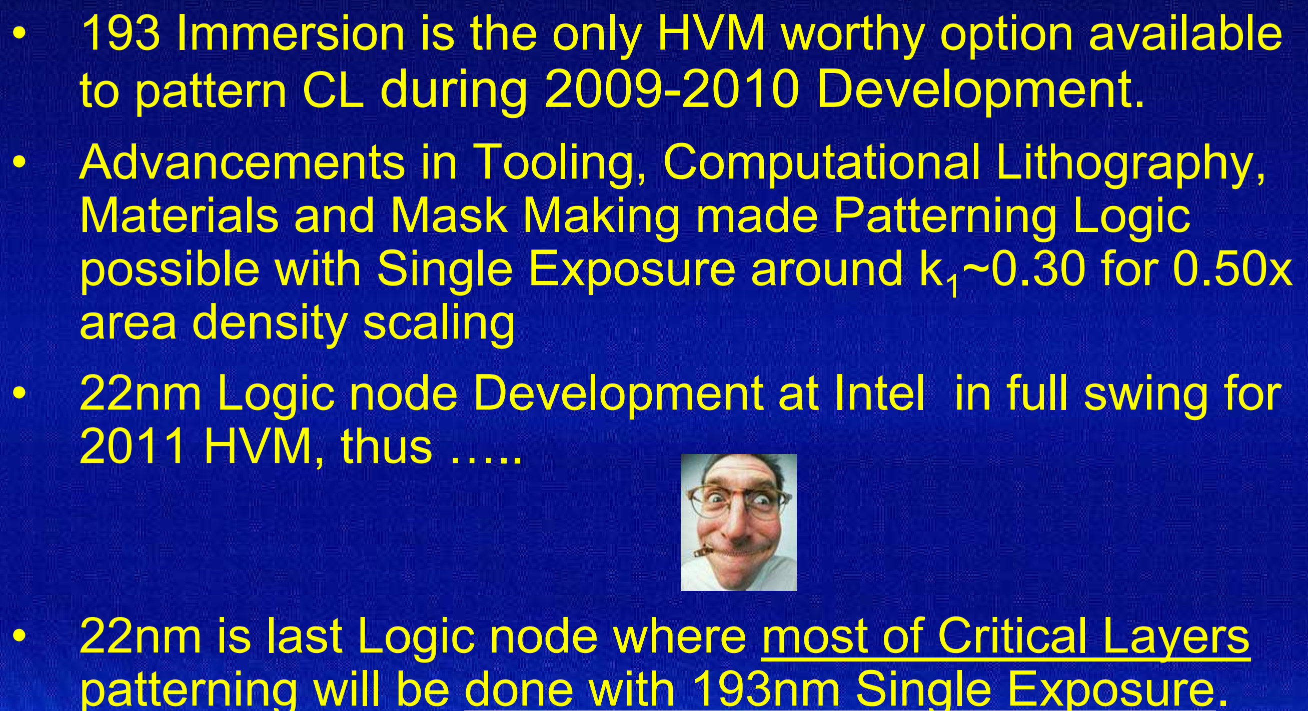

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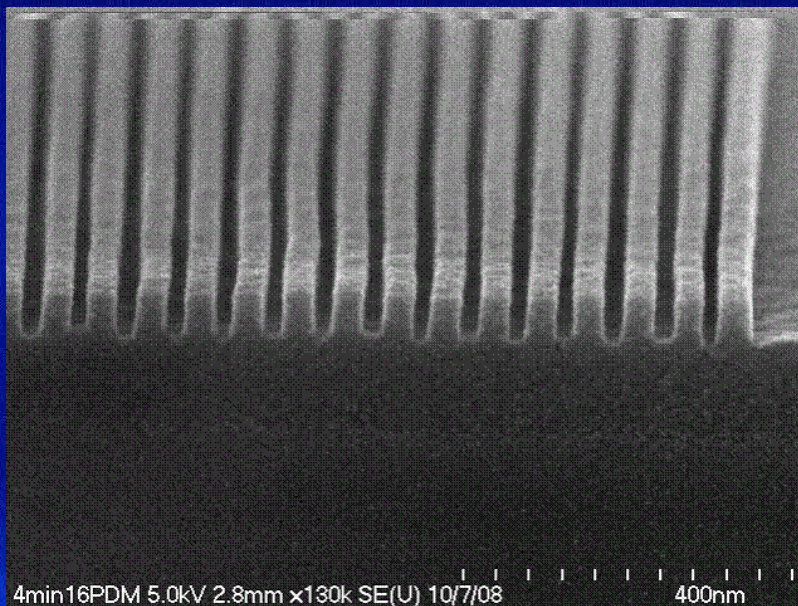
- 22nm is last Logic node where most of Critical Layers patterning will be done with 193nm Single Exposure.

Congratulations!!!

Congratulations to all who worked hard to extend Optical Litho to its ultimate limits!

Intel's 15nm Node - 2013 HVM

193i with Pitch Division (PD) is the only Option available in 2009 and 2010 to support patterning for 15nm Logic (Pitch~112.5*0.5) DRs definition for 2011-2012 Development.



It works!

This makes 193i with PD default approach for 15nm Logic 2013 HVM.

Multiple PD methods under study for best density, wafer cost and design productivity co-optimization

Intel’s 11nm Node - 2015 HVM

	32nm		22nm		15nm		11nm
Min Pitch	112.5nm	*0.71		*0.71		*0.71	= 40nm

Still Single Pitch Division,
might need 3 masks for complex dense 2D layouts.

Intel's 11nm Node - 2015 HVM

193i with Pitch Division can and will be extended as viable option for Intel's 11nm Node patterning in 2015

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***ITRS 2008 Reference*:**

Year of Production	2013	2015	2017	2019	2021
MPU Metal 1 Pitch *nm*	64	50	40	31.8	25.2