Exhibit E

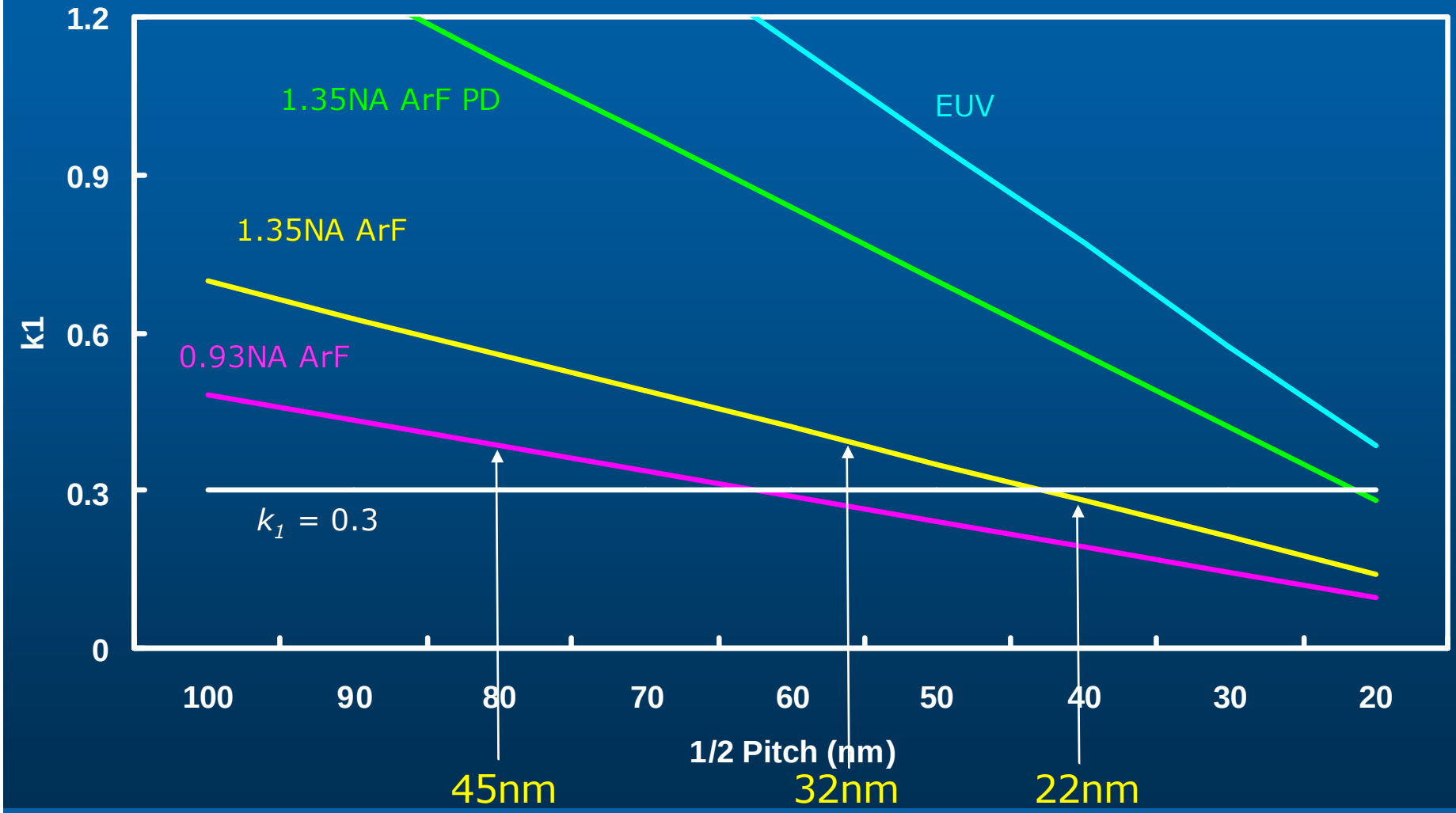
Excerpts from
Technical and Manufacturing Challenges and the Prospect for HVM using ArF Pitch Division, S. Sivakumar

Technical and Manufacturing Challenges and the Prospect for HVM using ArF Pitch Division

Sam Sivakumar

Intel Corporation

22nm Process – 2011 HVM

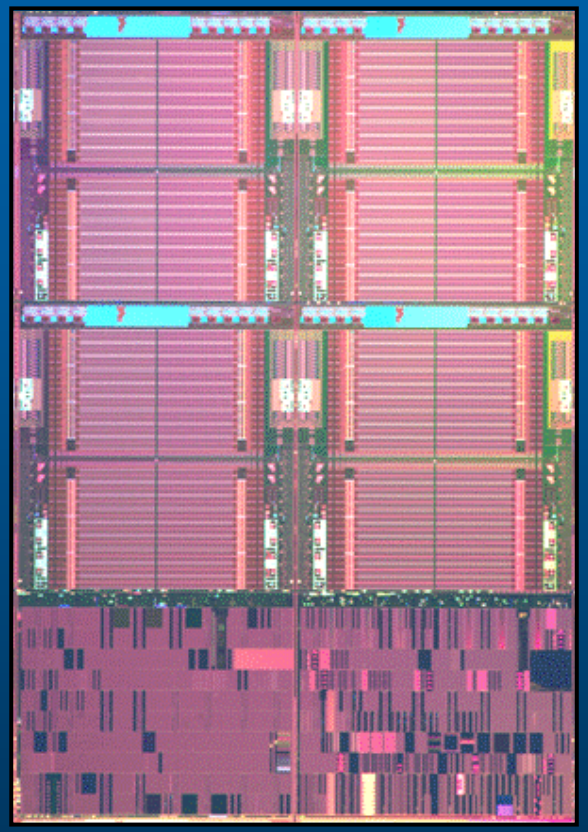


22nm SRAM Test Chip

SRAM, Logic, Mixed-Signal
Test Circuits

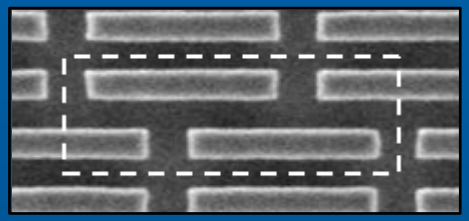
SRAM, Logic, Mixed-Signal
Test Circuits

Discrete
Test Structures

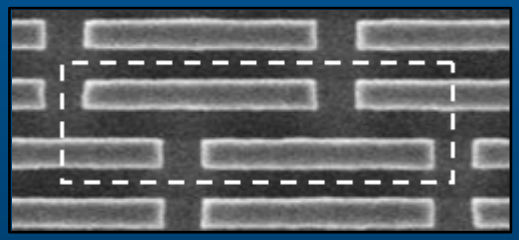


Intel is first in the industry to demonstrate working 22 nm circuits

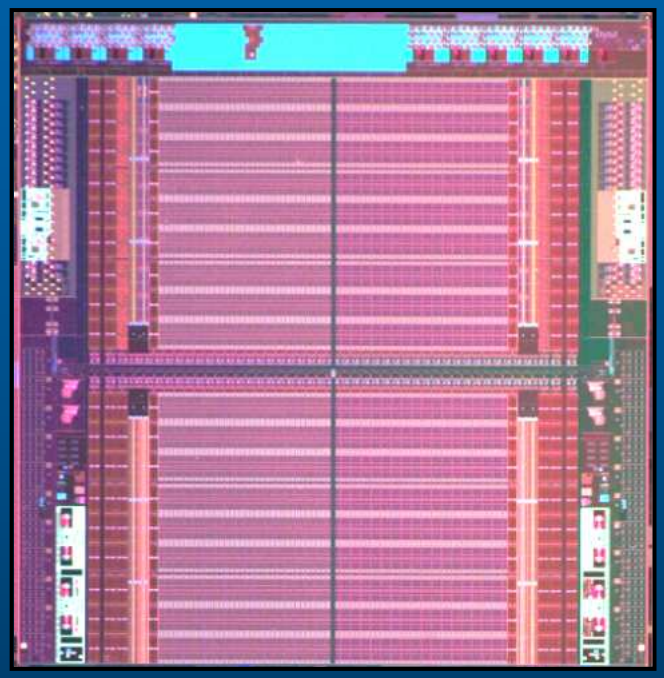
22nm SRAM Test Chip



0.092 um^2 SRAM cell
for high density applications

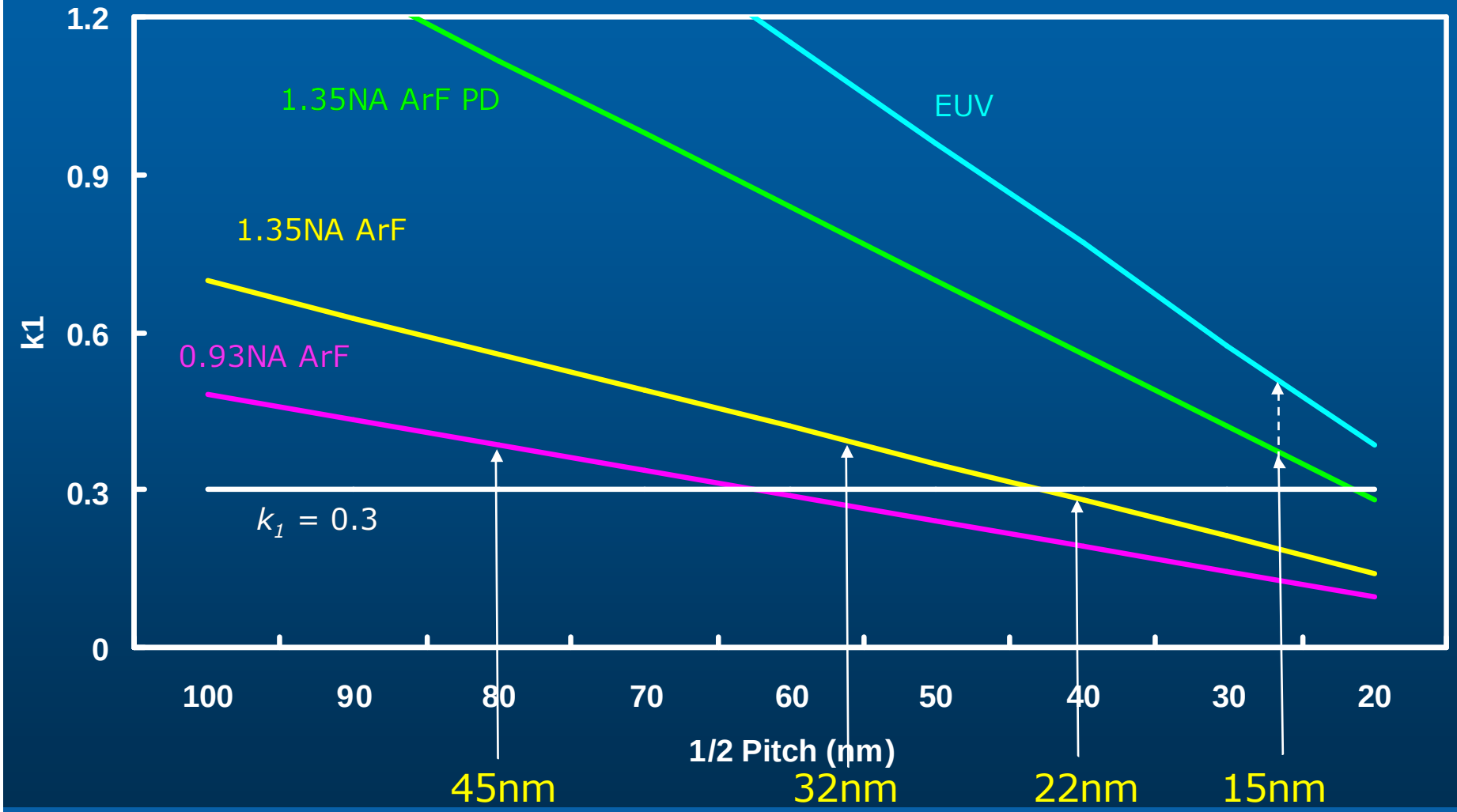


0.108 um^2 SRAM cell
for low voltage applications

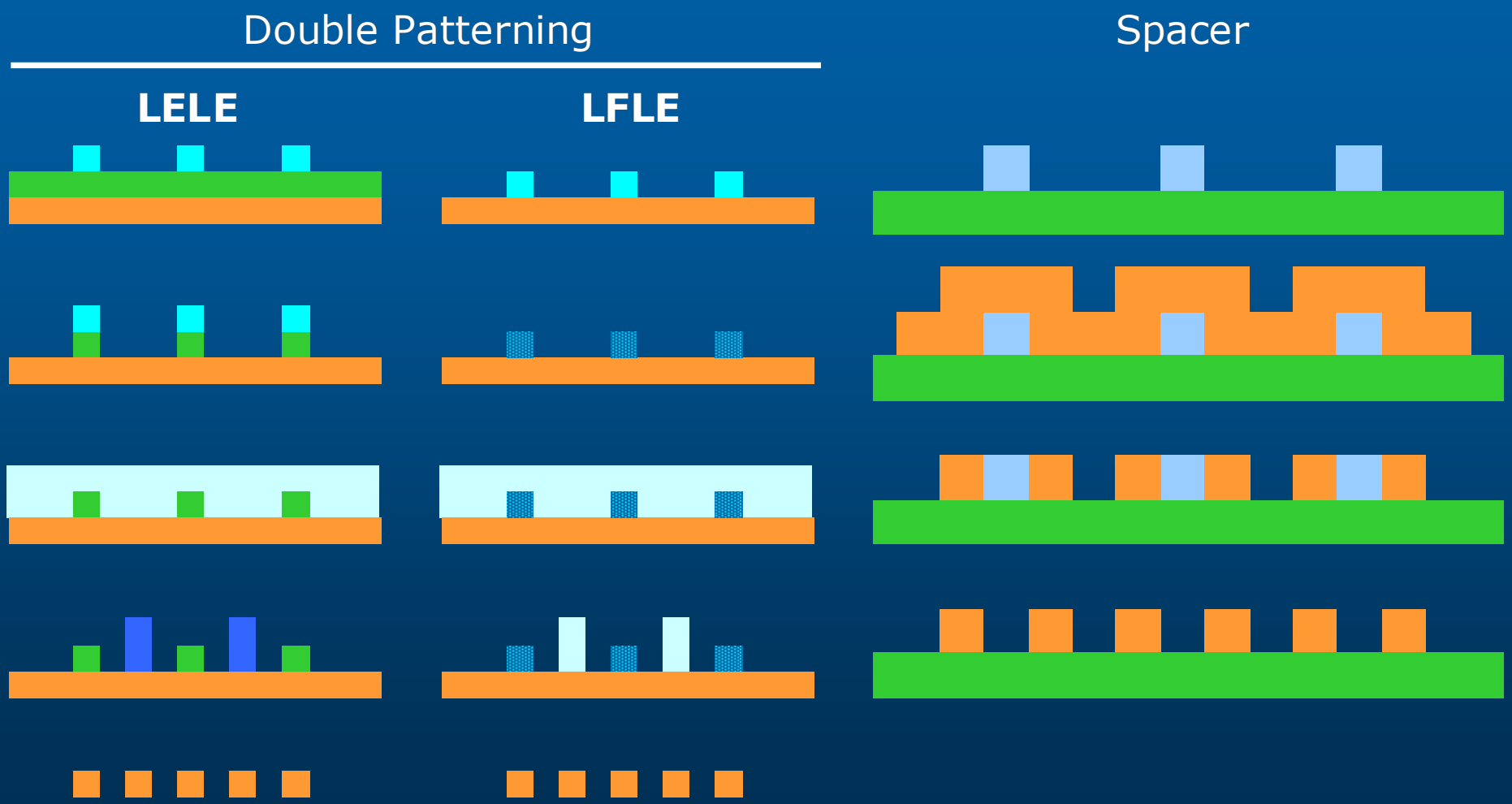


0.092 um2 is the smallest SRAM cell in working circuits reported to date

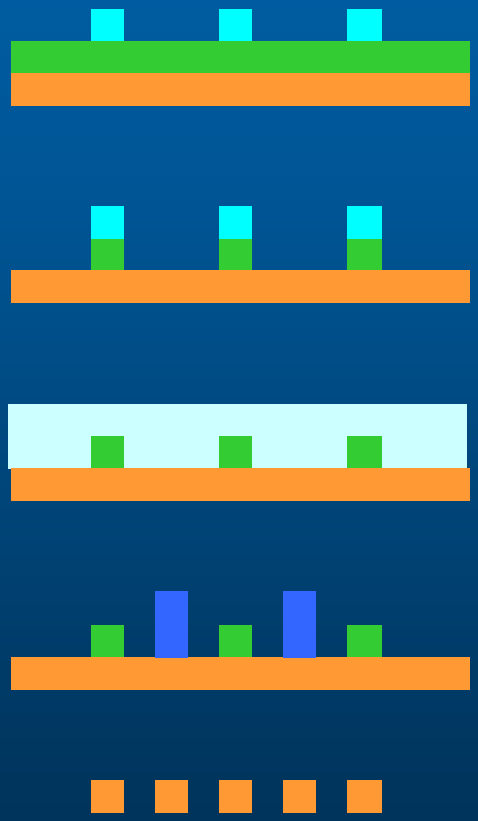
15nm Process – 2013 HVM

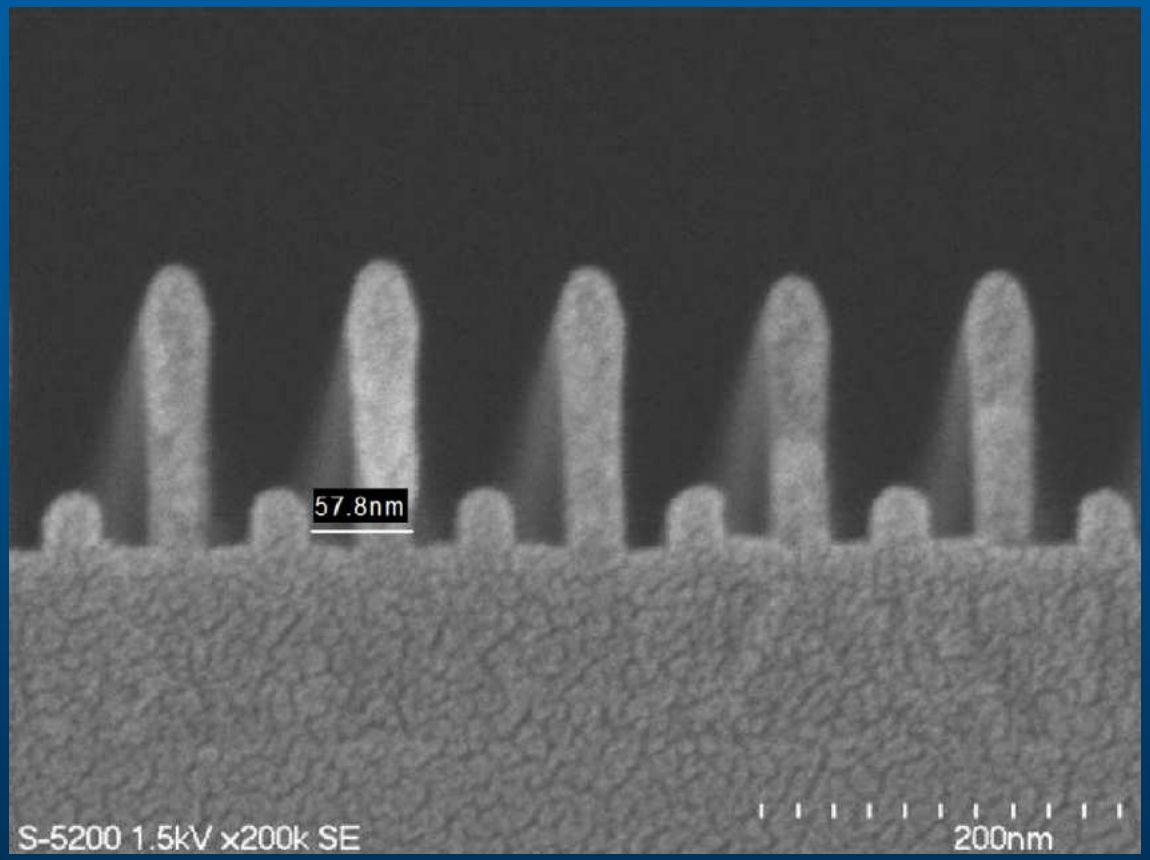


Pitch Division

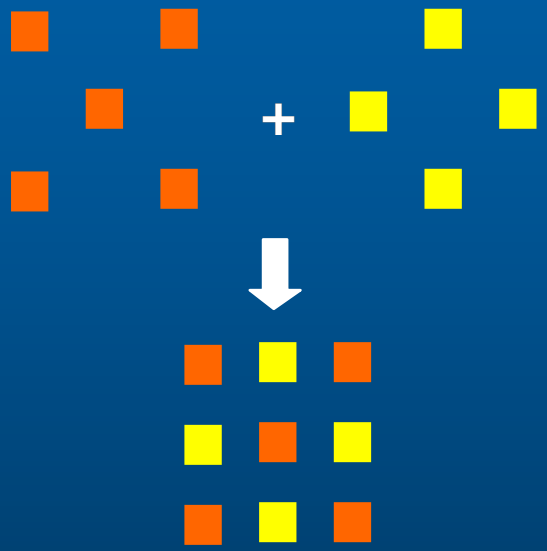


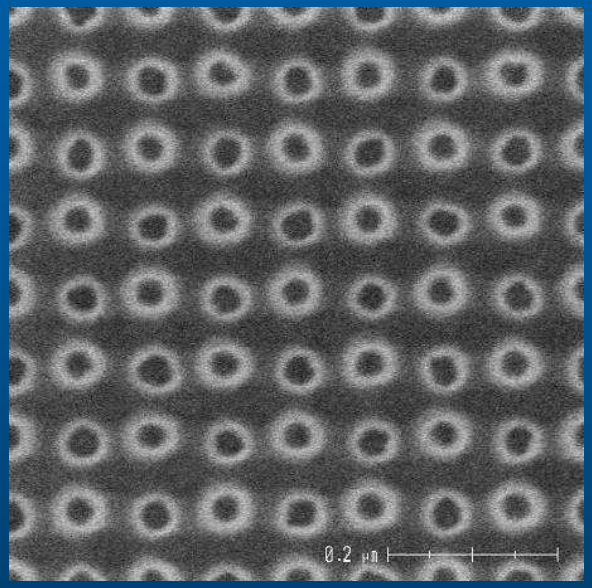
Double Patterning for L/S - LELE

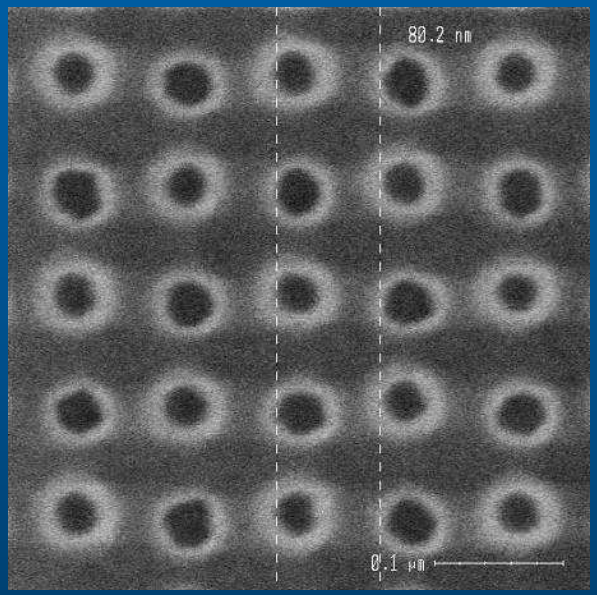




Double Patterning for Vias - LELE







Several different PD options will be picked and used depending on layer-by-layer applicability