IN THE UNITED STATES DISTRICT COURT

FOR THE DISTRICT OF OREGON

MEMORY INTEGRITY, LLC, Plaintiff, **v.** **INTEL CORPORATION**, Defendant.	Case No. 3:15-cv-00262-SI **OPINION AND ORDER**

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Michael H. Simon, District Judge.

Defendant Intel Corporation ("Intel") moves the Court to limit the number of claims asserted by Plaintiff Memory Integrity, LLC ("Memory Integrity") to 15 claims across five patents. For the reasons below, the Court grants Intel's motion. Dkt. 115.

STANDARDS

A court may limit the number of asserted claims in a patent case for the sake of judicial economy and management of a court's docket. *See* Fed. R .Civ. P. 16(c)(2)(P); *Stamps.com Inc. v. Endicia, Inc.*, 437 F. App'x 897, 902 (Fed. Cir. 2011) (recognizing "[the district] court's authority to impose a limit on the number of claims" in patent litigation). There exists little controlling precedent, however, to guide courts in deciding how many patent claims to allow parties to assert. Thus, in determining the most appropriate limit, courts are primarily guided by the goal of "secur[ing] the just, speedy, and inexpensive determination of every action and proceeding." Fed. R. Civ. P. 1; *see Medtronic Minimed Inc. v. Animas Corp.*, 2013 WL 3322248, at *1 (C.D. Cal. Apr. 5, 2013).

BACKGROUND

Memory Integrity has brought infringement claims against Intel under five patents: U.S. Patent Nos. 7,296,121 (the "'121 patent"), 7,103,636 (the "'636 patent"), 7,107,409 (the "'409 patent"), 8,572, 206 (the "'206 patent"), and 8,898,254 (the "'254 patent"). Memory Integrity asserts that the five patents come from four distinct families of patents. The patents are, however, all directed to maintaining cache coherency in multi-processor systems in which computer processors are connected in a "point-to-point architecture" or through "point-to-point links."[1] Dkt. 105-1 at 29 (the '121 patent); Dkt. 105-2 at 19-20 (the '636 patent); Dkt. 105-3 at 18 (the '409 patent); Dkt. 105-4 at 16-17 (the '206 patent); Dkt. 105-5 at 16 (the '254 patent). David B.

[1] Cache coherence issues arise in multiprocessor systems where each individual processor has a small, local memory called a cache and the system has a shared main memory. Each local cache stores data upon which the processor is currently operating to optimize access to that data. The data is then saved back to the main memory after operations conclude. Two or more processors operating on the same data may write different values into the cached copies of the data, in which case the system may be unable to determine which version to save to the shared memory. Cache coherence mechanisms address this problem. *See Computer Cache Coherency Corp. v. Via Techs.*, Inc., 2008 WL 4369770, at *2 (N.D. Cal. Sept. 23, 2008).

Glasco is either the sole inventor or one of several co-inventors for all five patents. Dkt.1 05-1 at 2; Dkt. 105-2 at 2; Dkt. 105-3 at 2; Dkt. 105-4 at 2; Dkt. 105-5 at 2. Across the five patents, Memory Integrity asserts 118 claims against Intel.[2]

Discovery has been ongoing since approximately October 2014.[3] *See* Dkt. 23 at 6. Intel has served Memory Integrity with invalidity contentions consisting of more than 6,000 pages. Dkt. 116 ¶ 5. Additionally, Intel has provided a forty-page explanation of its non-infringement positions. Dkt. 142-1.[4] Memory Integrity and Intel have conferred multiple times regarding reducing the number of asserted claims but have been unable to reach an agreement. *See* Dkt. 116 ¶¶ 4, 6-7; Dkt. 129 ¶¶ 2-4.

DISCUSSION

The parties acknowledge, and the Court agrees, that 118, or even 112, claims are far too many with which to proceed to trial. The parties disagree, however, on the appropriate number of claims and the timing for when Memory Integrity should reduce the number of claims. Quoting *High Point Sarl v. Sprint Nextel Corp.*, Intel argues that "[t]he time for identifying critical issues and for narrowing the scope of the litigation, if not passed, is now." 2010 WL 9497168, at *2-3 (D. Kan. Aug. 18, 2010). According to Intel, 118 is an unmanageable number of claims at the claim construction and expert discovery stages of proceedings. Memory Integrity responds that a

[2] Memory Integrity voluntarily dropped six of these claims on September 29, 2015, almost a month after Intel filed its motion to limit the number of asserted claims. Dkt. 141-2 at 1. This reduction brings the total number of asserted claims to 112.

[3] Memory Integrity filed this lawsuit on November 1, 2013, in the U.S. District Court for the District of Delaware. Dkt. 1. On February 13, 2015, the District Court in Delaware granted Intel's motion to transfer the case to the District of Oregon. Dkt. 44. Discovery was already proceeding while the case was in Delaware.

[4] Intel served Memory Integrity with its non-infringement positions on September 25, 2015, a week after Memory Integrity filed its brief opposing Intel's motion to limit the number of asserted claims.

limitation on asserted claims at this time, given the state of discovery, would be unduly prejudicial. Memory Integrity argues that it requires the benefit of important case developments, such as the Court's order on claim construction, before Memory Integrity can choose as low as 15 claims, the number requested by Intel.

Decisions across the country support a proposition that a limit of approximately 15 claims is not inappropriate in patent litigation. *E.g., In re Katz Interactive Call Processing Patent Litig.*, 639 F.3d 1303, 1310-12 (Fed. Cir. 2011) (affirming a limit of 16 claims per defendant from an original 1,975 claims); *Stamps.com Inc.*, 437 F. App'x at 900-03 (affirming a limit of 15 claims from an original 629 claims across 11 patents); *Select Comfort Corp. v. Gentherm, Inc.*, 2014 WL 4976586 (D. Minn. Oct. 3, 2014) (ordering a limit of 15 claims across five patents); *Joao Control & Monitoring Sys., LLC v. Ford Motor Co.*, 2014 WL 106926 (E.D. Mich. Jan. 10, 2014) (ordering a limit of 15 claims across five patents against the first defendant and eight claims per patent against the second defendant where the second defendant did not request a lower number); *Medtronic*, 2013 WL 3322248 (ordering a reduction of 255 claims to four claims for each of the nine patents in suit and then two claims for each patent after the submission of non-infringement and invalidity claims); *Havco Wood Products, LLC v. Indus. Hardwood Products, Inc.*, 2011 WL 5513214 (W.D. Wis. Nov. 10, 2011), *amended*, 2012 WL 5199185 (W.D. Wis. Oct. 22, 2012) (ordering a limit of 15 claims from an original 135 claims across five patents); *Visto Corp. v. Little Red Wagon Techs., Inc.*, 2012 WL 7989618 (N.D. Tex. Oct. 18, 2012) (ordering a limit of ten claims from an original 35 claims across five patents); *Fenster Family Patent Holdings, Inc., Elscint Ltd.*, 2005 WL 2304190 (D. Del. Sept. 20, 2005) (ordering a limit of ten claims from an original 90 claims across five patents).

Courts also generally agree that the time for limiting asserted claims is before the claim construction hearing. *E.g.*, *Joao*, 2014 WL 106926, at *4 ("It would be a waste of time and resources to conduct a claim construction hearing for a multitude of claims that Plaintiff may later elect not to pursue during the claim selection process."); *Masimo Corp. v. Philips Elecs. N. Am. Corp.*, 918 F. Supp. 2d 277, 284 (D. Del. 2013) ("[E]arly claim reduction is warranted before claim construction briefing and summary judgment motions are filed."); *Oasis Research, LLC v. Adrive, LLC*, 2011 WL 7272473, at *2 (E.D. Tex. Sept. 13, 2011) (holding "that limiting the amount of claims asserted by Plaintiff is appropriate at this time to aid in efficiency and narrowing the claims prior to claim construction"); *Hearing Components, Inc. v. Shure, Inc.*, 2008 WL 2485426 (E.D. Tex. June 13, 2008) (ordering the plaintiff to select no more than three representative claims from each patent before claim construction).

Memory Integrity argues that the Court should refrain from limiting the number of asserted claims at this time because Intel has failed to show that the asserted claims are duplicative under the standard set out in *Katz*. That case, however, did not require defendants to demonstrate that asserted claims are duplicative before claim limitation. Although acknowledging the defendant's "convincing showing that many of the claims are duplicative," the *Katz* court explicitly rejected the plaintiff's argument that the defendant must "bear the burden to show that issues were duplicative." 639 F.3d at 1311 (internal quotation marks omitted). The Federal Circuit instead found that the plaintiff was "in the best position to narrow the dispute" and thus could bear "the production burden" without suffering unfair prejudice. *Id.* This "allocation of burdens in the claim selection procedure" served to "benefit the decision-making process." *Id.* Other courts have also interpreted *Katz* as rejecting the proposition that defendants bear the burden of showing claim duplication. *See., e.g.*, *Thought, Inc. v. Oracle*

Corp., 2013 WL 5587559, at *2 (N.D. Cal. Oct. 10, 2013) ("[T]he Court does not agree that *In re Katz* requires defendants to make a prima facie showing of duplication in order to require a reduction in the number of asserted claims from a demonstrably unmanageable amount, here 102, to a manageable one.").

Although Intel is not required to show the duplicative nature of Memory Integrity's claims, Intel has demonstrated that the asserted claims overlap. For example, '254 patent is a continuation of the '206 patent, and the two patents share specifications. *See* Dkt. 105-5 at 2. The '636 patent also states that it is "related to" the application for the '409 patent. 105-2 at 19; *see* Dkt. 105-3 at 2. The patents all share at least one common inventor and detail methods or mechanisms for maintaining cache coherency in multi-processor systems.

Memory Integrity responds that its claims are all different in scope. As the *Katz* court notes, however, "[w]hile different claims are presumed to be of different scope, that does not mean that they necessarily present different questions of validity or infringement." 639 F.3d at 1313. Memory Integrity has not shown, at this juncture, that it requires more than 15 claims to adequately address unique questions of validity and infringement. Further, Memory Integrity acknowledges that it must reduce asserted claims at some point in these proceedings; Memory Integrity has not offered sufficient reasons why that point is not now.

Memory Integrity has had more than a year to conduct discovery. Intel has served Memory Integrity with its invalidity contentions and an explanation of its non-infringement positions. Memory Integrity is thus able to limit its number of asserted claims to 15 without suffering undue prejudice and without requiring the gradual, staged reduction that Memory Integrity offers as a counterproposal. Like the district court's decision in *Stamps.com*, however, the Court's decision is not "immutable." 437 F. App'x at 902. If Memory Integrity ultimately

discovers that non-selected claims raise separate and distinct legal issues from those raised by the already-selected claims, Memory Integrity may ask the Court for leave to reassert unselected claims. Similarly, after claim construction and summary judgment motions, if any, have been resolved, the Court may consider the parties positions on whether further limitations of Memory Integrity's claims should be ordered before trial. *See* Fed. R. Civ. P. 42(b) ("[T]he court may order a separate trial of one or more separate . . . claims.").

Intel proposes that to further streamline the case, it will limit itself to asserting no more than 35 prior art references within three months of Memory Integrity's reduction of asserted claims. Other courts have found that defendants have the ability to limit prior art references within two to three weeks of the plaintiff limiting the claims at issue. *E.g.*, *Select Comfort Corp.*, 2014 WL 4976586, at *2; *Thought*, 2013 WL 5587559, at *4. Given the advanced stage of discovery, Intel should be able to limit its prior art references to 35 within three weeks of Memory Integrity's reduction of asserted claims.

CONCLUSION

Intel's Motion to Limit the Number of Asserted Claims (Dkt. 115) is GRANTED. The Court directs Memory Integrity to limit its asserted claims to no more than 15 within 14 days of the entry of this Order. The Court further directs Intel to limit the number of prior art references to no more than 35 within 21 days after Memory Integrity selecting its 15 (or less) asserted claims.

IT IS SO ORDERED.

DATED this 30th day of October, 2015.

/s/ Michael H. Simon
Michael H. Simon
United States District Judge