United States District Court

EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

MICROLINC, LLC	§	
	§	
v.	§	**Case No. 2:07-cv-488**
	§	
INTEL CORP., et al.	§	

MEMORANDUM OPINION AND ORDER

This claim construction order construes the disputed claim terms of U.S. Patent No. 6,009,488 ('488 Patent) entitled "Computer Having Packet-Based Interconnect Channel." On May 16, 2013, the Court held a claim construction hearing to construe the disputed terms. For the following reasons, the Court adopts the constructions set forth below. *See also* Appendix A.

I. PROCEDURAL BACKGROUND

The procedural background for this case is atypical. It involves two lawsuits, four ex parte reexaminations of the asserted patent by the U.S. Patent and Trademark Office (USPTO), an appeal to the Board of Patent Appeals and Interferences (BPAI), two court orders staying the case, and the issuance of two Reexamination Certificates. Plaintiff filed the original lawsuit against Intel and other defendants on November 10, 2005. *See Microlinc, L.L.C. v. Acer Am. Corp., et al.*, No. 2:05-cv-514 (the First Lawsuit). Shortly thereafter, Plaintiff dismissed the First Lawsuit and submitted the '488 Patent for reexamination by the USPTO. Plaintiff filed its Request for Ex Parte Reexamination of all claims of the '488 Patent on June 30, 2006 (the First Reexamination) (No. 90/008,106). The USPTO agreed to reexamine the patent on August 22,

2006. Defendant Intel filed a separate Request for Ex Parte Reexamination on August 28, 2006 (the Second Reexamination) (No. 90/008,196). The First Reexamination and the Second Reexamination were then merged on October 12, 2007. On October 29, 2007, the USPTO issued a non-final Office Action confirming the patentability of claims 10 and 13 of the '488 Patent.

Plaintiff then filed the present suit on November 7, 2007, even though the '418 Patent was still in reexamination. Intel then filed its second Request for Ex Parte Reexamination on March 26, 2008 (the Third Reexamination) (No. 90/009,098), which was later merged with the First and Second Reexaminations on July 19, 2008. On May 29, 2008, the defendants sought to stay the case pending the reexamination of the '488 Patent (Doc. No. 111). Given the exceptional circumstances surrounding the pending reexamination, the Court granted the defendants' motion on September 16, 2008 (Doc. No. 154).

On October 28, 2008, the USPTO issued a Notice of Intent to Issue Reexamination Certificate for the '488 Patent confirming the patentability of original claim 13 and new claims 14-28. On December 23, 2008, Intel filed a third Request for Ex Parte Reexamination (the Fourth Reexamination) (No. 90/009,376), which was granted on March 16, 2009. Despite the pending fourth reexamination request, the USPTO issued the first Reexamination Certificate for the '488 Patent on February 10, 2009. Accordingly, the Court lifted the stay in this case on August 14, 2009 (Doc. No. 201).

On June 30, 2010, the defendants sought to stay this case for a second time because the USPTO issued a final rejection of all pending claims in the fourth reexamination (Doc. No. 314). On September 20, 2010, the Court granted the defendants' motion because Plaintiff was continuing to amend the claims and prosecute new claims in the pending reexamination (Doc. No. 374). On January 12, 2011, Plaintiff appealed the final rejection to the Board of Patent Appeals and Interferences (BPAI). On June 6, 2012, the BPAI reversed the examiner on certain

rejections pertaining to independent claims 14, 27–29, 31, 34, and 35, and dependent claims 15–17, 20–26, 30, and 37–40, and found that claims 14–17 and 27–31 were patentable over the prior art of record. On November 13, 2012, the USPTO issued the second Reexamination Certificate for the ’488 Patent, which sets forth that: (l) the patentability of claims 14–17 and 20–28 was confirmed; (2) claims 1–12 were previously canceled; (3) claims 13, 18, and 19 were canceled; and (4) new claims 29–39 were added and determined to be patentable. The USPTO issued a Certificate of Correction on February 12, 2013, which corrected errors appearing in the claims of the ’488 Patent. On October 25, 2012, the Court entered the Fifth Amended Scheduling and Discovery Order (Doc. No. 408).

II. BACKGROUND OF THE TECHNOLOGY

The ’488 Patent issued on December 28, 1999 and generally relates to a physically non-distributed microprocessor-based computer that includes a “packet-based” communication system that allows a computer’s components—such as a microprocessor, main memory, and disk drive—to communicate with each other. Specifically, the specification states that the “present invention provides a system with the configuration flexibility of a bus-based PC while reducing the electrical problems” by applying “a point-to-point packetized interconnection structure to facilitate communication between functional units (e.g., processor, memory, disk, I/O, etc.) within a PC.” ’488 Patent at 2:12–18. Thus, the invention purports to overcome “several limitations and unique problems associated” with prior art bus systems. ’488 Patent at 1:26–2:63.

The ’488 Patent explains that in the prior art computer, components talked to each other over a shared “bus.” ’488 Patent at 1:10–2:11, 4:26–31, 4:63–5:18. Figure 1 from the ’488 Patent is an example of a prior art bus system, where components such as the video card **45** and the disk/storage device **46** all share access to one shared bus **43** in order to communicate with the

microprocessor **40** or system memory **42**:

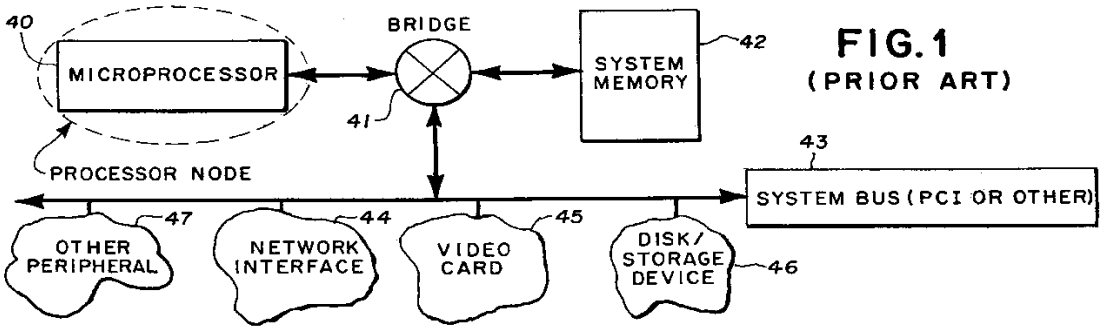


FIG. 1
(PRIOR ART)

In this shared bus system, each message is broadcast to all components, which means that only one conversation can occur at a time over the bus. The specification identifies this as the single transaction and sequential problem because only two functional units can communicate with one another at any given time and establishing this communication required considerable handshaking. '488 Patent at 1:26–33.

In addition to this problem, the '488 Patent identified a number of other problems with the prior art bus system. '488 Patent at 1:33–2:63. For example, the specification states that the prior art bus system required that "all functional units connected to the bus must meet the electrical specifications and requirements of the bus even if these specifications and requirements are quite dated, technologically." *Id.* Additionally, the specification states that "because the bus is a generic interconnect in nature, it can not be truly optimized for communication between any specific subset of functional units without adversely affecting communication performance between another subset of functional units." *Id.* The specification further states that "the speed of the bus is substantially slower than might otherwise be obtainable" because of the electrical noise margin requirements that restrict the speed of the bus and the fact that the highly variable electrical loading of the bus requires it to be "slowed down to a rate that would sustain a worst case loading situation even though this may occur in one PC in a thousand." *Id.* Finally, the specification states

that "[o]ther major drawbacks of a bus are the need for electrical handshake signals and its fixed electrical data width (i.e., 8 bits, 16 bits, 32 bits, etc.)." *Id.*

The '488 Patent purports to solve these stated problems by disclosing a personal computer system in which data is transmitted in the form of "packets." Rather than broadcasting a message to all components, a packet is transmitted through a network analogous to how packages are delivered by the postal service. Each packet (like a package) contains a "payload" of data (contents of a package) and a "header" (address on a package). The header routes the packet to the intended receiver, which then accesses the payload (opening the package and retrieving the contents). *See* '488 Patent at 5:45–6:25, Figs. 3–8. Because the components of a personal computer may not be designed to communicate with each other using packets, the '488 Patent provides for packet communication through "packet nodes." This is shown in Figures 2, 24, and 25:

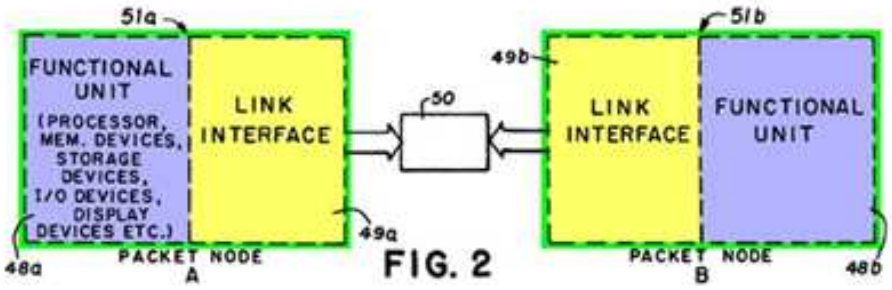
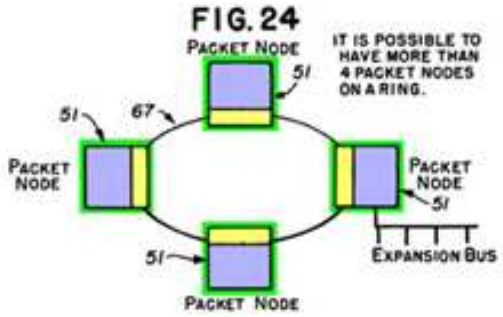
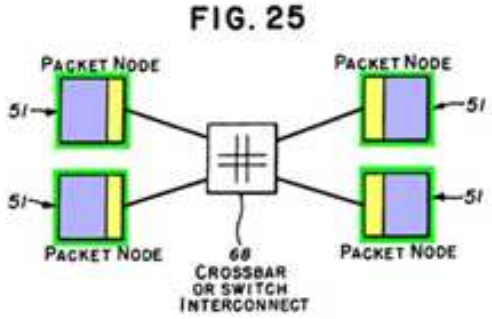


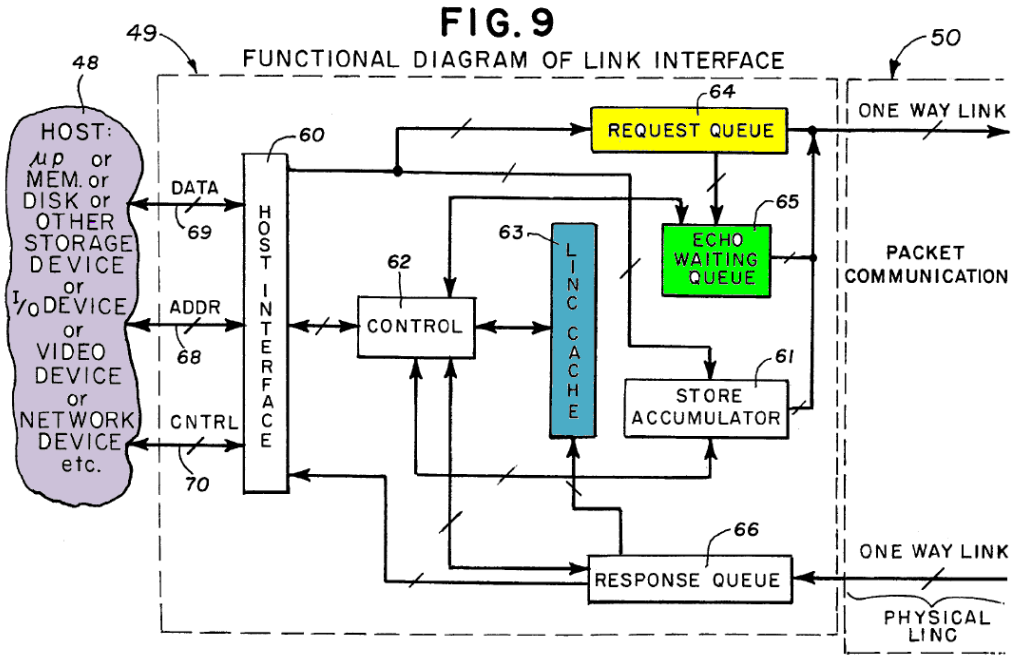
FIG. 2





These figures show that packet nodes **51** (outlined in green) include a functional unit **48** (shaded in purple) and a "link interface" **49** (shaded in yellow). The functional unit **48** portion of a packet node includes a component of a personal computer (*e.g.*, a processor, a memory, a display, or an input/output device). *See* '488 Patent at Fig. 2. The packet nodes are connected with a packet-based data channel that extends between the interfaces of the packet nodes. '488 Patent, Abstract at 1:5–8, 4:23–25. This "high speed message passing packetized interconnect channel and protocol is intended to allow asynchronous communication between any two nodes, so equipped, in any system configuration using packets of data or instructions." '488 Patent at 4:32–35. Thus, according to the specification, the claimed invention avoids being "a hardware restricted, single transaction, high overhead interconnect (i.e., a bus)." '488 Patent at 4:52–53.

The asserted claims focus on two sets of structures included in a functional unit's interface: (1) a "linc cache," and (2) a set of two buffers, in which one buffer is used to queue packets for transmission, and a separate buffer is used to store packets for retransmission, if necessary. Those features are illustrated in Figure 9, which is an expansion of a functional unit's interface **49** (shaded in yellow in the previous figures):



The Court turns first to the "cache" structure. A "cache" may be generically described as high-speed memory used for temporary storage of frequently-used data (*see, e.g.*, Doc. No. 511-4 at 1). The patent's "linc cache" **63** (shaded above in blue) is one type of cache located in the functional unit's link interface. The linc cache stores packets for use by functional unit **48** (shaded above in purple). '488 Patent at 8:63–64. This can reduce the need for the functional unit **48** to send requests for data since the data may already be stored in the linc cache.

The Court turns next to the "two buffer" structure. The "first buffer" in the interface is illustrated above as "request queue" **64** (shaded in yellow). This buffer queues packets until they are transmitted over data channel **50**. '488 Patent at 8:28–29, Fig. 9. A copy of the transmitted packet is stored in a separate "second buffer," shown above as the "echo waiting queue" **65** (shaded in green). '488 Patent at 8:45–49, Fig. 9. If a transmission error occurs, the copy in the second buffer is retransmitted. '488 Patent at 9:61–10:1.

Thus, according to the specification of the '418 Patent, the point-to-point interconnection

scheme of the invention solves the problems with prior art bus systems because it: (1) "is of relatively fixed electrical load and can, therefore, be optimized for speed," (2) "provides a means of eliminating the typical physical layer control signals of a bus and replacing them with link-layer control which is much more flexible," and (3) "improves speed and performance at reduced cost and with better noise characteristics (both internal electrical noise and radiated EMI) as compared to the bus interconnect currently employed within a PC." '488 Patent at 2:19–43.

The abstract of the '488 Patent is reproduced below:

> A physically non-distributed microprocessor-based computer includes a microprocessor, and a random access memory device, a mass storage device, and an input-output port device, all operable from the microprocessor and including an interface for receiving and transmitting data in packet form. A novel packet-based data channel extends between the microprocessor and the interfaces of the devices to provide communication between the microprocessor and the devices. By varying the size of the packets in accordance with actual data transmission requirements improved computer performance is achieved.

As an exemplary claim of the '488 Patent, claim 14 is reproduced below:

> A physically non-distributed microprocessor-based computer system comprising:
>
> a microprocessor;
>
> a random access memory device;
>
> a mass storage device;
>
> an input-output port device;
>
> said devices each being operable in conjunction with said microprocessor; said microprocessor and said devices each including an interface for receiving and transmitting data in packet form;
>
> a packet-based data channel extending between said microprocessor and said interfaces of said devices for providing simultaneous bi-directional communication

between said microprocessor and said devices; and

a first one of said interfaces including a first buffer for queuing packets for a transmission, and a second buffer for storing a copy of a packet transmitted by said first interface to a second one of said interfaces, said second buffer storing said copy pending receipt of a reply packet acknowledging receipt of said transmitted packet by said second interface.

III. LEGAL STANDARD

Claim construction is a matter of law. *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995). The purpose of claim construction is to resolve the meanings and technical scope of claim terms. *U.S. Surgical Corp. v. Ethicon, Inc.*, 103 F.3d 1554, 1568 (Fed. Cir. 1997). When the parties dispute the scope of a claim term, "it is the court's duty to resolve it." *O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co.*, 521 F.3d 1351, 1362 (Fed. Cir. 2008).

The claims of a patent define the scope of the invention. *Teleflex, Inc. v. Ficosa N. Am. Corp.*, 299 F.3d 1313, 1324 (Fed. Cir. 2002). They provide the "metes and bounds" of the patentee's right to exclude. *Corning Glass Works v. Sumitomo Elec. U.S.A., Inc.*, 868 F.2d 1251, 1257 (Fed. Cir. 1989). Accordingly, claim construction begins with and "remain[s] centered on the claim language itself." *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1116 (Fed. Cir. 2004).

Claim terms are normally given their "ordinary and customary meaning." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)). Generally, "the ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention." *Id* at 1313.

The best guide for defining a disputed term is a patent's intrinsic evidence. *Teleflex*, 299 F.3d at 1325. Intrinsic evidence includes the patent's specification and the prosecution history. *Id.*

The claims are part of the specification. *Markman*, 52 F.3d at 979. "[T]he context in which a term is used in the asserted claim can be highly instructive." *Phillips*, 415 F.3d at 1314; *see also Abtox, Inc. v. Exitron Corp.*, 122 F.3d 1019, 1023 (Fed Cir. 1997) ("[T]he language of the claim frames and ultimately resolves all issues of claim interpretation."). "Differences among claims can also be a useful guide in understanding the meaning of particular claim terms." *Phillips*, 415 F.3d at 1314.

In addition to the claims, the specification's written description is an important consideration during the claim construction process. *See Vitronics Corp.*, 90 F.3d at 1582. The written description provides further context for claim terms and may reflect a patentee's intent to limit the scope of the claims. *See Watts v. XL Sys., Inc.*, 232 F.3d 877, 882 (Fed. Cir. 2000). "[T]he specification 'is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.'" *Phillips*, 415 F.3d at 1315 (quoting *Vitronics*, 90 F.3d at 1582).

The specification may also resolve ambiguous claim terms "where the ordinary and accustomed meaning of the words used in the claims lack sufficient clarity to permit the scope of the claim to be ascertained from the words alone." *Teleflex, Inc.*, 299 F.3d at 1325. For example, "[a] claim interpretation that excludes a preferred embodiment from the scope of the claim 'is rarely, if ever, correct.'" *Globetrotter Software, Inc. v. Elam Computer Grp., Inc.*, 362 F.3d 1367, 1381 (Fed. Cir. 2004) (quoting *Vitronics Corp.*, 90 F.3d at 1583).

But care must be taken to avoid unnecessarily reading limitations from the specification into the claims. *Teleflex*, 299 F.3d at 1326; *see also Raytheon Co. v. Roper Corp.*, 724 F.2d 951, 957 (Fed. Cir. 1983) ("That claims are interpreted in light of the specification does not mean that everything expressed in the specification must be read into all the claims."). "[P]articular embodiments appearing in the written description will not be used to limit claim language that has broader effect." *Innova/Pure Water*, 381 F.3d at 1117; *see also Phillips*, 415 F.3d at 1323 ("[A]lthough the specification often describes very specific embodiments of the invention, we have repeatedly warned against confining the claims to those embodiments.").

The prosecution history is also part of the intrinsic evidence. *Phillips*, 415 F.3d at 1317. It "consists of the complete record of the proceedings before the PTO and includes the prior art cited during the examination of the patent." *Id.* "As in the case of the specification, a patent applicant may define a term in prosecuting a patent." *Home Diagnostics, Inc. v. LifeScan, Inc.*, 381 F.3d 1352, 1356 (Fed. Cir. 2004). Statements made during the prosecution of the patent may limit the scope of the claims. *Teleflex*, 299 F.3d at 1326; *see Omega Eng'g Inc. v. Raytek Corp.*, 334 F.3d 1314, 1323 (Fed. Cir. 2003) (explaining that the doctrine of prosecution disclaimer "preclud[es] patentees from recapturing through claim interpretation specific meanings disclaimed during prosecution").

Finally, the Court may rely on extrinsic evidence to aid with understanding the meaning of claim terms. *Markman*, 52 F.3d at 981. Extrinsic evidence includes "all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises." *Id.* at 980. Extrinsic evidence is generally less useful or reliable, *Phillips*, 415 F.3d at 1317, and it should not be relied on when it contradicts the intrinsic evidence, *Markman*, 52 F.3d at 981.

IV. DISCUSSION

The parties' dispute focuses on the meaning and scope of 14 terms/phrases in the claims of the '488 Patent. Additionally, the parties have agreed on the construction of a number of other terms.

a. "microprocessor" and "[a] physically non-distributed microprocessor-based computer system"

Disputed Claim Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction
"microprocessor"	Ordinary meaning, in the alternative: "a central processing unit residing within a single chip"	"the central processing unit of a computer on a single integrated chip"
"[a] physically non-distributed microprocessor-based computer system"	"a microprocessor-based computer system in which all the components are close to one another and contained within a single enclosure, e.g., a personal computing device or server"	"a microprocessor-based computer system (other than a multiprocessor-based system) in which all the components are close to one another (e.g., a personal computer within a single enclosure)"

The parties dispute whether the term "microprocessor" and the phrase "[a] physically non-distributed microprocessor-based computer system" should be limited to a single microprocessor or whether the terms include multiprocessor-based systems. Defendants contend that it should be limited to a single microprocessor based on prosecution history estoppel. *Standard Oil Co. v. Am. Cyanamid Co.*, 774 F.2d 448, 452 (Fed. Cir. 1985) ("[T]he prosecution history (or file wrapper) limits the interpretation of claims so as to exclude any interpretation that may have been disclaimed or disavowed during prosecution in order to obtain claim allowance."). Specifically, Defendants contend that the patentee argued to the USPTO that certain prior art was different from the claimed invention because it disclosed "a packet-based

interconnect for use in high-performance *multiprocessor* systems" (Doc. No. 511-32 at 7 (emphasis added)). Defendants argue that this statement represents a clear disavowal of a multiprocessor-based system and that their proposed constructions properly limit the claims to systems with one microprocessor. Plaintiff disagrees and contends that the claim terms should not be limited to a single microprocessor or a microprocessor with only a single core.

The Court agrees with Plaintiff and finds that the patentee did not make a clear and unmistakable disclaimer of a physically non-distributed unit containing more than one microprocessor or a microprocessor with more than one core. However, as discussed in more detail below, the Court concludes that Plaintiff did make a clear disclaimer of a physically distributed system (*i.e.*, where the multiple microprocessors are not contained within a single enclosure or common housing). This conclusion is consistent with the representations made by Plaintiff during the claim construction hearing that the patentee limited the invention to physically non-distributed systems. Accordingly, the Court concludes that Plaintiff's proposed constructions are consistent with the claim language, the specification, and the prosecution history.

i. The Claim Language

The Court first turns to the language of the claims, as it provides "substantial guidance as to the meaning of particular claim terms." *Phillips*, 415 F.3d at 1313 (citing *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)). The term "microprocessor" appears in claims 14, 24, 27–29, 31–35, and 37. The phrase "[a] physically non-distributed microprocessor-based computer system" appears in claims 14, 27–29, and 31–35. Having reviewed the claims, the Court concludes that the term "microprocessor" term, and the phrase "[a] physically non-distributed microprocessor-based computer system" are used consistently in each claim and are

meant to have the same meaning in each claim. The Court further concludes that the plain language of the disputed phrase requires a "physically non-distributed" system (*e.g.*, a computer within a single enclosure).

Furthermore, the Court concludes that the plain language of the claims requires at least one microprocessor, but that the claims are not limited to systems having only a single microprocessor or a microprocessor with only a single core. Indeed, Defendants' proposed constructions ignore a fundamental principle of claim construction by replacing the article "a" with the article "the" and suggesting that there can only be a single central processing unit. It is well established that "a" is generally understood to mean "one or more." *Baldwin Graphic Sys., Inc. v. Siebert, Inc.*, 512 F.3d 1338, 1342 (Fed. Cir. 2008) ("That 'a' or 'an' can mean 'one or more' is best described as a rule, rather than merely as a presumption or even a convention."). As discussed in more detail below, nothing in the claim language, specification, or prosecution history indicates that the patentee departed from the general rule for the article "a." Accordingly, the Court finds that Plaintiff's constructions are consistent with the ordinary and customary meaning of the claim language as understood by one of ordinary skill in the art. The Court will now turn to the other intrinsic evidence.

ii. The Intrinsic Evidence

In addition to the claims, the other intrinsic evidence in this case, specifically the specification and prosecution history, supports the adoption of Plaintiff's constructions. Although the specification does not explicitly disclose an embodiment including a multiprocessor system or a multicore processors, the specification states that "[w]hile a particular embodiment of the invention has been shown and described, it will be obvious to those skilled in the art that changes and modifications may be made therein without departing from the invention

in its broader aspects, and, therefore, the aim in the appended claims is to cover all such changes and modifications as fall within the true spirit and scope of the invention." '488 Patent at 11:49–55. Moreover, it is well established that claims are not limited to the embodiments disclosed in the specification. *Rexnord Corp. v. Laitram Corp.*, 274 F.3d 1336, 1344 (Fed. Cir. 2001) ("[A]n applicant is not required to describe in the specification every conceivable and possible future embodiment of his invention.").

Defendants respond that general claim interpretation guidelines do not trump a clear disclaimer. *Omega Eng'g, Inc, v. Raytek Corp.*, 334 F.3d 1314, 1324 (Fed. Cir. 2003) ("[W]here the patentee has unequivocally disavowed a certain meaning to obtain his patent, the doctrine of prosecution disclaimer attaches and narrows the ordinary meaning of the claim congruent with the scope of the surrender."). However, the Court does not find that the patentee unequivocally disavowed a physically non-distributed unit containing more than one microprocessor or a microprocessor with more than one core.

Defendants' disclaimer argument hinges on a single statement made during the first reexamination regarding the Scalable Coherent Interface References ("SCI References"). Specifically, in disclosing these references, the patentee stated:

> [The SCI References] disclose a packet-based interconnect for use in high-performance multiprocessor systems. While these references disclose a packet-based interconnection, and therefore are arguably relevant to claims 1-13 of the '488 reference, these references do not disclose an interconnect for use in physically non-distributed microprocessor based computer systems.

(Doc. No. 511-32 at 7). Defendants contend that this single statement represents a clear disavowal of multiprocessor systems. The Court disagrees and finds that as it relates to the "microprocessor" element of a non-distributed system, one of ordinary skill in the art would find

that the patentee's statement is ambiguous and amenable to multiple reasonable interpretations, and thus, is not a clear disavowal. *Elbex Video, Ltd. v. Sensormatic Elecs. Corp.*, 508 F.3d 1366, 1373 (Fed. Cir. 2007) ("For a prosecution statement to prevail over the plain language of the claim, the statement must be clear and unmistakable . . . ."); *see also N. Telecom Ltd. v. Samsung Elecs. Co.*, 215 F. 3d 1281, 1293–95 (Fed. Cir. 2000) (holding that prosecution history failed to support the judicial narrowing of a claim term because the inventors' statements concerning the invention and the prior art were amenable to multiple reasonable interpretations).

The parties agree that the SCI References are directed towards a physically distributed system. In fact, one of the SCI specifications states that its purpose is "[t]o define an interface standard for very high performance multiprocessor systems that supports . . . systems with up to 64K nodes" (Doc. No. 504-4 at 3). Accordingly, a person of ordinary skill in the art would understand that the SCI References at least pertain to physically distributed computing systems that may be used for identifying a large number of physically distributed nodes. Thus, the Court concludes that the patentee clearly disclaimed physically distributed systems in distinguishing the SCI References.[1]

However, in distinguishing the SCI References, it is unclear if the patentee disclaimed anything other than a physically distributed system. Specifically, the patentee stated that "these references do not disclose an interconnect for use in physically non-distributed *microprocessor* based computer systems" (Doc. No. 511-32 at 7 (emphasis added)). The patentee did not mention multiprocessor systems or multicore systems in this statement, but instead uses the term

[1] The Court's conclusion is consistent with the claim language, which recites a "physically non-distributed" computer system. Likewise, the Court's conclusion is consistent with the representations made by Plaintiff during the claim construction hearing that the patentee limited the invention to physically non-distributed systems.

"microprocessor." In other words, if the patentee's statement was that "these references do not disclose an interconnect for use in physically non-distributed [*multiprocessor*] based computer systems," then a disclaimer finding would be warranted. Accordingly, the Court finds that the patentee did not unequivocally disclaim a multiprocessor system or a multicore system included in a physically non-distributed system.

iii. Court's Construction

In light of the claim language, the specification, and the prosecution history, the Court adopts Plaintiff's proposed constructions and construes a **"microprocessor"** to mean **"a central processing unit residing within a single chip."** The Court construes **"[a] physically non-distributed microprocessor-based computer system"** to mean **"a microprocessor-based computer system in which all the components are close to one another and contained within a single enclosure."**

b. "said microprocessor and said devices each including an interface for receiving and transmitting data in packet form"

Disputed Claim Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction
"said microprocessor and said devices each including an interface for receiving and transmitting data in packet form"	"each of the microprocessor, the random access memory device, the mass storage device, and the input-output port device has at least one interface connected to it, for receiving and transmitting data in packet form"	"each of the microprocessor, the random access memory device, the mass storage device, and the input-output port device includes its own interface for receiving and transmitting data in packet form"

The parties' dispute is focused on two issues. The first issue is whether the claimed "interface" must be physically incorporated within each of the claimed devices (*i.e.*, the microprocessor, the mass storage device, the random access memory). The second issue is

whether the claimed devices may share an interface or whether each of the claimed devices must have a separate interface.

Regarding the first issue related to the physical incorporation, Defendants contend that their proposed construction uses the word "including" exactly as the inventor used the word in the specification and that the interfaces must be physically incorporated within each device. Defendants further contend that Plaintiff's position would effectively overrule the USPTO's determination that the interface must be included in the functional unit. Plaintiff responds that the specification of the '488 Patent expressly depicts and discusses embodiments of an interface that is separate from but connected to a functional unit, in addition to embodiments of a link interface that is integrated within a functional unit. *See e.g.*, '418 Patent at 9:28–40, Figs. 13, 14. The Court agrees with Plaintiff and finds that the claimed "interface" may either be incorporated within each of the claimed devices or connected to the claimed devices.

Regarding the second issue related to the shared interface, Plaintiff concedes that the amended claims require an interface for the microprocessor and for each device but contends that the "interface" language was not at issue during the reexamination. Plaintiff further contends that Defendants have not pointed to any discussion in the prosecution history that prohibits functional units from sharing an interface. Defendants respond that the plain language of the claims, specification, and file history make clear that each device must have its own interface. The Court agrees with Defendants because the patentee amended the claims during the reexamination to emphasize that the claimed devices each require a separate interface. Moreover, during the claim construction hearing, Plaintiff agreed with the Court that each of the claimed devices must have its own interface. Accordingly, the Court does not adopt either side's construction. Instead, the Court provides a construction that is consistent with the claim

language, the specification, and the prosecution history.

i. The Claim Language

The phrase "said microprocessor and said devices each including an interface for receiving and transmitting data in packet form" appears in claims 14, 27–29, and 31–35. Having reviewed the claims, the Court concludes that the phrase is used consistently in each claim and is meant to have the same meaning in each claim. Regarding the second issue related to the shared interface, the Court finds that the plain language of the claims requires not only that the devices are "operable in conjunction with said microprocessor," but the claims also require that the microprocessor and the devices "each includ[e] an interface for receiving and transmitting data in packet form." Thus, the claim language requires that the microprocessor and each claimed device must have its own interface for receiving and transmitting data in packet form.

Regarding the first issue related to the physical incorporation, Plaintiff correctly contends that as a general matter of patent claim construction, "includes" and "comprising" are open-ended terms which are well understood to mean "including but not limited to." *Cias, Inc. v. Alliance Gaming Corp*., 504 F.3d 1356, 1360–61 (Fed. Cir. 2007); *Sandisk Corp. v. Memorex Prods., Inc.*, 415 F.3d 1278, 1284 (Fed. Cir. 2005) ("As a patent law term of art, 'includes' means 'comprising.'") (citations omitted). Thus, the Court agrees that the use of "including" in the claims is not a limiting term, and that the "elements" linked together by the term "including" can have additional elements, such as, connections.

Additionally, Plaintiff contends that claims 20 and 21 are dependent claims which further define the relationship of the interface to the functional unit, respectively, as either connected to or integrated within the functional unit. The '488 Patent specification supports these narrower claims because it discloses multiple arrangements of the interface and functional

unit that would fall within the embodiments claimed in dependent claims 20 and 21. *See e.g.*, '488 Patent, 9:28–40, Figs. 13, 14. Accordingly, the Court concludes that the claimed "interface" may be either connected to or integrated within the functional unit. *Phillips v. AWH Corp.*, 415 F.3d, 1303, 1314–15 (en banc) ("[T]he presence of a dependent claim that adds a particular limitation gives rise to the presumption that the limitation in question is not present in the independent claim."). The Court will now turn to the other intrinsic evidence.

ii. The Intrinsic Evidence

In addition to the claims, the other intrinsic evidence in this case, specifically the specification and prosecution history, supports the Court's construction. Regarding the first dispute related to the physical incorporation, the specification depicts and discusses embodiments of an interface (*i.e.*, link interface) that is separate from but connected to a functional unit, in addition to embodiments of an interface that is integrated within a functional unit. *See e.g.*, '488 Patent at 9:28–40, Figs. 13, 14.

Defendants do not dispute that the specification discloses these embodiment but instead argue that their proposed construction uses the word "including" exactly as the inventor used the word in the specification. Specifically, when referring to Figure 14, the specification describes the first interface as "include[d]" within the processor but is silent about the second interface. '488 Patent at 9:37–40. Thus, according to Defendants, because the inventor did not use "including" when referring to both of the illustrated interfaces, the claimed "interface" must be "included" or physically incorporated within the functional unit. The Court disagrees because "[a] claim construction that excludes a preferred embodiment . . . 'is rarely, if ever, correct.'" *Sandisk Corp.*, 415 F.3d at 1285 (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1583 (Fed. Cir. 1996)).

Plaintiff correctly notes that the language in the specification is "include[d] within the processor *silicon itself*." '488 Patent at 9:39–40 (emphasis added). Moreover, as discussed above, the claim language does not include the further qualification that the interface be included within the functional unit itself. Furthermore, the specification continues to state that "[i]t will be shown in the description to follow how the memory node interface may be extended to *include* any peripheral device." '488 Patent at 9:44–46 (emphasis added). The Court agrees that a person of ordinary skill in the art would not interpret this use of "include" to be restricted to "physically incorporating" a peripheral device into a memory node interface. Finally, Defendants failed to point to any evidence in the prosecution history that would warrant restricting the meaning of "including an interface for receiving and transmitting data in packet form" to a structure wherein a link interface is incorporated within the functional unit.

Regarding the second issue related to the shared interface, Defendants contend that the specification and file history make clear that each device must have its own interface. The Court agrees because in every disclosed embodiment, each claimed device has its own interface. *See* '488 Patent at Figs. 2, 24, 25. Plaintiff responds that Figure 24 of the '488 Patent explicitly discloses a configuration where one packet node (a device plus an interface) provides an interface for other devices. Plaintiff, however, does not provide any citation to the specification that confirms Plaintiff's theory.

Moreover, the patentee amended the claims during reexamination to emphasize that the claimed devices "each" include an interface. Specifically, the patentee canceled claim 1 and added new claims (14, 27, and 28) that require one interface for each claimed device, as illustrated below:

Claim 1 (canceled)	Claims 14, 27, 28, 31, 32, 33, 34, 35
said devices each being operable in conjunction with said microprocessor and including an interface for receiving and transmitting data in packet form	said devices each being operable in conjunction with said microprocessor, said microprocessor and said devices each including an interface for receiving and transmitting data in packet form

(Doc. No. 511-23 (Suppl. Am. in Consolidated *Ex Parte* Reexams., Control No. 90/008,106, at 2–3, 6–7 (Jan. 21, 2008))). These amendments recite that the microprocessor must include an interface and that "each" device must include its own interface. *Pfund v. United States*, 40 Fed. Cl. 313, 367 (Fed. Cl. 1998) ("In interpreting the scope of claims, [courts] should endeavor to give meaning to each claim term."). Thus, the patentee narrowed the claim scope during the reexamination, and the disputed phrase will not be construed to include a broader scope. *Elekta Instrument S.A. v. O.U.R. Scientific Int'l, Inc.*, 214 F.3d 1302, 1308 (Fed. Cir. 2000) ("Claims that have been narrowed in order to obtain issuance over the prior art cannot later be interpreted to cover that which was previously disclaimed during prosecution."). Finally, during the claim construction hearing, Plaintiff agreed with the Court that each claimed device must have its own interface. Accordingly, the Court does not adopt either side's construction but instead provides a construction that is consistent with the claim language, the specification, and the prosecution history

iii. Court's Construction

In light of the claim language, the specification, and the prosecution history, the Court construes **"said microprocessor and said devices each including an interface for receiving and transmitting data in packet form"** to mean **"each of the microprocessor, the random access memory device, the mass storage device, and the input-output port device has its own interface for receiving and transmitting data in packet form."**

c. "interface"

Disputed Claim Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction
"interface"	"a circuit that links a packet-based data channel to either a microprocessor or a device"	"a circuit that links a packet-based data channel to either a microprocessor or a device and that speaks the same language electrically and logically with each other such circuit"

The parties agree that the claimed "interface" is "a circuit that links a packet-based data channel to either a microprocessor or a device." Thus, the dispute is whether the claimed interfaces must "speak the same language electrically and logically with each other." Defendants contend that the interfaces must speak the same language based on the problem statement of the invention and statements made in the specification. Plaintiff responds that the portion of the specification referenced by Defendants is directed to a "packet node," not the claimed "interface," and that nothing in the intrinsic record justifies Defendants' attempt to further limit the meaning of the claimed interface. The Court agrees with Defendants. Accordingly, the Court finds that Defendants' proposed construction is consistent with the claim language, the specification, and the prosecution history.

i. The Claim Language

The term "interface" appears in claims 14, 16–17, 20–21, 27–29, 31–35, and 37. Having reviewed the claims, the Court concludes that the term is used consistently in each claim and is meant to have the same meaning in each claim. The Court also finds that the claim language recites an "interface for receiving and transmitting data in packet form." Thus, the data that is transmitted and received by the interface is in packet form. The Court will now turn to the

other intrinsic evidence.

ii. The Intrinsic Evidence

The other intrinsic evidence in this case, specifically the specification and prosecution history, supports the adoption of Defendants' construction. The specification states that "*[t]he present invention* applies a point-to-point packetized interconnection structure to facilitate communication between functional units (e.g., processor, memory, disk, I/O, etc.) within a PC." '488 Patent at 2:16–19 (emphasis added). The patentee accomplished this point-to-point packetized interconnection structure by using what the specification refers to as a packet node, which is the combination of a link interface and a functional unit. '488 Patent at 4:36, Fig. 2. Specifically, "[i]nterface **49**, which is the embodiment of *the present invention*, provides a seamless interface between functional unit **48** and the physical layer **50**. Physical layer **50** connects to any other packet node **51**, thereby, in conjunction with interface **49**, allowing communication between any group of functional units." '488 Patent at 4:37–43 (emphasis added). Thus, the invention purports to overcome the drawbacks associated with "defining handshaking and data size at the physical layer" by "eliminating the typical physical layer control signals of a bus and replacing them with link-layer control which is much more flexible." '488 Patent at 1:61–2:26.

To support their contention that the interface must speak the same language electrically and logically with each other, Defendants point to the following passage from the specification:

> *[T]he present invention* makes each node . . . interface with each other using a uniform packe[t] based message passing interface. *The invention creates packet nodes which speak the same language electrically and logically.* This simplifies communication and minimizes traditional handshaking and overhead.

'488 Patent at 4:44–50 (emphasis added). Defendants argue that their construction expressly

follows the language and teaching from the patent that each interface is required to "speak the same language electrically and logically." The Court agrees.

As an initial matter, the "use of the phrase 'the present invention' does not 'automatically' limit the meaning of claim terms in all circumstances, and . . . such language must be read in the context of the entire specification and prosecution history." *Netcraft Corp. v. eBay, Inc.*, 549 F.3d 1394, 1398 (Fed. Cir. 2008). Moreover, the Court must be careful "to avoid the danger of reading limitations from the specification into the claim." *Phillips*, 415 F.3d at 1323. In this case, however, the Court concludes that the patentee limited the scope of the claims by describing features as "the present invention."

The patentee's repeated use of the phrases "the present invention" and "the invention" in describing the claimed interface makes clear that the specification is describing the invention as a whole, and not merely referring to a particular embodiment. *See, e.g.*, *Netcraft Corp.*, 549 F.3d at 1398 ("[T]he common specification's repeated use of the phrase 'the present invention' describes the invention as a whole . . . ."); *Verizon Servs. Corp. v. Vonage Holdings Corp.*, 503 F.3d 1295, 1308 (Fed. Cir. 2007) ("When a patent thus describes the features of the 'present invention' as a whole, this description limits the scope of the invention."); *Honeywell Int'l, Inc. v. ITT Indus., Inc.*, 452 F.3d 1312, 1318 (Fed. Cir. 2006) (limiting claims to a fuel filter where "the written description refers to the fuel filter as 'this invention' or 'the present invention'"). For example, the specification describes the advantages of using packet nodes by stating that "*the present invention* allows for more intelligent and flexible information exchange between nodes while requiring only that overhead and handshaking required for a specific transaction." '488 Patent at 4:56–59 (emphasis added). This statement, taken in context with the portion of the specification relied on by Defendants, confirms that the claimed invention requires interfaces

that "speak the same language electrically and logically" because the goal of the "present invention" was to avoid imposing "a set of costly rules and formalism" that slow down communication. '488 Patent at 4:60–61.

Plaintiff responds that the portion of the specification relied on by Defendants does not define the claimed "interface" but instead relates to a packet node. As it relates to the present issue, this is a distinction without a difference because the specification defines a packet node as combination of the claimed "interface" and the claimed "devices" (*i.e.*, a functional unit). '488 Patent at 4:36, Fig. 2. Moreover, it is "[i]nterface **49**, which is the embodiment of *the present invention*, [that] provides a seamless interface between functional unit **48** and the physical layer **50**. Physical layer **50** connects to any other packet node **51**, thereby, in conjunction with interface **49**, allowing communication between any group of functional units." '488 Patent at 4:37–43 (emphasis added). Thus, it is the "interface" portion of each packet node that provides the "seamless interface," not the functional unit. Accordingly, one of ordinary skill in the art would understand that it is the interface that allows the packet nodes to "speak the same language electrically and logically."

Plaintiff also contends that Defendants' construction would ignore disclosed situations where interfaces would not "speak the same language electrically and logically." The Court disagrees. Defendants' construction does not require that the interfaces use a particular electrical voltage or exclude claimed devices that have different physical data widths. '488 Patent at 5:25–31, 6:8–10. Instead, Defendants' construction only requires that each interface speak the same language electrically and logically. Accordingly, the Court finds that Defendants' construction is consistent with the intrinsic evidence.

iii. Extrinsic Evidence

In addition to the intrinsic evidence, there is also extrinsic evidence that supports Defendants' construction. The inventor, Mr. Gautam Kavipurapu, testified that that the interfaces speak a common language by describing that "from a link interface to a link interface, you have *the same electrical and logical interface*" (Doc. No. 511-24 at 2 (Kavipurapu Tr. 453:9–21) (emphasis added))). This is consistent with a construction that requires each interface "speak the same language electrically and logically."

iv. Court's Construction

In light of the claim language, the specification, the prosecution history, and the extrinsic evidence submitted by the parties, the Court adopts Defendants' proposed construction and construes **"interface"** to mean **"a circuit that links a packet-based data channel to either a microprocessor or a device and that speaks the same language electrically and logically with each other such circuit."**

d. "a packet-based data channel extending between said microprocessor and said interfaces of said devices"

Disputed Claim Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction
"a packet-based data channel extending between said microprocessor and said interfaces of said devices"	"a circuit capable of transporting a packet-based message between a microprocessor interface and the interfaces of the devices"	"a packet-based data channel that extends from the microprocessor interface to the interfaces in the random access memory device, the mass storage device, and the input-output port device for carrying uniform packet types"

The parties' dispute is focused on two issues. The first issue is whether a single path must

extend between a microprocessor interface and the interfaces of each of the devices or whether the path need only extend between a microprocessor interface and *one* device interface. The second issue is whether the packet-based data channel must carry uniform packet types.

Regarding the first issue related to the extension of the path, Plaintiff contends that requiring the same single path between the microprocessor and each device is inconsistent with the '488 specification and would be limiting the data channel to one disclosed embodiment. Defendants respond that Plaintiff's construction is incorrect because it would allow the channel to transmit packets from the microprocessor interface to only one of the device interfaces and would not require transmission to all of the device interfaces. As discussed below, the Court finds merit in certain aspects of both sides' arguments. Accordingly, the Court will require that the data channel be capable of transporting packets between a microprocessor interface and *each* interface of the devices.

Regarding the second issue related to uniform packet types, Defendants contend that the packet-based data channel must carry uniform packets. Plaintiff responds that while a packet-based data channel certainly may carry uniform packet types, neither the claim language nor the prosecution history requires incorporation of this limitation into the claim. The Court agrees with Defendant and will require that the packet-based data channel transport uniform packet types. Accordingly, the Court does not adopt the parties' proposed construction but instead provides a construction that is consistent with the claim language, the specification, and the prosecution history.

i. The Claim Language

The phrase "a packet-based data channel extending between said microprocessor and said interfaces of said devices" appears in claims 14, 27–29, and 31–35. Having reviewed the claims,

the Court concludes that the phrase is used consistently in each claim and is meant to have the same meaning in each claim. The Court also finds that the claim language requires that the claimed interface must be capable of receiving and transmitting data in packet form. Further, the Court finds that the claim language requires that the packet-based data channel extends between the microprocessor and the interfaces of the devices, not just between the microprocessor interface and the interface of one device. Thus, the Court finds that Plaintiff's construction that would allow the channel to transmit packets from the microprocessor interface to only one device interface is not consistent with the ordinary and customary meaning of the claim language. The Court will now turn to the other intrinsic evidence.

ii. The Intrinsic Evidence

In addition to the claims, the other intrinsic evidence in this case, specifically the specification and prosecution history, supports the Court's construction. Regarding the first issue related to the extension of the path, the specification describes and illustrates a number of interconnect topologies for interconnecting more than two functional units. '488 Patent at 2:27–36. For example, Figure 24 illustrates a ring interconnect in which each link interface is connected to a neighboring node's link interface until the ring is closed. '488 Patent at 7:36–40, Fig. 24. The specification also illustrates another common interconnect topology referred to as a switch. '488 Patent at 7:50–63, Fig 25. Plaintiff contends that Defendants' construction would limit the data channel to the ring topology, thereby excluding the disclosed switch topology because the same single path would not extend between a microprocessor interface and the interfaces of each of the devices in the switch topology. The Court agrees with Plaintiff. Defendants have not pointed to any evidence that indicates why the claims should not cover this embodiment. In fact, Defendants argue that the switch configuration in Figure 25 is not

precluded by Defendants' proposed construction because the crossbar 68 creates a packet-based data channel that extends all the way between interfaces that speak the same language electrically and logically. Thus, the Court's construction is consistent with the arguments made by both sides because it requires a data channel capable of transporting packet between a microprocessor interface and each interface of the claimed devices.

Regarding the second issue related to uniform packet types, Defendants contend that the packet-based data channel must carry uniform packet types. As with the disputed term "interface," Defendants point to the following passage from the specification to support their argument:

> [T]he present invention makes each node … interface with each other *using a uniform packe[t] based message passing interface.* The invention creates packet nodes which speak the same language electrically and logically. This simplifies communication and minimizes traditional handshaking and overhead.

'488 Patent at 4:44–50 (emphasis added). Defendants contend that this emphasizes that the interfaces must use uniform packet types. Having considered all of the intrinsic evidence, the Court agrees. First, for the reasons discussed above, the Court finds that this passage is describing the invention as a whole. Moreover, the passage explicitly describes the interface as using "uniform [packet]." The use of uniform packets is important because it enables the present invention to overcome the drawbacks associated with "defining handshaking and data size at the physical layer" by "eliminating the typical physical layer control signals of a bus and replacing them with link-layer control which is much more flexible." '488 Patent at 1:61–2:26. It does this by creating a uniform packet based message passing interface that creates packet nodes that speak the same language electrically and logically, thereby simplifying communication and providing a significant increase in data-rate speed. '488 Patent at 4:44–56. Thus, the

specification describes that the invention, as a whole, uses uniform packet types because this eliminates the "handshaking" and "overhead" issues that the invention was designed to solve. *See* '488 Patent at 4:44–50, 4:63–5:19, 5:49–50. Thus, the Court's construction is consistent with the claim language, the specification, and the prosecution history.

iii. Extrinsic Evidence

In addition to the intrinsic evidence, extrinsic evidence also supports the Court's construction. Plaintiff previously submitted a declaration of Dr. Richard Belgard in support of its claim construction positions (Doc. No. 312-4 (Belgard Decl. (June 18, 2010))). In his declaration, Dr. Belgard concedes that in describing the problems in the prior art bus system "the inventor believed that by providing *uniform packet types*, his invention would eliminate the need for electrical handshake, or control signals" (Doc. No. 312-4 (Belgard Decl. at ¶ 85 (June 18, 2010)) (emphasis added)). Thus, while Dr. Belgard disagreed that the paragraph relied upon by Defendants "necessarily suggests that the packet-based data channel carries 'uniform data packets,'" he confirmed that a person of ordinary skill in the art would understand that the invention overcame the problems with the prior art by providing "uniform packet types" (Doc. No. 312-4 (Belgard Decl. at ¶¶ 85–85 (June 18, 2010))). This is consistent with a construction that requires "a data channel capable of transporting uniform packet types."

iv. Court's Construction

In light of the claim language, the specification, the prosecution history, and the extrinsic evidence submitted by the parties, the Court construes **"a packet-based data channel extending between said microprocessor and said interfaces of said devices"** to mean **"a data channel capable of transporting uniform packet types between a microprocessor interface and each interface of the devices."**

e. "packet-based data channel"

Disputed Claim Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction
"packet-based data channel"	"a circuit capable of transporting a packet-based message between one interface and another interface"	"a set of wires and associated components necessary for carrying packets, without dedicated wires for address or data signals"

The parties dispute whether the claimed "packet-based data channel" should be construed with the negative limitation of "without dedicated wires for address or data signals." Defendants contend that the negative limitation is warranted because Plaintiff's construction fails to define what distinguishes a packet-based data channel from other types of data channels. Defendants also argue that Plaintiff's construction allows for a "partial" data channel, which would not meet the "extending between" interfaces claim limitation. Plaintiff responds that the claim language itself unambiguously states that the data channel is a "packet-based" data channel. The Court agrees with Plaintiff and does not find that a negative limitation is warranted. Accordingly, for the following reasons and for the reasons stated above, the Court provides a construction that is consistent with the claim language, the specification, and the prosecution history.

i. The Claim Language

The phrase "packet-based data channel" appears in claims 14, 20, 23, 27–29, 31–35, and 39. Having reviewed the claims, the Court concludes that the phrase is used consistently in each claim and is meant to have the same meaning in each claim. The Court notes that the claim language itself recites that the data channel is a "packet-based" data channel. Accordingly, the Court is not persuaded by Defendants' argument that a negative limitation is required to distinguish the claimed data channel from other types of data channels. The Court will now

turn to the other intrinsic evidence.

ii. The Intrinsic Evidence

In addition to the claims, the other intrinsic evidence in this case, specifically the specification and prosecution history, confirms that a negative limitation is not warranted. Defendants first argue that Figure 13a illustrates that the packet-based data channel is composed of "wires" (shown as arrows) and associated components necessary for carrying packets. Moreover, Defendants argue that it is a fundamental characteristic of packet networks that address and data information are treated interchangeably and transmitted together over the same wires. Specifically, Defendants argue that the '488 Patent consistently shows address and data information being combined onto the same packet channel. *See, e.g.*, '488 Patent at Figs. 9, 20. Although these statements are true, it does not support inserting a negative limitation because such limitations, absent an explicit disavowal, are generally disfavored. *See Omega Eng'g, Inc, v. Raytek Corp.*, 334 F.3d 1314, 1332–33 (Fed. Cir. 2003) (noting that a negative limitation imposed by the district found no support in the claim language, the plain and ordinary meaning of the phrase, or in any express disclaimer within the specification).

Defendants do not point to any evidence that the patentee defined this data channel by what it is not. Instead, the specification and intrinsic evidence confirms that "a packet-based data channel" is a data channel capable of transporting a packet. For example, the packet-based data channel may include at least two signal wires in each direction as illustrated in Fig. 13a, but that does not limit the claimed invention to only two signal wires. Accordingly, the Court provides a construction that is consistent with the claim language, the specification, and the prosecution history.

iii. Court's Construction

In light of the claim language, the specification, and the prosecution history, the Court construes **"packet-based data channel"** to mean **"a data channel capable of transporting a packet."**

f. "packet"

Disputed Claim Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction
"packet"	"a message including payload data and the control data indicative of the intended recipient"	"a message, including payload data and control data, that contains all the necessary information for the intended receiver"

The parties agree that a "packet" is a message including payload data and control data. The parties also agree that packets are for an intended receiver/recipient. Thus, the dispute is whether the packet must "contain all the necessary information for the intended receiver" as Defendants contend. Defendants are correct that the patentee stated that the "each packet contains all the necessary information that is required for the intended receiver," but Defendants ignore the context of this statement. Accordingly, the Court finds that Plaintiff's proposed construction is consistent with and supported by the claim language, the specification, and the prosecution history.

i. The Claim Language

The term "packet" appears in claims 14–17, 20, 23, 27–35, and 39. Having reviewed the claims, the Court concludes that the term is used consistently in each claim and is meant to have the same meaning in each claim. The Court finds that the claim language recites that the microprocessor and devices each include an interface for communicating in packet form. Thus,

the claims support the parties' proposed construction that a packet is a message including payload data and control data and that packets are intended for a recipient. However, the claims are silent as to Defendants' language requiring the packet to include "all the necessary information that is required for the intended receiver." Accordingly, the Court finds that Plaintiff's proposed construction is consistent with the ordinary and customary meaning of the claim language as understood by one of ordinary skill in the art. The Court will now turn to the other intrinsic evidence.

ii. The Intrinsic Evidence

In addition to the claims, the other intrinsic evidence in this case, specifically the specification and prosecution history, supports the adoption of Plaintiff's construction. Figure 3 illustrates the structure of a packet, and the specification provides a number of general characteristics of an exemplary packet. '488 Patent at 5:45–65. The Court finds this discussion is consistent with the parties agreed construction that a packet is a message including payload data and control data and that packets are intended for a recipient. Importantly, the patentee states that that "[t]he above definitions may easily be changed without affecting the nature of the invention." *Id.* at 5:64–65. Thus, the Court concludes that the patentee did not set out to define "packet" any different from its plain and ordinary meaning.

Defendants, however, argue that the patentee acted as his own lexicographer and explicitly defined "packet" with the following statement:

> A packet node in the present invention communicates with another packet node using "packets." *Each packet contains all the necessary information that is required for the intended receiver* without the added overhead of setting up the receiver or formatting the data to a node-specific set up.

'488 Patent at 5:45–49 (emphasis added). But Defendants ignore the context of the statement. As

discussed above, the invention purports to overcome the drawbacks associated with "defining handshaking and data size at the physical layer" by "eliminating the typical physical layer control signals of a bus and replacing them with link-layer control which is much more flexible." '488 Patent at 1:61–2:26. Thus, the "necessary information" contrasts how the prior art bus system operated at the physical layer. Moreover, Defendants do not point to any evidence in the prosecution history where a definition of packets was restricted to "containing all the necessary information for the intended receiver." Accordingly, the Court finds that Defendants' proposed language is superfluous and would only confuse the jury.

iii. Extrinsic Evidence

The parties submitted a number of technical dictionary excerpts that included definitions for the term "packet." The definitions for "packet" provided in these dictionaries generally refer to payload data and control data, but none state that a packet "contains all the necessary information for the intended receiver" (*see e.g.*, Doc. No. 504-13 at 3 (IBM Dictionary of Computing (10th ed. 1993) (excerpt))). Accordingly, the Court finds that the patentee used the term "packet" consistent with its plain and ordinary meaning.

iv. Court's Construction

In light of the claim language, the specification, the prosecution history, and the extrinsic evidence submitted by the parties, the Court adopts Plaintiff's proposed construction and construes **"packet"** to mean **"a message including payload data and the control data indicative of the intended recipient."**

g. "a first buffer for queuing packets for a transmission"

Disputed Claim Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction
"a first buffer for queuing	Ordinary meaning, in the	"a first buffer for storing

packets for a transmission”	alternative: “a first buffer capable of storing two or more packets prior to transmission”	two or more packets until they are transmitted from the buffer onto the packet-based data channel”

The parties’ dispute is focused on two issues. The first issue is whether the first buffer must store more than one packet at a time. The second issue is whether the first buffer must only queue packets for transmission onto the packet-based data channel without some other intermediate activity (*e.g.*, further formatting or manipulation).

Regarding the first issue related to storing more than one packet, the Court finds Defendants’ argument are without merit. First, both sides have agreed that a “buffer” should be construed to mean “a storage element used to store data temporarily when sending data from one functional unit to another.” Defendants attempt to add a further limitation to this agreed construction under the guise of the term “queuing.” Specifically, Defendants argue that the entire concept of “queuing” means holding *at least two items*, in order, such that an item that arrives later will not pass an item that arrived earlier. Although the Court agrees that queuing means holding items in order of arrival, the Court disagrees that this requires the claimed buffer to always store “two or more packets.”

As described in the specification, the claimed buffer may operate in a first in, first out (FIFO) manner. ’488 Patent at 9:61–62. This means that the claimed buffer (*i.e.*, the storage element used to store data temporarily) may go from an empty state to a state of storing multiple items. This FIFO operation, however, does not require that the buffer always store two or more items because the buffer may be empty or contain only one item. Accordingly, the Court rejects Defendants’ argument.

Regarding the second issue, the Court disagrees that the claims bar some other intermediate activity between the buffer and the packet-based data channel. As discussed below, the claim language is unambiguous about the nature of the transmission described in the claim. Accordingly, the Court concludes that a construction is not necessary for this disputed phrase, especially given the parties' agreed construction for the term "buffer."

i. The Claim Language

The phrase "a first buffer for queuing packets for a transmission" appears in claims 14, 27–29, 31, and 33–35. Having reviewed the claims, the Court concludes that the phrase is used consistently in each claim and is meant to have the same meaning in each claim. The Court also finds that the claim language states that the buffer is for queuing packets "for" a transmission. Because the claims use the term "comprising," the claim language does not exclude further formatting or manipulation of the data before it is placed onto the packet-based data channel. Instead, the claims require that the first buffer provide the order that the packets will be transmitted on the packet-based data channel. Accordingly, given the claim language, the Court finds that no construction is necessary for this disputed phrase. A jury will understand that the first buffer queues the packets for a transmission. The Court will now turn to the other intrinsic evidence.

ii. The Intrinsic Evidence

In addition to the claims, the other intrinsic evidence in this case supports the Court's conclusion that no construction is necessary. As discussed, Defendants' construction adds an unwarranted temporal limitation because it excludes any intermediate steps before the transmission occurs. Defendants fail to point to any substantive evidence to justify adding this limitation. Instead, Defendants only point to Plaintiff's characterization of the first buffer as a

"transmit buffer" in the prosecution history to support their construction. However, there is nothing in the intrinsic record that shows packets are transmitted by buffers onto the packet-based data channel. Indeed, the examiner confirmed this conclusion when he stated that "a buffer is a region of memory storage. It is not a transmitter that can retransmit its content" (Doc. No. 504-15 at 4 (Office Action dated May 26, 2010 at ¶7)). In other words, the claimed first buffer establishes the order of transmission but not the manner of transmission. This is consistent with the construction the parties agreed to for the term "buffer" as "a storage element used to store data temporarily."

During the claim construction hearing, Defendants argued that the phrase should be construed to prevent Plaintiff from arguing that the first buffer and second buffer may be arranged in a serial configuration. Such an alignment is contrary to Figure 9, which illustrates the first and second buffer in a parallel configuration. The Court agrees with Defendants' argument but finds that the plain and ordinary meaning of this disputed phrase, in conjunction with the Court's construction of the disputed phrase "a second buffer for storing a copy of a packet transmitted," properly addresses this issue. Thus, the Court need not construe the "first buffer" phrase. Accordingly, the Court concludes that the disputed "first buffer" phrase is unambiguous, is easily understandable by a jury, and requires no construction. Therefore, the phrase **"a first buffer for queuing packets for a transmission"** will be given its **plain meaning** to one of ordinary skill in the art.

h. "a second buffer for storing a copy of a packet transmitted"

Disputed Claim Term	**Plaintiff's Proposed Construction**	**Defendants' Proposed Construction**
"a second buffer for storing a copy of a packet transmitted"	Ordinary meaning, in the alternative: "a second buffer capable of temporarily storing	"a second buffer, separate from the first buffer, for storing only copies of

	a copy of a packet transmitted"	packets already transmitted from the first buffer onto the packet-based data channel"

The parties dispute whether the second buffer only stores packets previously transmitted by the first buffer or whether the second buffer can store packets before they are transmitted by the first buffer. Plaintiff contends that the copy of a packet stored in the second buffer may be created before the "original" packet has been transmitted (*i.e.*, before the original packet has left the first buffer). Defendants respond that the claim language and intrinsic evidence confirms that the second buffer only stores packets previously transmitted by the first buffer. The Court generally agrees with Defendants and adopts a modified version of their construction that is consistent with the claim language, the specification, and the prosecution history.

i. The Claim Language

The phrase "a second buffer for storing a copy of a packet transmitted" appears in claims 14, 27–29, 31, and 33–35. Having reviewed the claims, the Court concludes that the phrase is used consistently in each claim and is meant to have the same meaning in each claim. The Court finds that the claim language recites that the second buffer is separate from the first buffer. The claim language also recites "a second buffer for storing a copy of a packet *transmitted* by said first interface." By using the past tense, the claims recite that the packets have already been "transmitted" by the first interface. Plaintiff contends that the claim language "for storing" means that the second buffer is capable of storing packets that have already been transmitted but it does not exclude the capability to store such copies before transmission. The Court disagrees. The patentee could have drafted the claim without the "transmitted" language. Accordingly, the Court finds that Defendants' proposed construction is consistent with the ordinary and

customary meaning of the claim language as understood by one of ordinary skill in the art. The Court will now turn to the other intrinsic evidence.

ii. The Intrinsic Evidence

In addition to the claims, the other intrinsic evidence in this case, specifically the specification and prosecution history, supports the adoption of Defendants' construction. Plaintiff contends that Defendants' construction is limited to a "serial" arrangement (requiring that the first buffer be in-line with the second buffer), which would exclude a preferred embodiment from the claim scope. Specifically, Figure 9 depicts an embodiment that has a "parallel" arrangement for the packet to be transmitted showing a communication path from a first buffer ("Request Queue") to a second buffer ("Echo Waiting Queue") and a communication path from the first buffer to another interface.

Defendants respond that their construction is entirely consistent with Figure 9. The Court agrees. As stated in Plaintiff's opening brief, the parties are in agreement that the "Echo Waiting Queue" is claimed as the "second buffer" (Doc. No. 504 at 21). The specification states that a request "is queued in the echo waiting queue" (the second buffer) "*[o]nce any request has been sent out*." '488 Patent at 9:67–10:1 (emphasis added). Thus, Defendants' construction is consistent with Figure 9 and the specification, which describes transmitting packets from the first buffer ("Request Queue") and providing copies of "outstanding" packets, in parallel, to the second buffer ("Echo Waiting Queue"). '488 Patent and 8:45–49; 9:67–10:1.

Moreover, Defendants point to statements made by the patentee during the file history to support their construction. Defendants argue that during reexamination, the patentee distinguished prior art that allowed for the storage of packets before being transmitted. Specifically, the prior art used a "sliding window implementation" in a single "transmit buffer"

holding both "packets that have been transmitted, and packets that have yet to be transmitted" (Doc. No. 511-30 at 18–19 (Am. in Consol. Reexam.) (emphasis added)). To distinguish this prior art, the patentee argued to the USPTO that this was different from the '488 Patent because "the transmit interface disclosed by the '488 Patent makes use of two buffers[:] a Request Queue for holding packets for transmission, as well as an Echo Waiting Queue that holds only those packets *that have already been transmitted* by the Request Queue." (Doc. No. 511-30 at 18–19 (Am. in Consol. Reexam.) (emphasis added)). The Court agrees that Defendants' construction is consistent with the statements made to the USPTO to distinguish the invention from the prior art.

Finally, during the claim construction hearing, the Court proposed its construction to the parties. Defendants stated they could agree with the Court's construction if the Court were to adopt their proposed construction for the disputed "first buffer" phrase. For the reasons stated above, the Court finds that its construction for this disputed phrase, in conjunction with the plain and ordinary meaning of the disputed "first buffer" phrase, properly addresses the issues raised by the parties and does not require the Court to construe the "first buffer" phrase.

iii. Court's Construction

In light of the claim language, the specification, and the prosecution history, the Court adopts a modified version of Defendants' proposed construction and construes **"a second buffer for storing a copy of a packet transmitted"** to mean **"a second buffer, separate from the first buffer, for storing copies of packets that have already been transmitted from the first buffer."**

i. "cache"

Disputed Claim Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction
"cache"	Ordinary meaning, in the alternative: "a circuit for temporarily storing data"	"a section of fast memory that stores frequently used data until it is full and then replaces old data with more recently requested data"

The parties' dispute is focused on three issues. The first issue is whether the cache must be "fast" memory. Plaintiff contends that "fast" memory introduces unnecessary ambiguity into the claim. The Court agrees and finds that the claim language itself provides for Defendants' "fast" memory construction. The second issue is whether the cache is limited to storing only "frequently used data." Plaintiff contends that not all caches are limited to storing only "frequently used data." The Court agrees with this statement, but Defendants' construction is not limited to only storing frequently used data. It also allows for storing other data (*e.g.*, pre-fetched data). The third issue is whether the cache must "store frequently used data until it is full." Plaintiff contends that there are different types of caches, and requiring the cache to "store frequently used data until it is full" would exclude one cache type described in the specification. The Court agrees. Accordingly, the Court provides a construction that is consistent with the claim language, the specification, and the prosecution history.

i. The Claim Language

The term "cache" appears in claims 32 and 35. Having reviewed the claims, the Court concludes that the term is used consistently throughout the claims and is meant to have the same meaning. Claim 35 specifies that the cache is included in the microprocessor interface, stores a quantity of data requested from one of the devices, and is organized with a variable line size

adjusted dynamically based on changes in hit rate. Thus, the claim language captures the "fast" memory aspect of Defendants' construction because the cache is included in the microprocessor interface itself. Similarly, the claim language supports a construction that includes storing frequently used data because the claim requires the cache to store data requested from one of the devices. Finally, the claim language is silent as to whether the cache must store frequently used data until it is full. Accordingly, the Court finds that its construction is consistent with the plain and ordinary meaning of the claim language as understood by one of ordinary skill in the art. The Court will now turn to the other intrinsic evidence.

ii. The Intrinsic Evidence

In addition to the claims, the other intrinsic evidence in this case supports the Court's construction. First, Defendants contend that Plaintiff's construction is so broad that it would encompass almost any form of memory, including the "main memory," "buffers," and "mass storage device" that the '488 Patent identifies as separate elements. The Court agrees and finds that Plaintiff's construction would not help the jury understand the differences between the claimed cache and the other claimed devices. Indeed, during the claim construction hearing, Plaintiff conceded that its proposed construction is broad and would read on other claimed memory devices (*e.g.*, random access memory device, mass storage device). Although the Court agrees with Defendants' argument, it does not adopt Defendants' construction because it goes too far.

First, Defendants argue that a cache must "store frequently used data until it is full." The parties do not dispute that this is a characteristic of a particular type of cache that is commonly referred to as "fully associative" (*see, e.g.*, Doc. No. 504-2 at 25, ¶64 (Dec. of William Mangione-Smith)). Fully associative caches allow data to be stored at any location

within the cache (Doc. No. 504-2 at 25, ¶64 (Dec. of William Mangione-Smith)). In contrast, "direct-mapped" or "set-associative" caches restrict where a particular piece of data can reside within a cache and typically require cache management before the cache is full (Doc. No. 504-2 at 25, ¶64 (Dec. of William Mangione-Smith)). Thus, Defendants' construction is not consistent with a direct-mapped cache, which is described as an embodiment of the linc cache. Specifically, the specification states that the "[l]inc cache **63** is basically a directed [sic] mapped cache for caching response data for the functional unit." '488 Patent at 8:63–64. Accordingly, the Court will not include Defendants' "until it is full" language in its construction because it is not consistent with a "direct-mapped" cache.

Defendants also contend that it is well document that a cache stores data until it is full and replaces old data with more recently requested data. However, none of the definitions for cache included in the extrinsic evidence provided by the parties, or even the definition quoted by Defendants in their brief, specify that the cache *must* "store data until it is full and replaces old data with more recently requested data." Although the Court recognizes that a cache must have some mechanism for replacing data, the Court does not find that Defendants' proposed language is necessary for its construction. Moreover, Defendants point to no intrinsic evidence that would compel the Court to include this language in its construction. The Court will now turn to the extrinsic evidence submitted by the parties.

iii. Extrinsic Evidence

In addition to the intrinsic evidence, there is also extrinsic evidence that supports the Court's construction. First, the Court finds that the definitions for cache provided in the extrinsic evidence commonly references frequently used data (*see, e.g.*, Doc. No. 511-6 at 3 (*Dictionary of Computer Words* 34 (rev. ed. 1995)); Doc. No. 511-8 at 3 (*Prentice Hall's*

Illustrated Dictionary of Computing 73 (2d ed. 1995))). Plaintiff's basis for opposing this language is that not all caches are limited to storing only "frequently used data." To be clear, the Court's construction does not require that the cache store only frequently used data, but also allows the cache to store other data (e.g., pre-fetched data). *See, e.g.*, '488 Patent, 11:15–20. Accordingly, in order to help the jury understand the difference between a "cache" and the other claimed elements (*e.g.*, "main memory," "buffers," "mass storage device"), the Court's construction includes "frequently used data."

This conclusion is also consistent with the testimony of Plaintiff's expert, Mr. William Henry Mangione-Smith. Mr. Mangione-Smith agreed that it would be fair to characterize the cache's intent as storing frequently used data. Doc. No. 511-19 at 13 (Mangione-Smith Tr. 172:20–23). Accordingly, the Court's construction that requires the cache to store "frequently used data" is consistent with the extrinsic evidence submitted by the parties.

iv. Court's Construction

In light of the claim language, the specification, the prosecution history, and the extrinsic evidence submitted by the parties, the Court construes "cache" to mean "a section of memory that temporarily stores frequently used data."

j. "linc cache"

Disputed Claim Term	**Plaintiff's Proposed Construction**	**Defendants' Proposed Construction**
"linc cache"	Ordinary meaning in the context of the claim language, in the alternative: "a circuit that contains a first memory block for storing recently received data and a second memory block for storing additional data related to said received data"	"a single link-layer cache"

The parties dispute whether "linc cache" should be construed as "a single link-layer cache." Plaintiff contends that Defendants' construction introduces unnecessary ambiguity to the claim and could improperly limit the claim to exclude systems using more than one "linc cache." Defendants respond that the patentee made clear and unequivocal statements to the USPTO that a "linc cache" is a single link-layer cache. The Court agrees with Defendants and finds that their proposed construction is consistent with the claim language, the specification, and the prosecution history.

i. The Claim Language

The phrase "linc cache" appears in claim 32. Having reviewed the claim, the Court concludes that the phrase is used consistently throughout the claim. Plaintiff contends that the remainder of the claim language sufficiently and unambiguously defines the meaning of the phrase "linc cache." Specifically, Plaintiff argues that the claim language describes the "linc cache" as follows: (1) included in the microprocessor interface; (2) used for storing data requested by the microprocessor from at least one of said devices (*i.e.*, random access memory device, mass storage device and/or input-output port device); and (3) made up of at least two memory blocks—one block for storing at least data most recently requested (by the microprocessor) and one block for storing data not most recently requested. The Court agrees with Plaintiff's summary of the claim elements but finds that it does not take into account the statements made to the USPTO that describe the linc cache as a single link-layer cache. Moreover, Plaintiff's proposed construction does not provide any guidance to the jury because it only repeats the elements of the claim. The Court will now turn to the other intrinsic evidence.

ii. The Intrinsic Evidence

The other intrinsic evidence in this case, specifically the prosecution history, supports the adoption of Defendants' construction. Defendants contend that during the reexamination, the patentee explicitly defined the "linc cache" to mean a single link-layer cache. Specifically, Defendants point to the following statement:

> The '488 linc cache defines a hardware-controlled data cache that is *incorporated at the link layer* in each node of a *packet-based* computer bus. This hardware cache implementation is a non-obvious design choice and represents a valid patent claim.

(Doc. No. 511-5 (Gardner Decl. ¶ 50) (emphasis added)). Using this statement, the patentee then distinguished three prior art references on the ground that they did not disclose a *link-layer* cache. Specifically, Defendants point to the following arguments made by the patentee to the USPTO:

1) "Yoshizawa's "link cache" . . . does not teach the structural and functional limitations of *the link-layer cache in '488*" (Doc. No. 511-5 (Gardner Decl. at ¶ 63) (emphasis added)).
2) "A local memory cache is at a higher layer in the OSI communications model and is *fundamentally different from cache at the link layer* of the communications channel" (Doc. No. 511-5 (Gardner Decl. at ¶ 57) (emphasis added)).
3) "Since Yoshizawa . . . does not use packets, does not operate as a bus interface, and *does not operate at the link layer of a communications system*, a person of ordinary skill in the art would not look to Yoshizawa . . . to arrive at the linc cache invention of '488" (Doc. No. 511-5 (Gardner Decl. at ¶ 64) (emphasis added)).
4) "A software disk cache like Holzhammer's has to operate *at a communications layer higher than the link layer implementation of the '488 patent*" (Doc. No. 511-5 (Gardner Decl. at ¶ 74) (emphasis added)).

Similarly, Defendants point to the patentee's repeated statements to the USPTO that its "linc cache" is a single cache, not a combination of two separate caches (*see* Doc. No. 511-10 at 75 (Patent Owner's Appeal Brief (Feb. 8, 2011)) ("[T]he specification of the '488 Patent, in

every instance, depicts and/or discusses the link cache of the claimed invention as **single cache**, and not as two separate caches."); Doc. No. 511-12 at 25 (Resp. in '376 Reexam. (Nov. 11, 2009)); Doc. No. 511-13 at 51–52 (Resp. in '376 Reexam. (May 14, 2010)); Doc. No. 511-34 (Belgard Decl. ¶¶ 14, 15, 38); Doc. No. 511-14 at 42–43 (Resp. in '376 Reexam. (July 26, 2010)); Doc. No. 511-3 (Reinman Decl. ¶¶ 216–18)).

Plaintiff contends that the USPTO expressly rejected these characterization as not supported by either the specification or the claim language. This argument is without merit because the patentee representation is binding regardless of whether the USPTO accepted the patentee's argument. *Am. Piledriving Equip., Inc. v. Geoquip, Inc.*, 637 F.3d 1324, 1336 (Fed. Cir. 2011) (finding disclaimer based on statements with which "examiner explicitly disagreed"); *Lifestream Diagnostics, Inc. v. Polymer Tech. Sys., Inc.*, 109 F. App'x 411, 414–16 (Fed. Cir. 2004) ("We agree with the district court that arguments deliberately and repeatedly advanced by the patent applicant in regard to the scope of a claim term during prosecution may be used for purposes of claim construction even though the Patent Office rejected the arguments."). Accordingly, the Court agrees with Defendants and finds that the patentee defined the "linc cache" to mean "a single link-layer cache" given the repeated statements made to the USPTO during the reexaminations.

Finally, Plaintiff's argument that this construction could improperly limit the claim to exclude systems using more than one "linc cache" is unfounded. Defendants' construction only requires that the linc cache must be a single cache and not the combination of two or more caches. In other words, while the system may have multiple linc caches, there must be at least one linc cache that contains the two required blocks in a single cache. Accordingly, the Court adopts Defendants' construction.

iii. Court's Construction

In light of the claim language, the specification, and the prosecution history, the Court construes a "linc cache" to mean "a single link-layer cache."

k. "said linc cache comprising first and second memory blocks"

Disputed Claim Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction
"said linc cache comprising first and second memory blocks"	Ordinary meaning in the context of the claim language, in the alternative: "a circuit that contains a first memory block for storing recently received data and a second memory block for storing additional data related to said received data"	"the linc cache contains two blocks with fixed locations, each of which has identical functionality but stores different data"

The parties' dispute is focused on two issues. The first issue is whether the "first and second memory blocks" of the linc cache must have fixed locations. The second issue is whether the "first and second memory blocks" of the linc cache must have identical functionality. Regarding the first issue related to the fixed locations, Defendants argue that the claim language dictates that the locations of the first and second memory blocks of the linc cache are fixed. The Court is not persuaded by Defendants' argument because their construction is based on pure speculation that the "patentee must have meant the two-block limitation to mean something other than what every cache already has" (Doc. No. 511 at 28). Accordingly, the Court rejects Defendants' argument because the addition of the "fixed locations" limitation is not supported by the claim language, the specification, or the prosecution history.

Regarding the second issue related to identical functionality, Defendants contend that the intrinsic evidence requires that the first and second memory blocks have identical caching

functionality. The Court agrees with Defendants on this issue and adopts a modified version of Defendants' construction.

i. The Claim Language

The phrase "said linc cache comprising first and second memory blocks" appears in claim 32. Having reviewed the claim, the Court concludes that the phrase is used consistently throughout the claim. As with the term "linc cache," Plaintiff contends that the remainder of the claim language sufficiently and unambiguously defines the meaning of this phrase and that no separate definition is required for this phrase. The Court agrees that the claim further defines the disputed phrase but finds that this alone would not capture the statements made to the USPTO that further define the disputed phrase. Moreover, Plaintiff's proposed construction does not provide any guidance to the jury because it merely repeats the elements of the claim. The Court will now turn to the other intrinsic evidence.

ii. The Intrinsic Evidence

Defendants contend that the intrinsic evidence requires that the first and second memory blocks have identical caching functionality (although they may store different data).[2] Specifically, Defendants point to the portion of the specification that states that "the Linc Cache 63 is partitioned into two identical blocks." '488 Patent at 8:63–9:3. Defendants further point to arguments made by the patentee in the prosecution history. During the reexamination, the patentee argued that a prior art reference was "different from the dual-block design of '488," because the '488 Patent's linc cache "divides a cache into two parts with identical functionality" (Doc. No. 511-5 (Gardner Decl. ¶ 80)). Plaintiff responds that Defendants seek

[2] During the claim construction hearing, Defendants agreed that their proposed language of "but stores different data" was not necessary for the construction of this disputed phrase.

to impose additional unstated limitations into the claim and Defendants' additional limitations are not only unnecessary but also introduce ambiguity into the claim. The Court disagrees. Accordingly, the Court concludes that the patentee defined the "first and second memory blocks" as "two blocks with identical functionality" as indicated in the intrinsic record.

iii. Court's Construction

In light of the claim language, the specification, and the prosecution history, the Court construes "said linc cache comprising first and second memory blocks" to mean "the linc cache contains two blocks with identical functionality."

l. "said first memory block storing a first portion of said stored data comprising the data most recently requested"[3]

Disputed Claim Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction
"said first memory block storing a first portion of said stored data comprising the data most recently requested"	Ordinary meaning, in the alternative: "a first memory block capable of storing the data most recently requested"	"the first memory block always stores the data most recently requested"

The parties dispute whether the linc cache's first memory block must "always" store the data most recently requested. Plaintiff contends that the claim language is unambiguous in its meaning. Defendants respond that the intrinsic evidence uniformly describes the first memory block as storing the data most recently requested. The Court agrees with Defendants' argument but finds that this is captured by the plain and ordinary meaning of the disputed phrase. The phrase requires that the first memory block store a first portion of the stored data "comprising the

[3] The phrase "said first memory block storing a first portion of said stored data comprising the data most recently requested" appears in claim 32.

data most recently requested."

Defendants also contend that their "always stores" construction is compelled by the patentee's statement to the USPTO. During reexamination, the patentee argued that the link cache's dual-block design allowed simultaneous access to both blocks, "with one block *always having the* latest data and the other block being one access behind" (Doc. No. 511-5 (Gardner Decl. ¶ 80) (emphasis added)). The Court has reviewed the claims in light of this intrinsic evidence and concludes that the claim language faithfully captures the statements made by the patentee to the USPTO. Moreover, the Court concludes that the disputed phrase is unambiguous, is easily understandable by a jury, and requires no construction. Therefore, the phrase "said first memory block storing a first portion of said stored data comprising the data most recently requested" will be given its plain meaning to one of ordinary skill in the art.

m. "the balance of said stored data"

Disputed Claim Term	**Plaintiff's Proposed Construction**	**Defendants' Proposed Construction**
"the balance of said stored data"	Ordinary meaning, in the alternative: "additional data related to the received data"	"all of the stored data except the data most recently requested"

The parties dispute whether the term "balance" should be replaced with "all of the stored data except the data most recently requested."[4] Plaintiff contends that the claim language is clear enough that the ordinary meaning should be applied. Defendants respond that Plaintiff's alternative construction ignores the word "balance" and could allow the second memory block to store some "stored data" but not necessarily the "balance of said stored data." Defendants' argument is unfounded because Plaintiff's primary position is for the plain meaning of the

[4] The phrase "the balance of said stored data" appears in claim 32.

disputed phrase, which includes the word "balance." Defendants fail to point to any evidence that would justify significantly redrafting one term in the disputed phrase. Moreover, the Court concludes that the disputed phrase is unambiguous, is easily understandable by a jury, and requires no construction. Therefore, the phrase "the balance of said stored data" will be given its plain meaning to one of ordinary skill in the art.

n. Agreed Constructions

In addition to the above disputed terms, the parties have come to several agreed constructions. Based upon the joint submission of a claim construction chart, the parties agree to the construction of the following terms. These constructions are therefore adopted by the Court:

Claim Term/Phrase	Location	Agreed Construction
"buffer"	14, 17, 27, 28, 29, 31, 33, 34, 35	"a storage element used to store data temporarily when sending data from one functional unit to another"
"parallel data/address bus circuit"	20	"a circuit having multiple address, data and control lines"
"switching means"	24	Function: selectively connecting said microprocessor to selected ones of said devices Structure: a ring and a switch and/or crossbar interconnect ('488 Patent, Figs. 24, 25; Col. 7, Lines 36–63 at
"a quantity of data requested from one of said devices"	32, 35	"a quantity of data requested by the microprocessor from one of the devices"
"physical address"	33, 34	"an address corresponding to a physical memory location or a particular functional unit"
"virtual address"	34	"a non-physical memory address that can be converted to a corresponding physical address to access data in physical memory"

"translation lookaside buffer"	34	"a memory that stores the physical address associated with each virtual address"
"hit rate"	35	"a measure of how often data requested by the microprocessor is in the cache"
"said cache being organized with a variable line size"	35	"the amount of data corresponding to a cache tag is variable"
"said cache being organized with a variable line size adjusted dynamically based on changes in hit rate"	35	"the amount of data corresponding to a cache tag is variable, and is adjusted dynamically based on changes in hit rate"

a. "for providing simultaneous bi-directional communication between said microprocessor and said devices"[5]

Prior to the claim construction hearing, the parties disputed whether packet-based data channel must provide simultaneous bi-directional communication between the microprocessor and all of the devices, or whether it needs to provide communication between the microprocessor and only one of the claimed devices. The Court reviewed the intrinsic evidence and concluded that Defendants' proposed construction was ambiguous on its face and that Plaintiff's proposed construction was broader than the scope of the claims.

As with the disputed phrase "said microprocessor and said devices each including an interface for receiving and transmitting data in packet form," the Court concluded that the bi-directional communication must be capable of extending from a microprocessor to each interface because every disclosed embodiment illustrates a data path channel extending to each device. *See* '488 Patent at Figs. 2, 24, 25. However, the Court also concluded that the claims do not require that the simultaneous bi-directional communication between the microprocessor and each

[5] The phrase "for providing simultaneous bi-directional communication between said microprocessor and said devices" appears in claims 14, 27-29, and 31-35.

of the multiple devices must occur at the same time. For example, Figure 24 illustrates a ring interconnect where "each link interface's physical link output is connected to a neighboring nodes link interface physical input until the ring is closed." '488 Patent at 7:37–40, Fig. 24. This embodiment confirms that while the communication between the microprocessor and any one device must be simultaneous bi-directional communication, the simultaneous bi-directional communication between the microprocessor and more than one device may occur at the same time or different times. In other words, there would be no need to circulate or forward the packet from one interface in the ring to another interface in the ring if the claims required the bi-directional communication to occur at the same time to each device.

Thus, during the claim construction hearing, the Court proposed a construction to the parties that is consistent with the claim language, the specification, and the prosecution history. The parties agreed with the construction presented by the Court. Accordingly, the Court adopts the parties' agreed construction and construes "for providing simultaneous bi-directional communication between said microprocessor and said devices" to mean "for providing simultaneous bi-directional communication between the microprocessor and each of the devices."

V. CONCLUSION

For the forgoing reasons, the Court adopts the constructions as set forth above, and as listed in the attached chart. The parties are ordered that they may not refer, directly or indirectly, to each other's claim construction positions in the presence of the jury. Likewise, the parties are ordered to refrain from mentioning any portion of this opinion, other than the actual definitions adopted by the Court, in the presence of the jury. Any reference to claim construction

proceedings is limited to informing the jury of the definitions adopted by the Court.

It is SO ORDERED.

SIGNED this 7th day of June, 2013.

MICHAEL H. SCHNEIDER
UNITED STATES DISTRICT JUDGE

APPENDIX A

Claim Term/Phrase	Location	Court's Construction
"microprocessor"	14, 24, 27-29, 31-35, 37	"a central processing unit residing within a single chip"
"[a] physically non-distributed microprocessor-based computer system"	14, 27-29, 31-35	"a microprocessor-based computer system in which all the components are close to one another and contained within a single enclosure"
"said microprocessor and said devices each including an interface for receiving and transmitting data in packet form"	14, 27-29, 31-35	"each of the microprocessor, the random access memory device, the mass storage device, and the input-output port device has its own interface for receiving and transmitting data in packet form"
"interface"	14, 16-17, 20-21, 27-29, 31-35, 37	"a circuit that links a packet-based data channel to either a microprocessor or a device and that speaks the same language electrically and logically with each other such circuit"
"a packet-based data channel extending between said microprocessor and said interfaces of said devices"	14, 27-29, 31-35	"a data channel capable of transporting uniform packet types between a microprocessor interface and each interface of the devices"
"packet-based data channel"	14, 20, 23, 27-29, 31-35, 39	"a data channel capable of transporting a packet"
"packet"	14-17, 20, 23, 27-35, 39	"a message including payload data and the control data indicative of the intended recipient"
"a first buffer for queuing packets for a transmission"	14, 27-29, 31, 33-35	No construction necessary
"a second buffer for storing a copy of a packet transmitted"	14, 27-29, 31, 33-35	"a second buffer, separate from the first buffer, for storing copies of packets that have already been transmitted from the first buffer"

"cache"	32, 35	"A section of memory that temporarily stores frequently used data"
"linc cache"	32	"a single link-layer cache"
"said linc cache comprising first and second memory blocks"	32	"the linc cache contains two blocks with identical functionality"
"said first memory block storing a first portion of said stored data comprising the data most recently requested"	32	No construction necessary
"the balance of said stored data"	32	No construction necessary
"for providing simultaneous bi-directional communication between said microprocessor and said devices"	14, 27-29, 31-35	**[Agreed]** "for providing simultaneous bi-directional communication between the microprocessor and each of the devices"
"buffer"	14, 17, 27, 28, 29, 31, 33, 34, 35	**[Agreed]** "a storage element used to store data temporarily when sending data from one functional unit to another"
"parallel data/address bus circuit"	20	**[Agreed]** "a circuit having multiple address, data and control lines"
"switching means"	24	**[Agreed]** Function: selectively connecting said microprocessor to selected ones of said devices Structure: a ring and a switch and/or crossbar interconnect ('488 Patent at Figs. 24, 25; Col. 7, Lines 36-63)
"a quantity of data requested from one of said devices"	32, 35	**[Agreed]** "a quantity of data requested by the microprocessor from one of the devices"

“physical address”	33, 34	**[Agreed]** “an address corresponding to a physical memory location or a particular functional unit”
“virtual address”	34	**[Agreed]** “a non-physical memory address that can be converted to a corresponding physical address to access data in physical memory”
“translation lookaside buffer"	34	**[Agreed]** “a memory that stores the physical address associated with each virtual address”
“hit rate”	35	**[Agreed]** “a measure of how often data requested by the microprocessor is in the cache”
“said cache being organized with a variable line size”	35	**[Agreed]** “the amount of data corresponding to a cache tag is variable”
“said cache being organized with a variable line size adjusted dynamically based on changes in hit rate”	35	**[Agreed]** “the amount of data corresponding to a cache tag is variable, and is adjusted dynamically based on changes in hit rate”