IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

PACT XPP TECHNOLOGIES, AG	§	
	§	
v.	§	Case No. 2:07-CV-563-RSP
	§	
XILINX, INC., et al.	§	

MEMORANDUM ORDER

Before the Court are Defendants' equitable defenses of laches and unclean hands. For the following reasons, the Court rejects both defenses.

FINDINGS OF FACT AND CONCLUSIONS OF LAW

A. Lawsuit and the Asserted Patents

This lawsuit was filed by PACT XPP Technologies, AG against defendants Xilinx, Inc. and Avnet, Inc. (collectively, "Defendants") on December 28, 2007. In May 2012, a jury found that Defendants infringe claims 1, 3, 17, and 30 of the '181 patent and claim 8 of the '106 patent.

United States Patent No. 6,119,181 issued on September 12, 2000 from a United States patent application filed on October 8, 1997, which in turn claims the benefit of a German patent application filed on December 20, 1996.

United States Patent No. 6,338,106 issued on January 8, 2002 from a United States patent application filed on June 18, 1999. The '106 patent claims the benefit of the application that issued as the '181 patent as well as the German patent application filed on December 20, 1996.

B. Infringing Products

At trial, PACT demonstrated that Defendants infringe the asserted claims by making, using, selling, and offering for sale Virtex-II Pro, Virtex-4, Virtex-5 and Virtex-6 FPGAs, or actively induced such infringement. PACT's expert Dr. Tredennick testified that each of the infringing products infringe the asserted patents because they contain a RocketIO, EMAC, or

PCIe unit. Dr. Tredennick explained to the jury how each RocketIO, EMAC, and PCIe unit independently infringes the asserted claims.

Dr. Tredennick offered detailed and persuasive testimony as to how each RocketIO, EMAC, and PCIe unit meets all of the limitations of the asserted claims, which included the following limitations: (1) "bus system"; (2) "interface"/"interface unit"; (3) "providing communication"/"combines multiple units"; (4) "multidimensional programmable cell architecture"; (5) "state machine"; (6) "address generator"; (7) "dynamically reconfigurable cells"; (8) "first bus"; (9) "interface unit being configured by at least one of a primary logic unit and the processing unit"; and (10) "register indicating whether data is stored in the at least one interface."

The Virtex-II Pro FPGA was introduced by Xilinx in 2002. The Virtex-II Pro FPGA was the first FPGA to have the infringing RocketIO feature. Xilinx describes the Virtex-II Pro as a "breakthrough" and "one of the most significant product introductions . . . since inventing the FPGA in 1984." PX431 at XL00227532. Dr. Tredennick testified that the RocketIO permitted the Xilinx FPGAs to be used in a "lot larger range of applications." The Virtex-4 FPGA was introduced by Xilinx in 2004. The Virtex-4 FPGA was the first FPGA to have the infringing EMAC feature and the DSP48. The Virtex-5 FPGA was introduced by Xilinx in 2006. The Virtex-5 FPGA was the first FPGA to have the infringing PCIe feature. Finally, the Virtex-6 FPGA was introduced in 2009. The Virtex-6 FPGA includes a RocketIO, an EMAC and a PCIe features.

C. Laches

1. Applicable Law

Laches is an equitable defense that applies to claims of patent infringement. *A.C. Aukerman Co. v. R.L. Chaides Constr. Co.*, 960 F.2d 1020, 1032 (Fed. Cir. 1992) (en banc). In

applying the defense, "[a] court must look at all of the particular facts and circumstances of each case and weigh the equities of the parties." (*Id.* at 1032.) In order to invoke laches, a defendant must prove that: (1) the plaintiff delayed filing suit for an unreasonable and inexcusable length of time from the time the plaintiff knew or reasonably should have known of its claim against the defendant, and (2) the defendant has been or will be prejudiced in a significant way due to the plaintiff's delay in filing the lawsuit. *A.C. Aukerman Co. v. R.L. Chaides Constr. Co.*, 960 F.2d 1020, 1032 (Fed. Cir. 1992) (en banc). The defendant must prove delay and prejudice by a preponderance of the evidence. *Id.* at 1045.

"The length of time which may be deemed unreasonable has no fixed boundaries but rather depends on the circumstances." *Id.* at 1032. Facts and circumstances that can justify a delay can include, during the period of delay: (1) being involved in other litigation; (2) being involved in negotiations with the alleged infringer; (3) poverty or illness; (4) wartime conditions; (5) being involved in a dispute about ownership of the patent; or (6) minimal amounts of allegedly infringing activity by the alleged infringer. *Id.* at 1033.

Material prejudice may be economic or evidentiary. *Id.* at 1043. Economic prejudice is determined by whether or not the alleged infringer changed its economic position in a significant way during the period of delay resulting in losses beyond merely paying for infringement and also whether the alleged infringer's losses as a result of that change in economic position likely would have been avoided if the patentee had filed this lawsuit sooner. *Id.* at 1033. Evidentiary prejudice "may arise by reason of a defendant's inability to present a full and fair defense on the merits due to the loss of records, the death of a witness, or the unreliability of memories of long past events, thereby undermining the court's ability to judge the facts." *Id.*

If suit was delayed for six years, a rebuttable presumption arises that the delay was unreasonable and unjustified, and that material prejudice resulted. *Id.* at 1034-35. This presumption shifts the burden of proof to the plaintiff to come forward with evidence to prove that the delay was justified or that material prejudice did not result. *Id.* Such evidence "must be sufficient to put the existence of a presumed fact into genuine dispute." *Id.* at 1037. If the plaintiff presents such evidence, then the burden of proving laches remains with the defendant.

However, "the establishment of the factors of undue delay and prejudice, whether by actual proof or by the presumption, does not mandate recognition of a laches defense in every case. Laches remains an equitable judgment of the trial court in light of all the circumstances." *Id.* at 1036.

2. PACT did not have actual or constructive knowledge of infringement before December 28, 2001, and no presumption of laches applies.

a. PACT did not have actual or constructive knowledge of Defendants' infringement of the '106 patent before December 28, 2001 because the '106 patent had not yet issued.

The '106 patent issued on January 8, 2002, which is less than six years before this lawsuit was filed. Because the laches period cannot begin until after the issuance of the patent (*Auckerman*, 960 F.2d at 1032), no presumption of laches can arise with respect to the '106 patent. Moreover, PACT did not have actual or constructive knowledge of Defendants' infringement before December 28, 2001 because the '106 patent had not yet issued.

b. PACT did not have actual or constructive knowledge of Defendants' infringement of the '108 patent before December 28, 2001.

The '181 patent issued in 2000. In order for the presumption of laches to arise, Defendants must show that PACT knew or should have known of Defendants' infringement by no later than December 27, 2001. Defendants contend that PACT had actual or constructive knowledge of Defendants' infringement before December 28, 2001 because (1) PACT knew or

should have known that Xilinx's pre-2002 products infringe, and (2) PACT's October 2001 Business Plan shows that PACT knew or should have known of Xilinx's infringement.

i. Xilinx's Pre-2002 Products

Because the infringing products were not introduced until after 2002, Defendants must show that PACT's knowledge of earlier Xilinx products should be "tacked on" to the delay period. Plaintiff's delay in filing suit may be measured from the plaintiff's knowledge of a product pre-dating the accused products if that earlier product was the "same or similar" to the accused product and thus "embodied the same claimed features as the accused product." *See Symantec Corp. v. Computer Associates Int'l, Inc.*, 522 F.3d 1279, 1295 & n.9 (Fed. Cir. 2008).

Defendants contend that PACT knew or should have known of Xilinx's pre-2002 products (such as Xilinx's 4000EX FPGA) that are the "same or similar" to the infringing products. Defendants contend that the pre-2002 products contained a serializer/deserializer and therefore "embodied the same claimed features as the accused products."

Xilinx's 4000EX FPGA was developed in 1995. Dr. Steven Trimberger was the architect of the 4000EX. Dr. Trimberger testified that the 4000EX contained an IO block that was given the marketing name "SelectIO." Dr. Trimberger testified that the SelectIO contained a serializer and a deserializer.[1] Dr. Trimberger testified that he filed for a patent on serializer/deserializer technology for an FPGA in 1995. Dr. Trimberger's application issued as the '367 patent.[2]

[1] On cross-examination, Dr. Trimberger admitted that the circuit he referred to as a "serializer" was in fact a "multiplexer," and that the circuit he identified as a "deserializer" was in fact a "flip flop." The Court is giving Dr. Trimberger the benefit of the doubt in concluding that a multiplexer is a "serializer" and that a flip-flop is a "deserializer."

[2] Dr. Trimberger admitted that the terms "serializer" and "deserializer" are not used in the '367 patent, and that symbols for a "serializer" and a "deserializer" do not appear in the patent.

Assuming that the 4000EX FPGA contains a "serializer" and a "deserializer," the Court finds that notice of the "serializer" and "deserializer" alone does not support a reasonable belief that the 4000EX FPGAs fall within the scope of the '181 and '106 patents. PACT's expert Dr. Tredennick testified that the serializer and deserializer in the infringing products are a "permanent implementation of a bus system control inside the RocketIO." But that testimony applies only to the Court's claim construction of one limitation (namely, "interface unit"). (Claim Construction Order at 20, Dkt No. 201.) It is well settled that to prove infringement, every element and limitation of a claim must be found in the accused device, literally or under the doctrine of equivalents. Here, the infringed patent claims recite a number of limitations, and "interface unit" is just one of them.[3]

Moreover, PACT likely would not have been suspicious of a serializer or deserializer standing alone because, as Mr. Vorbach admitted, serializers and deserializers predate the '181 and '106 patents. Indeed, the Hartenstein Paper was admitted as prior art at trial (Dkt No. 373 at 8) and explicitly teaches a "serializer." Yet Defendants chose not to present an invalidity theory based upon the Hartenstein Paper. This suggests that Defendants appreciated that the "serializer" in the Hartenstein Paper, standing alone, does not establish that the Hartenstein Paper teaches the claimed inventions in PACT's '106 and '181 patents. The Court finds that the 4000EX likewise does not teach the claimed inventions in PACT's '106 and '181 patents merely by virtue of purportedly having a "serializer" or "deserializer."

[3] In Defendants' motion for judgment as a matter of law of no infringement, Defendants argue that there was no substantial evidence that the infringing products met nine separate claim limitations. Defendants have made no attempt to show that any more than one limitation may have been met by the pre-2002 Xilinx products.

The Court also finds that PACT did not have actual knowledge of the presence of the "serializer" and "deserializer" in the pre-2002 products, and cannot be reasonably charged with constructive notice of that fact.

Defendants contend that "PACT's founders and employees were reading about, writing about, and working with Xilinx FPGAs since at least 1996." None of the evidence cited by Defendants reflects any awareness by PACT's employees of the 4000EX or the '367 patent, or that they knew that the 4000EX or '367 patent disclosed a "serializer" or "deserializer." But even assuming contrary to the record that PACT's employees were aware of the 4000EX or the '367 patent, the Court finds based on the above it would not have justified any suspicion of infringement on PACT's part.

Defendants have not identified any publicly available evidence for the 4000EX, or any other pre-2002 product, that discloses the "serializer" and "deserializer." The only evidence offered at trial came from the testimony of two of Xilinx's witnesses.

ii. PACT's October 2001 Business Plan

Defendants contend that the October 2001 Business Plan shows that PACT believed that Xilinx was infringing the '181 or '106 patents before December 28, 2001.

In October 2001, PACT compiled a business plan for use in presentations to potential investors and other companies. (DX71.) Defendants point to this document as evidence that PACT was aware of Xilinx's infringing activity more than six years before filing suit. (DX71 at 47 ("PACT detected major infringements at least at the following companies and the users of their products: . . . Xilinx . . . .").) However, the 2001 Business Plan does not indicate (1) who drafted the "major infringements" language; (2) what analysis, if any, was performed; (3) whether the "major infringements" related to PACT's patents in the United States or some other country; (4) if United States patents were involved, which United States patent(s) were analyzed;

or (5) which target products were analyzed. The later PACT business plans (DX644 and DX153) include the same language Xilinx relies upon and suffer from the same deficiencies.

The Court finds that the October 2001 Business Plan cannot relate to the '106 patent because it did not issue until 2002, and cannot relate to the infringing products because they were not introduced until 2002.

The Court also finds that there is no evidence suggesting that the "major infringements" referred to in the 2001 Business Plan related to the '181 patent. The October 2001 Business Plan lists all forty worldwide patents in PACT's portfolio at the time, and it makes no specific accusations of infringement as to any one of those patents. (DX71 at 45-47.) Defendants have offered no reason to believe that the "major infringements" analysis, if any, related to the '181 patent as opposed to one of the other forty PACT patents.

Other documentary evidence strongly suggests that PACT did not believe that Xilinx was infringing the '181 patent or '106 patent at the time. For example, Mr. Vorbach prepared a presentation entitled "One Standard for the World." (DX83.) This presentation was likely generated around 2003. (Vorbach Dep. at 1017-1018:6.) On page 4 of the presentation, Mr. Vorbach compares PACT's technology to "FPGAs," and mentions Xilinx's patents in connection with this FPGA discussion. Mr. Vorbach concludes "[n]o mutual patent infringement known," (*id.*), indicating his subjective belief that there was then no patent infringement between PACT and makers of FPGAs. (Vorbach Dep. at 1018:11-15.)

This presentation then goes on to discuss PACT's patent portfolio stating:

- PACT owns base patents on
  - coarse grained configurable devices
  - advanced reconfiguration technics
- Not used by FPGA suppliers yet

(DX83 at 4.) This discussion ("Not used by FPGA suppliers yet") further evidences that PACT had no subjective suspicion in 2003 that FPGA manufacturers (like Xilinx) were using its patented technology. (Vorbach Dep. at 1019:15-1020:20.)

In 2004, PACT compiled a "Matrix of Possible Patent Infringement." (DX50.) The matrix lists PACT's patent families by their internal nomenclature (PACT01, PACT02, etc.). The matrix shows that PACT suspected that Xilinx's customers, but not Xilinx itself, might be infringing the PACT03 family. (*Id.*) This reference to PACT03 is not necessarily even a citation to the '181 and '106 patents because the PACT03 family included additional patents. (*See* 5/14 a.m. Tr. at 135:22-136:5.) The document shows that PACT did not have a strong opinion that Xilinx was likely infringing '181 or '106 patents.

Accordingly, the Court finds that the 2001 Business Plan does not show that PACT had actual or constructive knowledge of Xilinx's infringement of the '181 or '106 patents.

c. Conclusion

The Court finds that PACT did not know, nor should have known, of Defendants' infringement of the '106 or '181 patents before December 28, 2001. The Court also finds that no presumption of laches applies.

3. PACT did not have actual or constructive knowledge of infringement between December 28, 2001 and early 2007.

From 2001 to 2006, PACT set up a series of meetings with Xilinx to explore combining PACT and Xilinx technology. During that time, PACT had at least ten meetings with 15 to 20 employees of Xilinx, in which they discussed both PACT's technology and Xilinx's products, including the accused Virtex-4.

In 2001, PACT met with Chris Dick of Xilinx to discuss integrating PACT's technology into Xilinx's products. In 2002, PACT again contacted Xilinx and proposed including its technology in Xilinx's FPGAs. PACT and Xilinx ultimately met in September 2002.

In 2003, PACT again contacted Xilinx to discuss incorporating PACT technology into Xilinx's products. PACT and Xilinx met in September 2003.

In 2005, PACT again contacted Xilinx to discuss incorporating PACT technology into Xilinx's products. During a 2005 meeting, PACT gave a presentation specifically proposing integrating PACT technology into the accused Virtex-4, which contained both RocketIO units and DSP48s:

> **Q.** Let's take a look at one of the attachments, DX 164. And if you look at the front there, the title is XPP Integration into Virtex-4. What does that mean, integration into Virtex-4?
>
> **A.** So that basically means that this is a proposal to add their technology into our Virtex-4 product.
>
> **Q.** And the Virtex 4 product -- I guess I should ask you, see the date there, September 13th, 2010? That's actually a print date. Do you understand that?
>
> **A.** Yeah. I was informed about that.
>
> **Q.** That's actually—that was a presentation that went along with that April 11th, 2005 e-mail?
>
> **A.** Yes, sir.
>
> **Q.** All right. So at this time, they're asking to integrate—proposing to integrate their technology into your Virtex-4 chip?
>
> **A.** Yes, sir.
>
> **Q.** And your Virtex-4 chip is the one that has the RocketIO on it, the DSP48s?
>
> **A.** Yes, sir. That's correct.
>
> **Q.** And the EMAC block?

A. Yes. That's correct, sir.

(5/17 p.m. Trial Tr. 36:11–37:10.)

As part of the 2005 meetings between PACT and Xilinx, Xilinx provided PACT with confidential benchmark data comparing the accused Virtex-4's performance to PACT's claimed performance. During the 2005 meetings, Xilinx alleges that it discussed the RocketIO units with PACT. During its discussions with Xilinx between 2001 and 2006 about integrating its technology into Xilinx's products, the parties agree that PACT never told Xilinx that it had any belief that Xilinx's products (or Xilinx's users) infringed PACT's patents.

PACT repeatedly highlighted the differences between Xilinx's and PACT's technology in an effort to convince Xilinx to add PACT technology to its products. (5/17 p.m. Tr. 42:2–9 ("Q. All right. At any time during these four to five years, did PACT ever say that you were using their technology? A. No, sir. They never said that. Q. Did they ever say that you were using their patents? A. No, sir. They kept on coming back and say their technology was different and better than ours.").)

At trial, Xilinx argued that the foregoing evidence showed that PACT had knowledge of Xilinx's infringing products, but nonetheless failed to warn Xilinx of their infringement. Mr. Vorbach credibly explained that PACT did not have a correct understanding of Xilinx's products, and believed that Xilinx was using a "fine-grained" design as opposed to the "coarse-grained" design necessary for infringement. The Court finds that Mr. Vorbach's explanation is reasonable and credible, and is further evidence that PACT did not have actual or constructive knowledge of Xilinx's infringement.

The evidence showed that FPGAs are highly flexible integrated circuits that may be configured and reconfigured to serve different applications. An FPGA cam be configured to work in an automobile and then reconfigured to work in an aircraft. FPGAs achieve this

flexibility by providing a large number of individual "low level blocks" known as configurable logic blocks ("CLBs"). Each CLB can be configured to perform one of several functions and can be interconnected with other CLBs using wiring known as a general routing matrix ("GRM"). Although individual CLBs can perform only relatively simple functions, the FPGA as a whole can be configured to perform much more complex functions by appropriately interconnecting and setting the functions of groups of CLBs.

CLBs are "fine grained" circuits. (5/14 p.m. Tr. 73:15-24, 116:7-9.) PACT's bus interface, in contrast, is "coarse-grained." (5/15 a.m. Tr. 32:16-23; 5/14 p.m. Tr. 116:2-22; *see also* 5/14 p.m. Tr. 72:24-73:24; 115:23-118:21 (contrasting coarse grain and fine grain).) Xilinx understood that the '181 and '106 patents related to "coarse grain" technology. (5/17 p.m. Tr. 76:11-18.)

Prior to 2007, Mr. Vorbach and PACT misunderstood the design of Xilinx's infringing products. (5/14 p.m. Tr. 74:18-25, 86:12-19, 87:1-16; 105:5-22; 114:12-115:2; 79:9-80:5; 83:25-84:3.) Specifically, PACT believed that Xilinx's infringing products were fine-grained devices. (5/14 p.m. Tr. 116:4-24, 117:14-17, 143:12-21; 5/15 a.m. Tr. 32:24-33:25, 34:5-24; Vorbach Dep. at 865:22-866:21.) Therefore, Mr. Weber, Mr. Vorbach and PACT did not believe Xilinx was infringing. (Vorbach Dep. at 436:16-21; Weber Dep. at 343:9-12; 5/14 p.m. Tr. 176:11-18; 187:9-188:3; 188:20-189:11.) Beginning in 2003, PACT began trying to convince Xilinx to incorporate PACT's coarse-grained technology into what Mr. Vorbach believed were Xilinx's fine-grained products. (5/14 p.m. Tr. 143:12-21.) In 2007, PACT learned for the first time that Xilinx's FPGAs were actually using coarse-grained interface units. (5/15 a.m. Tr. 34:11-17; 36:7-11.) Specifically, Mr. Vorbach became aware that Xilinx's new FPGA product lines infringed the PACT patents while conducting a "coarse review" of Xilinx products, shortly

before PACT contacted its attorneys. (Vorbach Dep. 242:2-19, 371:17-372:7, 425:15-429:25, 436:16-437:4; 927:7-22; Weber Dep. 113:7-13, 114:10-21, 119:1-18; 125:5-126:18; 127:4-13.)

PACT's misconception of how Xilinx's products functioned was known to Xilinx as early 2003. Despite having knowledge of PACT's misunderstanding, the evidence shows that Xilinx never told PACT that it misunderstood the design of Xilinx's products or provided sufficiently detailed information necessary to know of the infringement.

PX468 is an email that Mr. Vorbach sent to Dr. Bolsens at Xilinx in 2003. In the email, Mr. Vorbach proposed adding PACT's "coarse grain" technology to Xilinx's "fine grain" products:

> We should figure out whether a cooperation (on any level) between XILINX and PACT would make sense. PACT believes that a combined device having XILINX's fine grained structure and PACT's coarse grained array could be positioned very successful at the market.

(PX468.)

Defendants contend that the infringing features were present in Xilinx's devices as early as 1995 and would have been well established in Xilinx devices by 2003. If this were true, it seems unlikely that Mr. Vorbach would characterize Xilinx's devices as having a "fine grained structure." The Court finds that the most reasonable inference that can be drawn from this statement is that PACT believed at the time that Xilinx devices had a fine grained structure and were not infringing.

In any event, the recipient of the email, Dr. Ivo Bolsens, was the chief technology officer of Xilinx and understood the difference between "fine-grained" and "coarse-grained" architectures. Dr. Bolsens himself used the phrase "coarse-grained" in his own emails. (PX112; 5/17 p.m. Tr. 75:10-25.) Dr. Bolsens did not, after receiving this email or at any point thereafter,

correct Mr. Vorbach and inform him that Xilinx's products were more "coarse-grained" than Mr. Vorbach understood. (5/15 a.m. Tr. 33:13-25; 5/14 p.m. Tr. 117:14-21.)

Dr. Bolsens' testimony that he discussed the RocketIO technology with Mr. Vorbach does not establish that PACT had sufficient knowledge of Xilinx's products to know they were infringing. Dr. Bolsens did not testify that he provided sufficiently detailed technical information to give PACT actual or constructive knowledge that the RocketIO technology infringes. To the extent that Dr. Bolsens' account conflicts with Mr. Vorbach's account, the Court is convinced that the properly jury credited Mr. Vorbach's testimony over Dr. Bolsens', as does the Court.

The Court finds that the 2004 Matrix of Possible Infringement prepared by PACT is further evidence that PACT was not aware of the infringement because of its misconception that Xilinx's products were "fine grained." (DX50.) Referring to Xilinx, PACT stated: "Fine grained reconfigurable architecture (FPGA). Will require coarse grained structures in future." (*Id.*)

The Court has considered DX48/912 and finds that it, even in combination with the other documentary evidence, does not show that PACT knew or should have known of PACT's infringement. DX48/912 demonstrates, at best, that PACT engineers had reviewed Xilinx's product documentation, and were aware that the DSP48 units were present in Xilinx's products. However, there has been no showing that infringement could be ascertained or reasonably suspected from a review of Xilinx's public documentation. Moreover, the DSP48 only satisfies the "dynamically reconfigurable cells" limitation, which is only one of many claim limitations.

The Court finds that the remaining evidence cited by Defendants does not prove that PACT knew or should have known of Xilinx's infringement of the '181 and '106 patents. There

is more than sufficient evidence to corroborate Mr. Vorbach's explanation for why PACT did not know of Xilinx's infringement until just before filing suit.

The Court finds that the evidence only supports Defendants' contention that PACT knew of Xilinx's infringement if one draws all inferences in favor of Defendants. Much of the evidence recounted by the parties' in their proposed findings of fact and conclusion of law was presented to the jury in the context of PACT's claims for induced infringement and willful infringement. At the trial, Defendants forcefully argued that they did not know (and should not have known) that their acts infringed PACT's patents. Defendants relied heavily on the fact that PACT did not accuse Xilinx of infringement prior to suit, despite having business discussions stretching back over five years. Having put the issue front and center before the jury, the Court can only conclude that the jury resolved the issue against the Defendants and chose to accept PACT's view of the evidence in light of the jury's verdict. Moreover, the Court agrees with the jury's assessment that the evidence supports PACT's account.

The Court finds that PACT did not have actual or constructive knowledge of Defendants' infringement between December 28, 2001 and early 2007.

4. PACT did not unreasonably and inexcusably delay the filing of this lawsuit.

In order to invoke laches, Defendants must first prove that PACT delayed filing suit for an unreasonable and inexcusable length of time from the time the PACT knew or reasonably should have known of its claim against the Defendants. The Court finds that PACT did not know, nor should have known, of Defendants' infringement until just before this lawsuit was filed in 2007. Therefore the Court finds that factor for laches is not satisfied.

However, even if PACT had actual or constructive knowledge of Defendants' infringement before 2007, the delay in filing of this lawsuit would have been excusable and reasonable in light of the course of conduct between the parties.

From 2001 to 2006, PACT and Xilinx had periodic meetings to discuss entering a business arrangement. Had a deal been consummated, PACT likely would not have any viable claims for patent infringement because Xilinx would have likely insisted on any necessary patent licenses or would have received patent licenses by operation of law. Therefore, it would be reasonable to not initiate litigation until business discussions were completed. Even if PACT had learned of Xilinx's infringement during the period of discussions, the delay between the end of the discussions in August 2006 and the filing of suit in December 2007 would have been reasonable.

Finally, any delay would also be excusable because Xilinx's silence contributed to delaying PACT's recognition of Defendants' infringement.

5. Defendants have not suffered any prejudice from delay.

The Court finds that Defendants have not shown that they have suffered any prejudice from any reasonable or unreasonable delay in bringing this lawsuit.

a. Defendants have not demonstrated that they suffered any evidentiary prejudice.

Defendants argue that they have been prejudiced because PACT lost or caused the destruction of evidence that Xilinx could have relied on in this case. The Court finds that the cited evidence and argument are unpersuasive.

In light of the Court's finding that PACT did not have actual or constructive knowledge of Defendants' infringement until just prior to filing this lawsuit, PACT did not have any obligation to preserve documents because litigation was not then foreseeable. Moreover, the Court finds that there is no evidence to suggest that the documents related to Xilinx were accorded any less protection than any other business records in PACT's custody.

Despite the admitted loss of some documents, PACT produced a significant amount of documentary evidence from its own files. A number of those documents have been used by Xilinx to support its case. Xilinx has not offered any credible suggestion of what the lost documents might show that is not cumulative of the documents that have already been produced.

For example, with respect to the allegedly lost[4] email from Martin Vorbach to Markus Weinhardt, Xilinx argues that the email would have shown that Mr. Vorbach sent a copy of a Xilinx user manual to PACT's engineers. However, other emails showed that PACT looked at Xilinx's documentation, and PACT's witnesses freely admitted to looking at Xilinx's documentation. Although Xilinx has copies of all its documentation, Xilinx has failed to point to a single publicly available document that would have given PACT knowledge of Xilinx's infringement.

The Court finds that Defendants' conclusory allegation that "key testimony" has been lost as witnesses have passed away, left the company, or have simply forgotten past events is not persuasive. Xilinx had numerous employees present during various phases of the discussions with PACT, and only identifies Erich Goetting as a potential witness who became unavailable during the alleged delay. However, Xilinx makes no suggestion of what testimony Mr. Goetting could have offered that is not cumulative of the testimony available from other key witnesses such as Dr. Bolsens or Mr. Vorbach.

The Court finds that Mr. Vorbach and Mr. Weber lost some documents because of hard disk drive "crashes." The Court finds that Mr. Vorbach and Mr. Weber acted in good faith in

[4] Xilinx maintains that Mr. Vorbach must have sent an email to Mr. Weinhardt to prompt Mr. Weinhardt to send DX48/912 to Mr. Vorbach. The Court is not convinced that Mr. Vorbach ever sent such a message.

attempting to salvage the hard disk drives, and that their efforts were reasonable in light of the circumstances.

The Court finds that Defendants did not suffer any prejudice from PACT's exercise of its rights to demand the destruction of PACT's confidential information under the non-disclosure agreement drafted by Xilinx. At the time of the demand, PACT did not have chargeable knowledge of Xilinx's infringement, and had no reason to suspect that litigation may become necessary. Defendants fail to identify any prejudice from the destruction of PACT's confidential information. A number of the documents provided by PACT during the discussions have been produced, and Xilinx has contended that nothing in the documents provided by PACT during the discussions suggested that PACT believed Xilinx was infringing PACT's patents. Therefore, Xilinx has not articulated any prejudice that resulted from the destruction of the PACT's confidential information. Moreover, the Court finds that Xilinx did not fully comply with the request and improperly retained some of PACT's confidential information.

Finally, the Court finds that PACT did not exploit the loss of any relevant evidence in its arguments to the jury. Moreover, Defendants did not object to the argument, nor did they seek any pretrial relief (such as a sanction or simply an order in limine) even though Defendants knew that the lack of documentary evidence to substantiate Defendants' claim that PACT knew of Xilinx's infringement would be at issue.

The Court finds that Defendants have not suffered any evidentiary prejudice due to any delay in bringing this lawsuit.

b. Defendants have not shown that they suffered any economic prejudice.

Defendants contend that they suffered economic prejudice as a result of PACT's delay in filing suit. Defendants argue that they invested millions in technology licenses and development

costs in designing the accused products. Defendants argue that they could have implemented a non-infringing alternative had they known of PACT's infringement claims sooner.

The Court finds that Xilinx has not suffered any economic prejudice. First, Defendants argue that they spent millions to develop the accused products, and yet also argue that the infringing features had been designed and present in their products since 1995. This cuts against their argument that Xilinx changed its position in reliance on PACT's delay in bringing suit. Moreover, there is no competent evidence that there is a commercially viable non-infringing alternative. Although a non-infringing alternative would be relevant to the damages issue in this case, Xilinx chose not to present one. There is no evidence to suggest how much money a non-infringing alternative would cost to implement. Finally, the Court and the jury found that Xilinx has willfully infringed the asserted patents. Despite having knowledge of its infringing acts, Xilinx never attempted to stop its infringement -- by either removing the infringing features entirely or by implementing a non-infringing alternative.

6. It would inequitable to apply laches in light of Defendants' failure to timely disclose its factual basis supporting laches.

The Court finds that Defendants have failed to properly disclose its laches defense. First, Defendants rely on Xilinx's 4000EX FPGA and the '367 patent to show that PACT knew or should have known of Defendants' infringement. However, that evidence was relevant to invalidity, and the Court has previously found that Xilinx consciously decided not to timely disclose its contention that the 4000EX and the '367 patent disclose PACT's invention. For Xilinx's failure to timely disclose that evidence, it was excluded from trial. The Court finds that it would be inequitable to allow Defendants to base their laches defense on evidence that was otherwise excluded.

The Court has also reviewed Defendants' most recent interrogatory response concerning Defendants' laches defense. The Court finds that Defendants' response failed to properly disclose a number of their contentions that they now argue supports laches. The Court is persuaded that PACT was prejudiced by Defendants' failure to properly disclose the basis for the laches defense by depriving PACT of an opportunity to develop facts to rebut Defendants' contentions during discovery. The Court finds that it would be inequitable to apply a laches defense when the basis for the defense was not properly disclosed during discovery.

7. Avnet has not shown that it entitled to assert its own laches defense.

Laches is a defense that is personal to a party. Although Avnet has joined Xilinx in urging a laches defense, their proposed findings of fact and conclusions of law center entirely around PACT's knowledge of Xilinx's activities. Defendants have not offered any facts on which to find that PACT knew or should have known of its claim against Avnet. Defendants have offered no evidence that PACT even knew or should have known of the existence of Avnet, much less its infringement. Finally, Defendants have not offered any facts on which to find that Avnet was prejudiced by any purported delay in the filing of this lawsuit. Therefore, the Court finds that Avnet has not offered any evidence or argument sufficient to show that it is entitled to assert a laches defense.

8. Conclusion

For the foregoing reasons, the Court rejects Defendants' laches defense.

D. Unclean Hands

1. Applicable Law

The equitable doctrine of unclean hands bars a party from asserting claims where that party engaged in litigation misconduct. *See Aptix Corp. v. Quickturn Design Sys.*, 269 F.3d 1369, 1374–75 (Fed. Cir. 2001). The unclean hands doctrine is "not bound by formula or

restrained by any limitation that tends to trammel the free and just exercise of discretion." *Keystone Driller Co. v. Gen. Excavator Co.*, 290 U.S. 240, 245–46 (1933).

A finding of unclean hands may be warranted when a party has engaged in litigation misconduct. *See Aptix Corp.*, 269 F.3d at 1376. The spoliation of evidence, especially document destruction, is a basis for unclean hands. *See Samsung Elecs. Co., Ltd. v. Rambus, Inc.*, 523 F.3d 1374, 1376-77 (Fed. Cir. 2008). However, the Federal Circuit has explained that "[d]ismissal is a 'harsh sanction,' to be imposed only in particularly egregious situations where 'a party has engaged deliberately in deceptive practices that undermine the integrity of judicial proceedings.'" *Micron Technology, Inc. v. Rambus Inc.*, 645 F.3d 1311, 1328-29 (Fed. Cir. 2011). Dismissal should only be imposed if there is "clear and convincing evidence of both bad-faith spoliation and prejudice to the opposing party." *Id.*

2. Defendants have not shown clear and convincing evidence of bad-faith spoliation or prejudice.

As explained above, the Court found that PACT did not know of Defendants' infringement, or contemplated litigation, at the time PACT exercised its right to demand the return of its confidential information under Xilinx's form non-disclosure agreement. As also recounted above, the Court finds that the Defendants have failed to show any prejudice from the destruction of those documents.

The Court has also found that PACT unintentionally lost some documents stored on hard disk drives that crashed in 2005, 2006, and 2007. The Court found that PACT made a reasonable effort to recover those documents. The Court finds that there has been no demonstrable prejudice from the loss of the documents.

Finally, the Court finds that there is no clear and convincing evidence that PACT deliberately destroyed documents or took any action to undermine the integrity of these proceedings.

Accordingly, the Court rejects Defendants' unclean hands defense.

CONCLUSION

For the foregoing reasons, the Court rejects Defendants' laches and unclean hands defenses.

SIGNED this 3rd day of September, 2013.

ROY S. PAYNE
UNITED STATES MAGISTRATE JUDGE