Exhibit C-1

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(54) **GENERAL PURPOSE, MULTIPLE PRECISION PARALLEL OPERATION, PROGRAMMABLE MEDIA PROCESSOR**

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(58) **Field of Classification Search** ..... None
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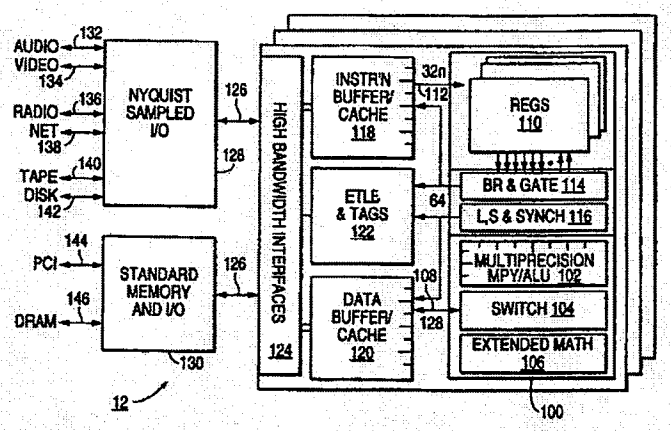
(57) **ABSTRACT**

A general purpose, programmable media processor for processing and transmitting a media data stream of audio, video, radio, graphics, encryption, authentication, and networking information in real-time. The media processor incorporates an execution unit that maintains substantially peak data throughout of media data streams. The execution unit includes a dynamically partionable multi-precision arithmetic unit, programmable switch and programmable extended mathematical element. A high bandwidth external interface supplies media data streams at substantially peak rates to a general purpose register file and the multi-precision execution unit. A memory management unit, and instruction and data cache/buffers are also provided. High bandwidth memory controllers are linked in series to provide a memory channel to the general purpose, programmable media processor. The general purpose, programmable media processor is disposed in a network fabric consisting of fiber optic cable, coaxial cable and twisted pair wires to transmit, process and receive single or unified media data streams. Parallel general purpose media processors are disposed throughout the network in a distributed virtual manner to allow for multi-processor operations and sharing of resources through the network. A method for receiving, processing and transmitting media data streams over the communications fabric is also provided.



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Claim Chart for the HP 7100 LC Chip Set Article.
Joint Claim Construction and Prehearing Statement that includes MicroUnity's Proposed Claim Construction ("Joint Claim Construction") submitted in *MicroUnity Systems Engineering, Inc.* v. *Dell, Inc., et al.* No. 2:04–CV–120(TJW) (E.D. Tex 2004)(the "Lawsuit").
Selected portions of MicroUnity's Preliminary Infringement Contentions submitted in the Lawsuit ("MicroUnity's Preliminary Infringement Contentions").
MicroUnity System Engineering, Inc.'s Opening Brief Regarding Claim Construction submitted Apr. 11, 2005 in the Lawsuit ("MicroUnity's Claim Construction Brief").
MicroUnity System Engineering, Inc.'s Reply Brief Regarding Claim Construction submitted May 25, 2005 in the Lawsuit ("MicroUnity's Claim Construction Reply Brief").
Deposition of Richard A. Belgard, technical expert for MicroUnity in the Lawsuit.
IEEE Draft Standard for "Scalable Coherent Interface–Low–Voltage Differential Signal Specifications and Packet Endoding", IEEE Standards Department, P1596.3/D0.15 (Mar. 1992).
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* cited by examiner

EX PARTE REEXAMINATION CERTIFICATE ISSUED UNDER 35 U.S.C. 307

THE PATENT IS HEREBY AMENDED AS INDICATED BELOW.

Matter enclosed in heavy brackets [ ] appeared in the patent, but has been deleted and is no longer a part of the patent; matter printed in italics indicates additions made to the patent.

AS A RESULT OF REEXAMINATION, IT HAS BEEN DETERMINED THAT:

The patentability of claim **11** is confirmed.

Claims **7**, and **10** are cancelled.

Claim **1** is determined to be patentable as amended.

Claims **2–6**, **8**, and **9**, dependent on an amended claim, are determined to be patentable.

1. [An] *A multi-precision* execution unit, *operating within a general purpose programmable media processor and utilizing a single instruction set,* that maintains substantially

peak data throughput *utilizing simultaneous parallel processing* in the unified execution of multiple media data streams, the execution unit having a data path *and an instruction path, with the simultaneous parallel processing using all or nearly all of the entire width of the data path,* comprising:

a multi-precision arithmetic unit coupled to the data path, the multi-precision arithmetic unit capable of dynamic partitioning based on the elemental width of data received from the data path, the elemental width of the data being equal to or narrower than the data path;

a switch coupled to the data path and programmable to manipulate data received from the data path *in the course of executing programmed instructions, including copying, shifting and resizing operations,* the switch providing data streams to the data path; and

an extended mathematical element *that processes higher level mathematical operations other than addition, subtraction, multiplication and division* coupled to the data path and programmable to implement additional mathematical operations at substantially peak data throughput *through simultaneous parallel processing.*

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