

**Exhibit U**  
**Part 1**



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(54) **METHOD AND SOFTWARE FOR GROUP FLOATING-POINT ARITHMETIC OPERATIONS**

(75) Inventors: **Craig Hansen**, Los Altos, CA (US);  
**John Moussouris**, Palo Alto, CA (US);  
**Alexia Massalin**, San Jose, CA (US)

(73) Assignee: **Microunity Systems Engineering, Inc.**,  
Santa Clara, CA (US)

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(52) **U.S. Cl.** ..... **712/222; 712/221**

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See application file for complete search history.

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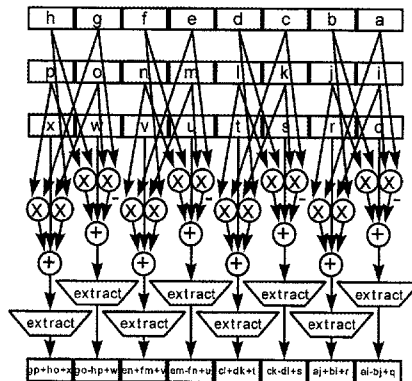
*Primary Examiner*—Eric Coleman

(74) *Attorney, Agent, or Firm*—McDermott Will & Emery LLP

(57) **ABSTRACT**

Methods and software are presented for processing data in a programmable processor, involving (a) decoding instructions for execution using an execution unit operable to execute instructions by partitioning data stored in registers in a register file into multiple data elements, the instructions selected from an instruction set that includes group arithmetic instructions and group data handling instructions, (b) in response to decoding different group data handling instructions, executing group data handling operations that re-arrange data elements in different ways, and (c) in response to decoding different group arithmetic instructions, executing a plurality of different group floating-point and group integer arithmetic operations that each arithmetically operates on the multiple data elements stored in registers in the register file to produce a catenated result that is returned to a register in the register file, wherein the catenated result comprises a plurality of individual results.

**22 Claims, 384 Drawing Sheets**



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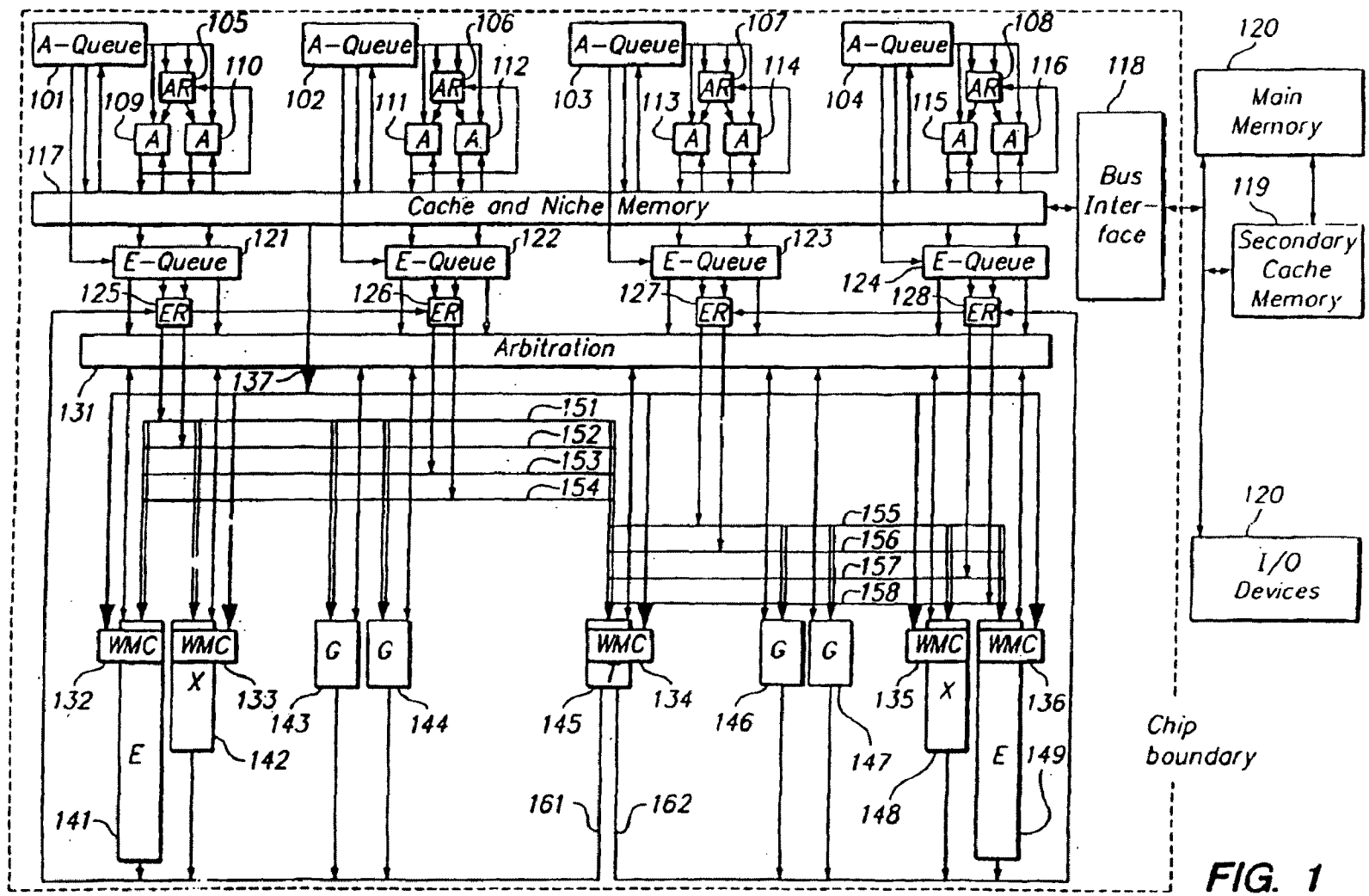


FIG. 1

$$rd_{128} = m[rc]_{(128*64/size)} * rb_{128}$$
$$m[rc]_{(128*64/size)}$$

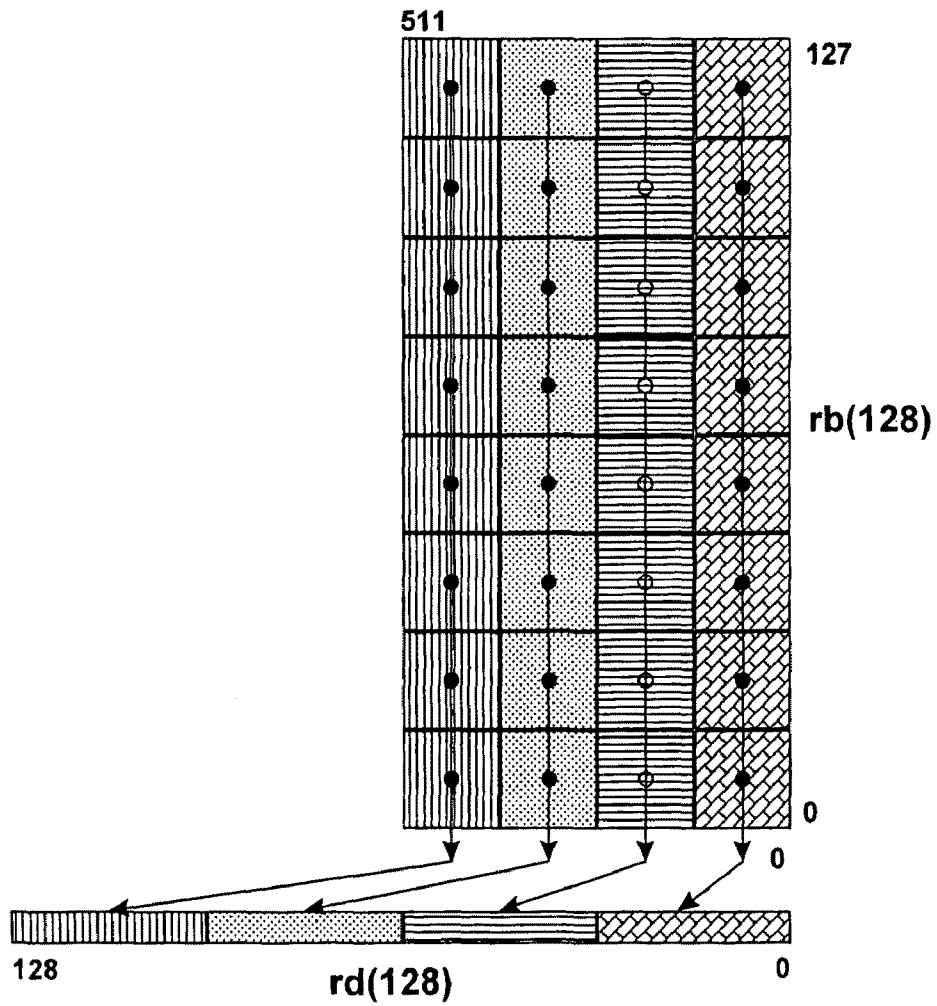


FIG. 2



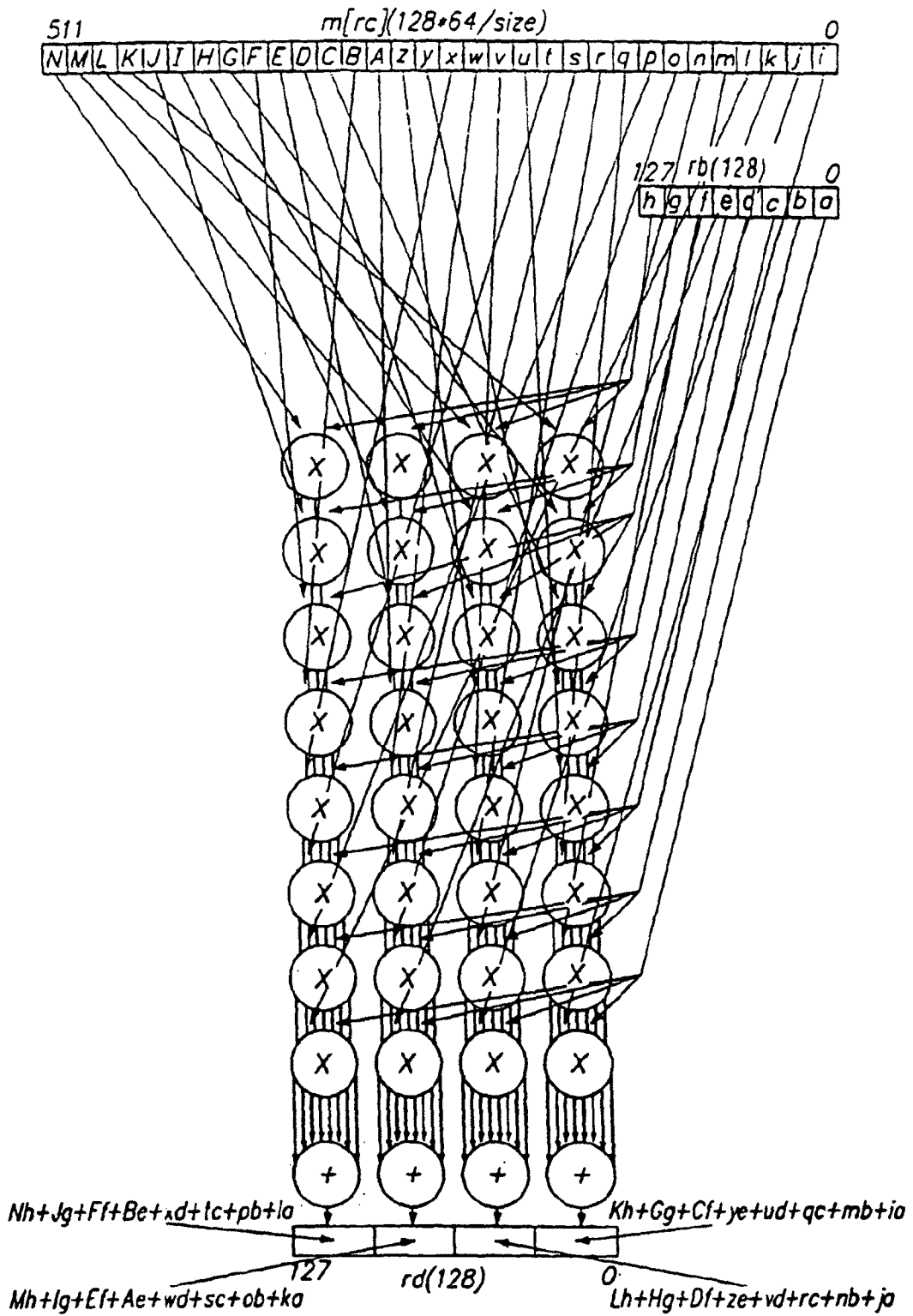


FIG. 3

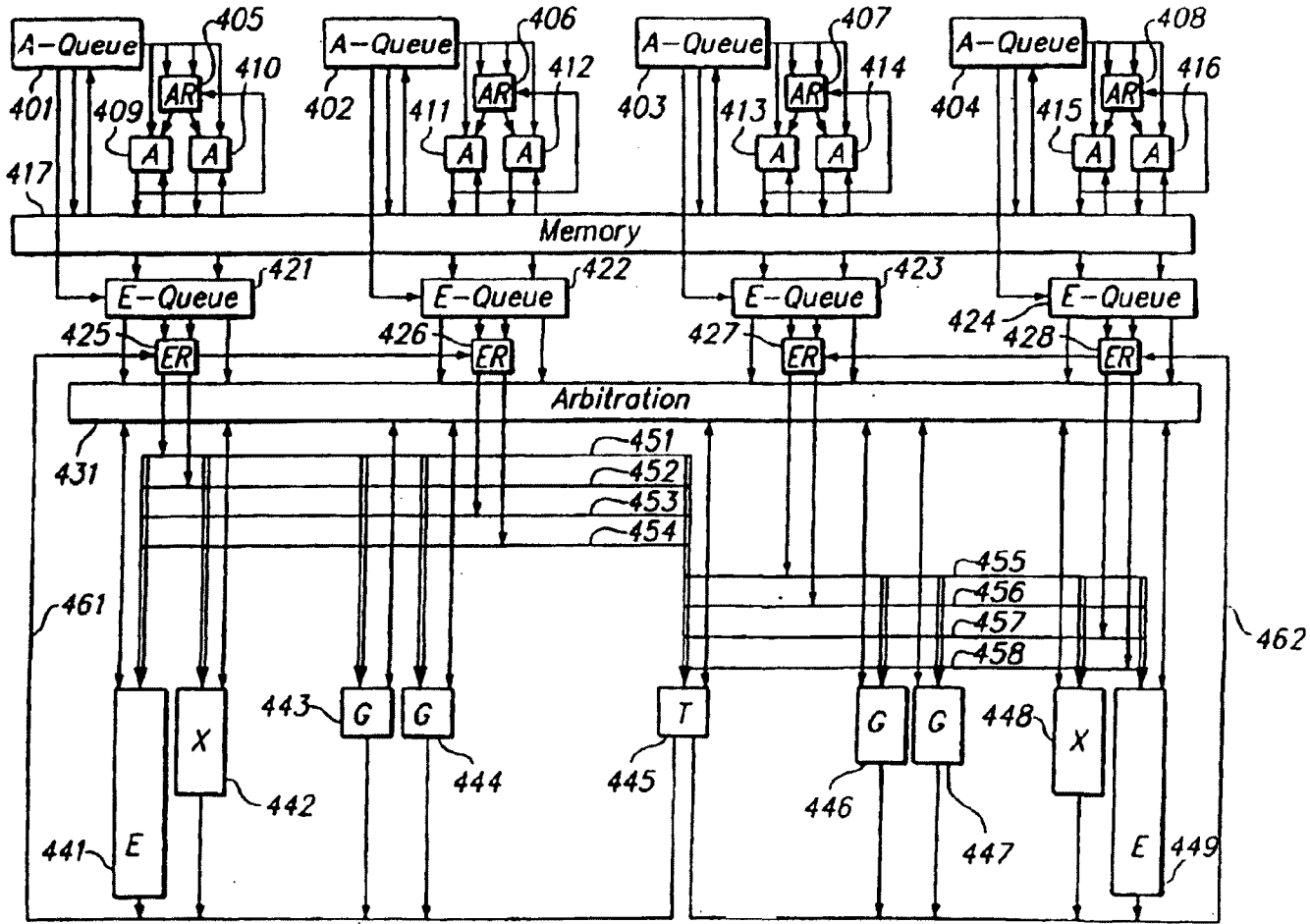
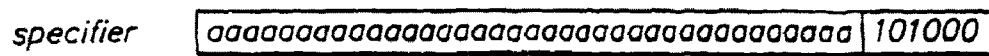
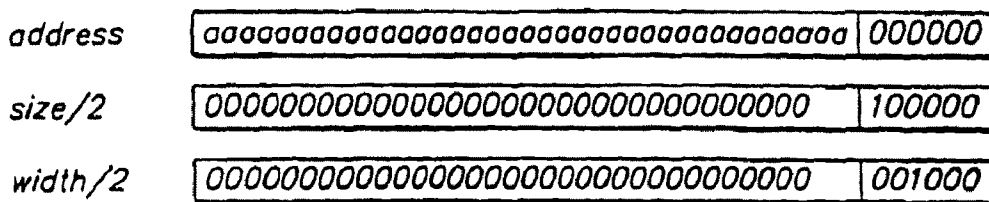
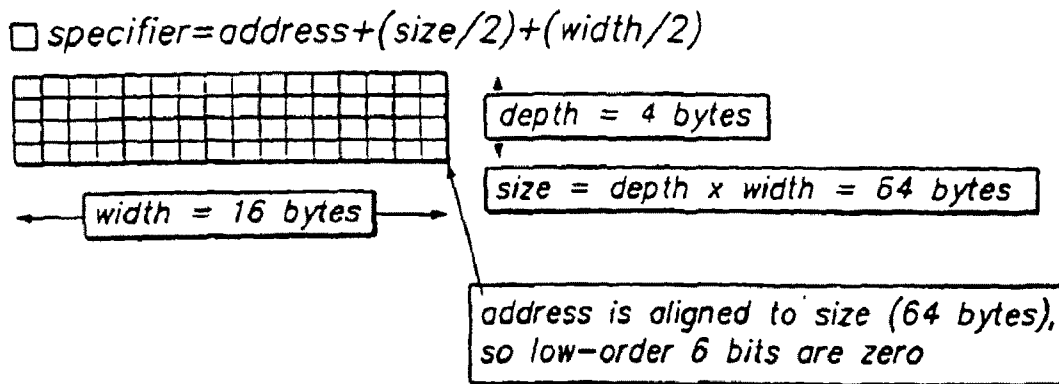
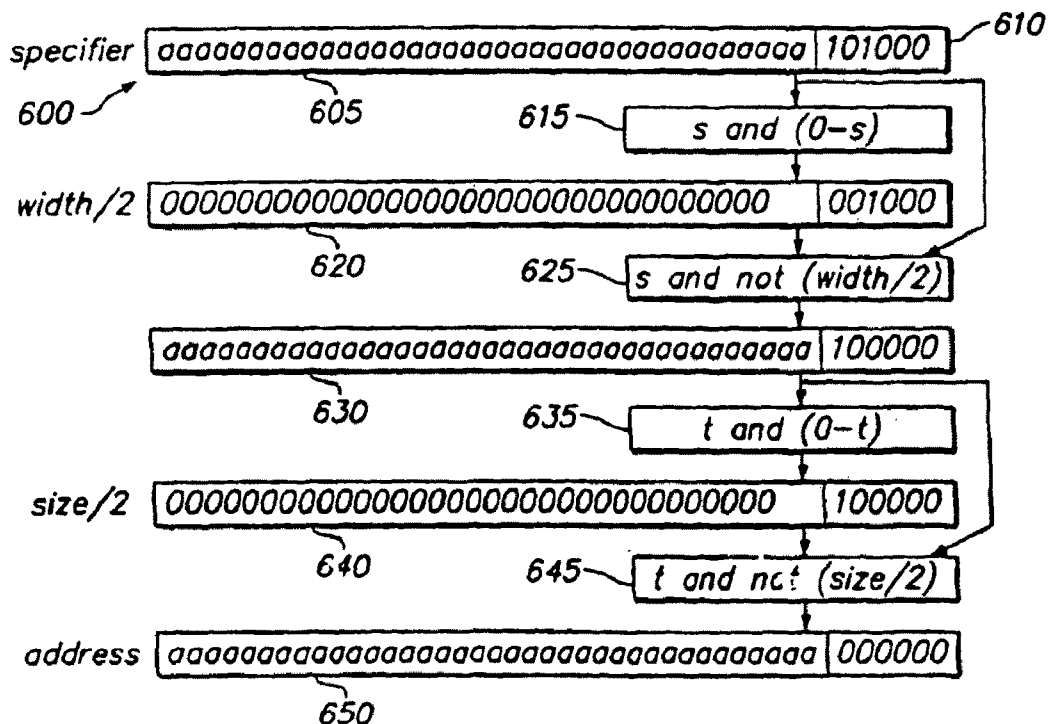


FIG. 4



500 505 510 **FIG. 5**



**FIG. 6**

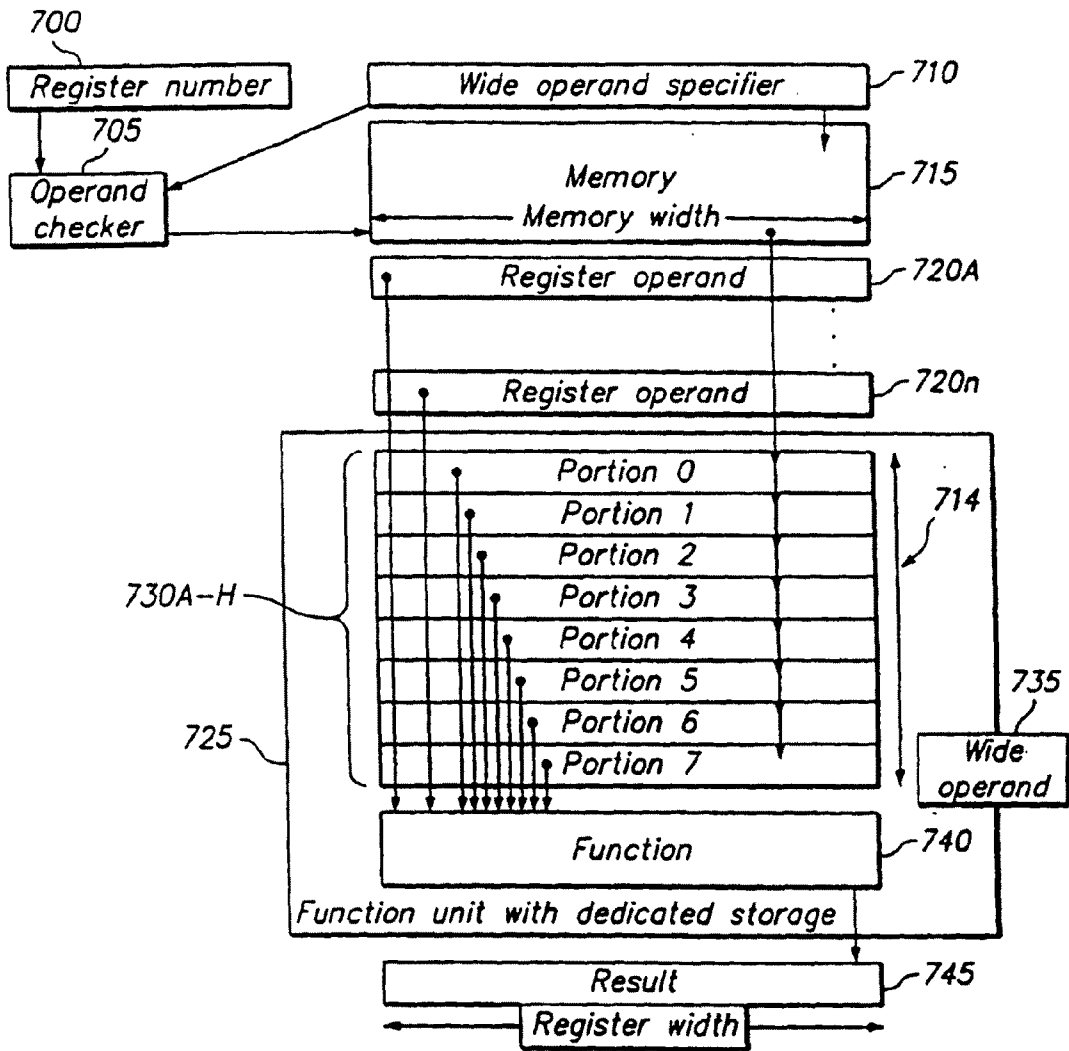


FIG. 7

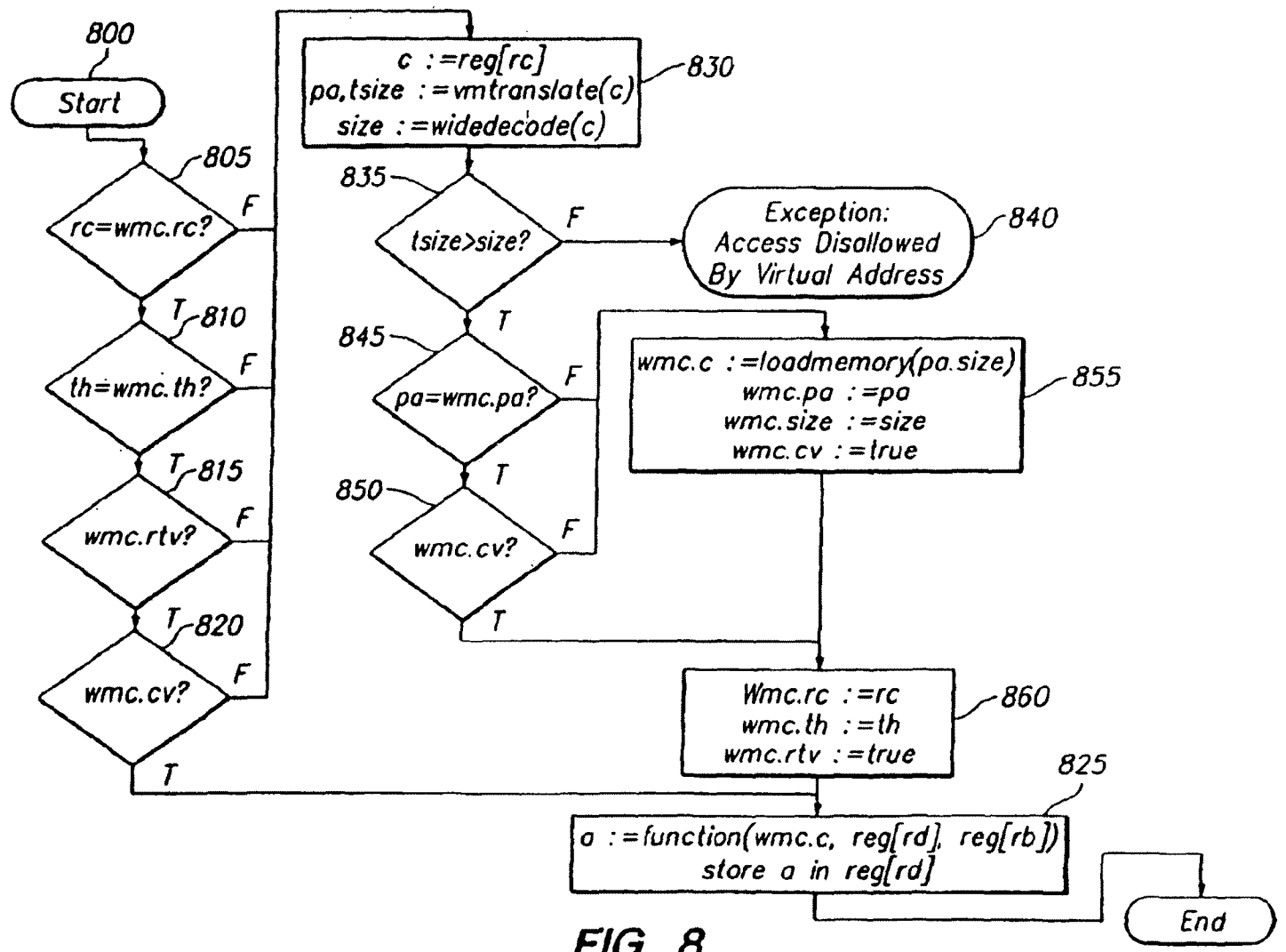
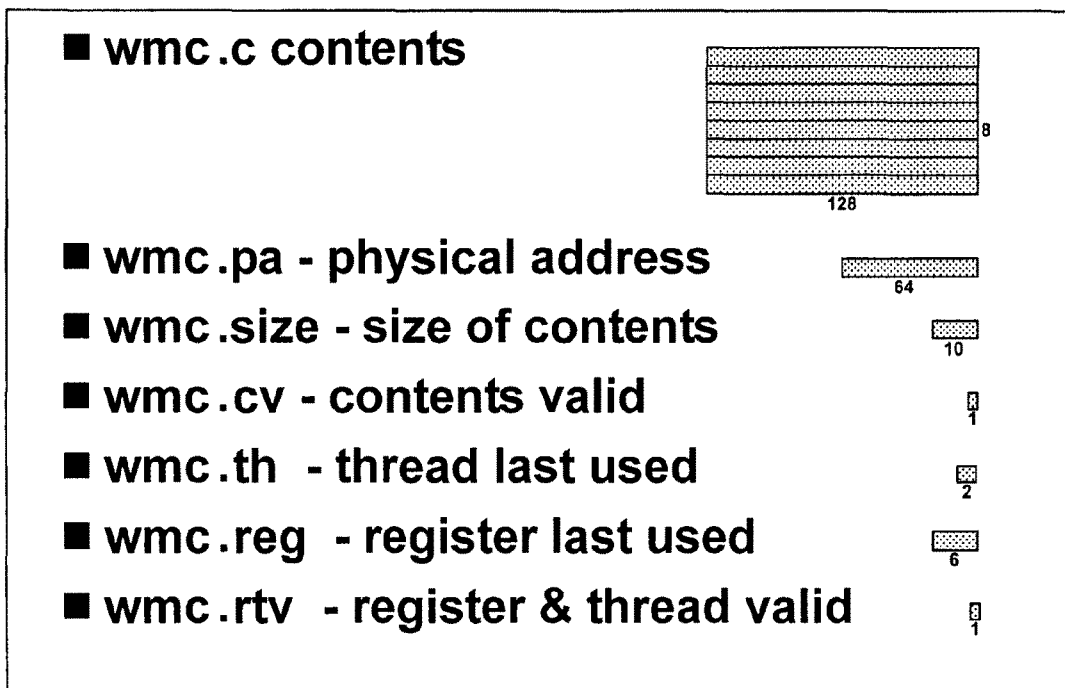


FIG. 8



wide microcache data structures

FIG. 9

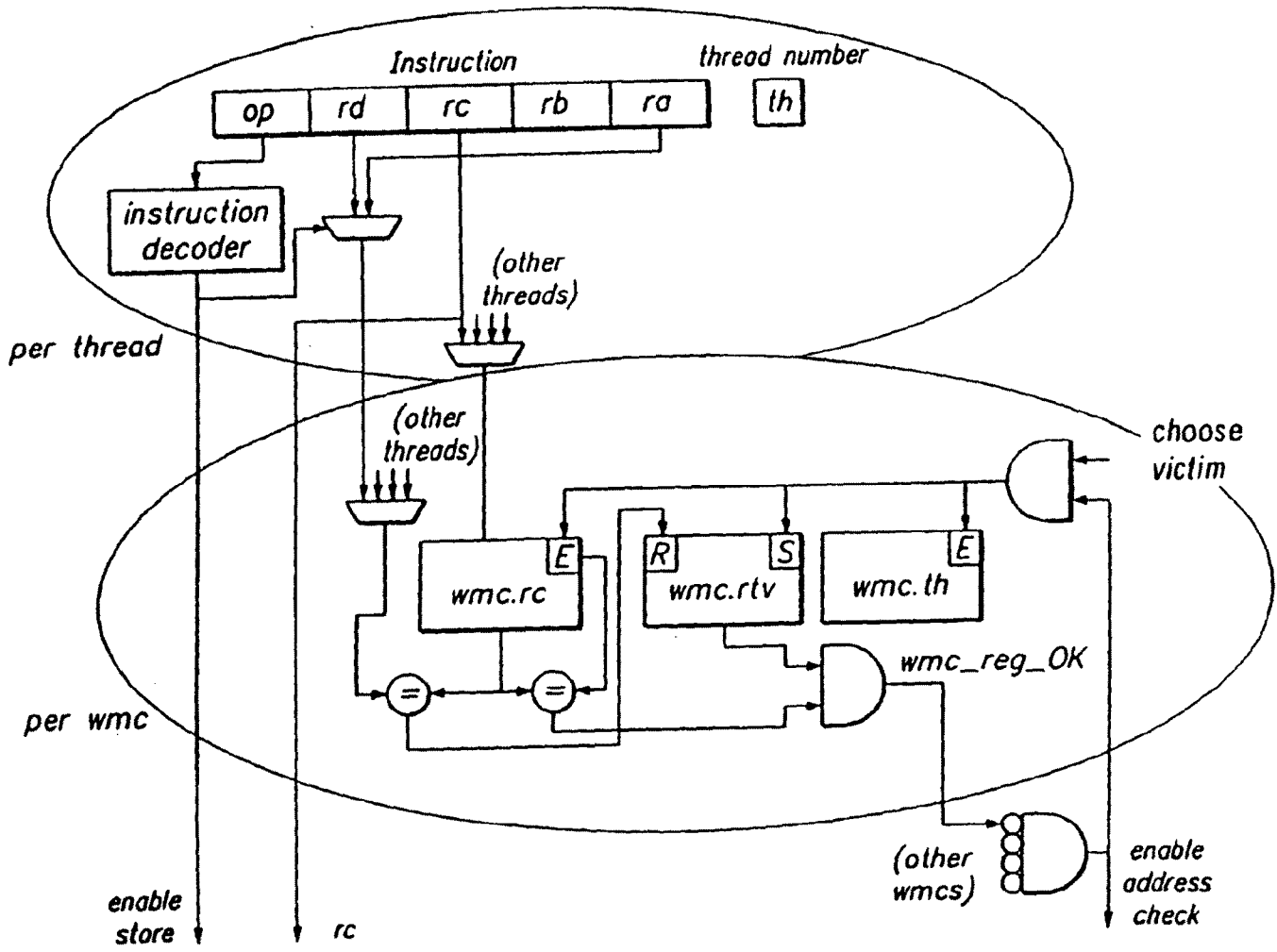
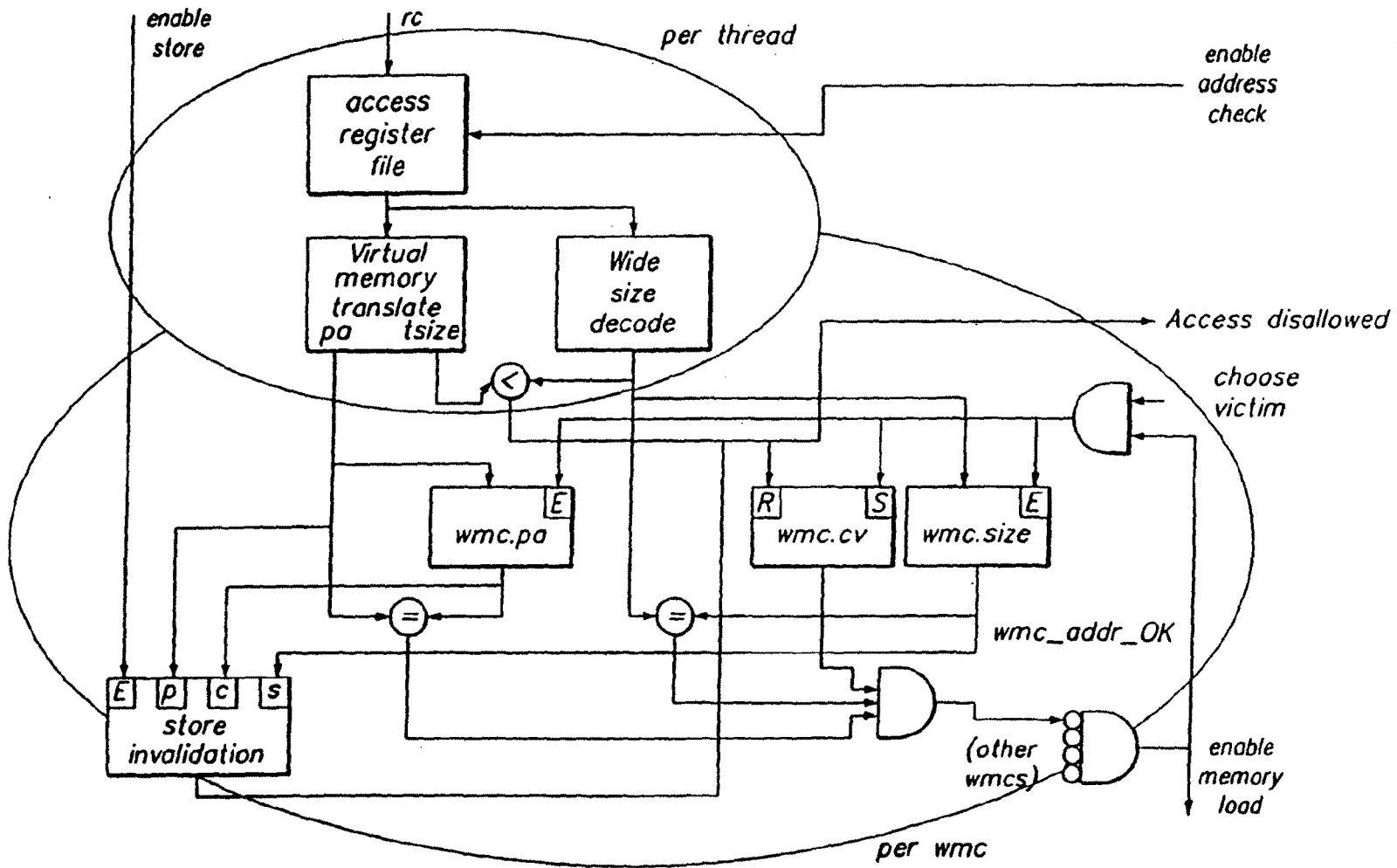


FIG. 10



**FIG. 11**



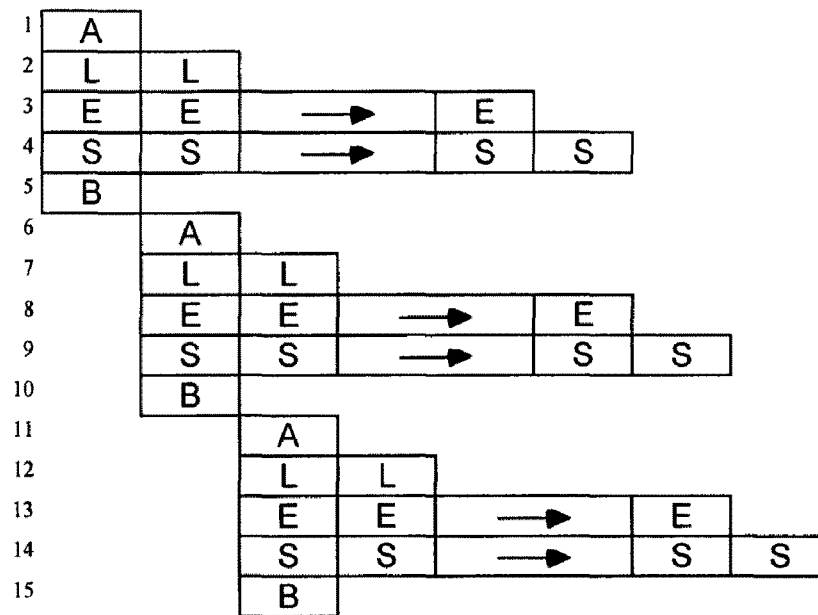


FIG. 12

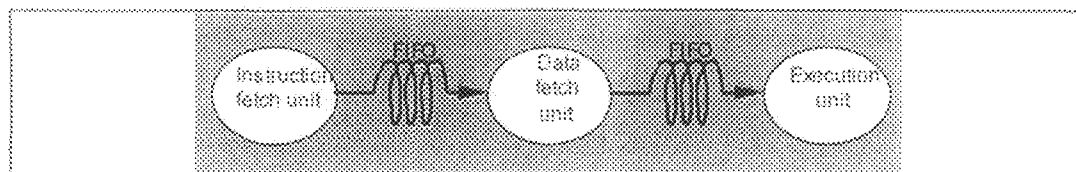


FIG. 13

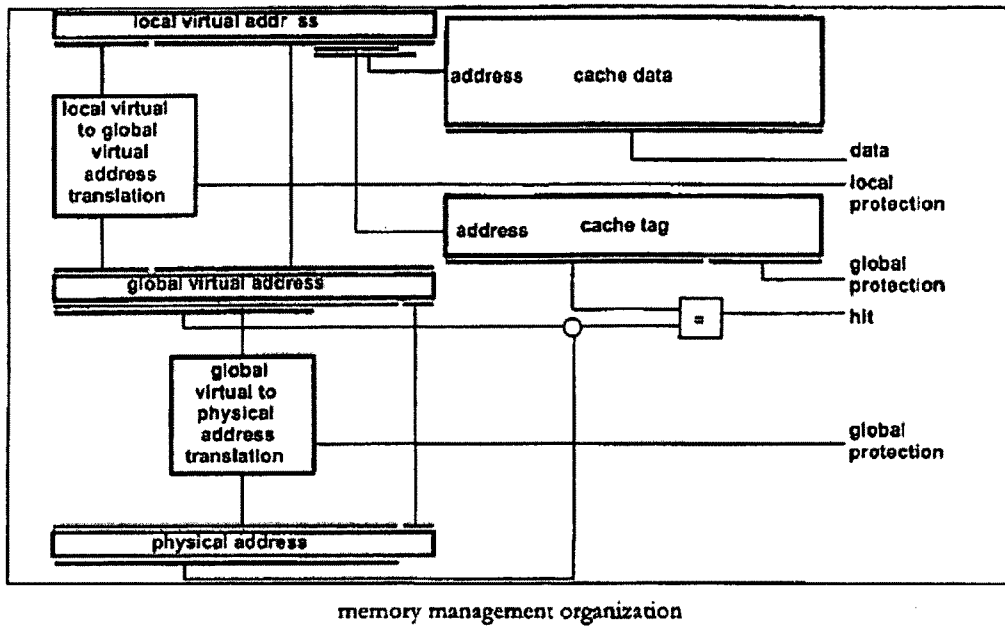


FIG. 14

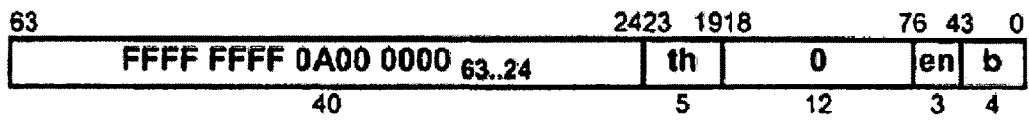


FIG. 15

```
def data,flags ← AccessPhysicalLTB(pa,op,wdata) as
  th ← pa23..19
  en ← pa8..4
  if (en < (1 || 0LE)) and (th < T) and (pa18..8=0) then
    case op of
      R:
        data ← 064 || LTBArry[th][en]
      W:
        LocalTB[th][en] ← wdata63..0
    endcase
  else
    data ← 0
  endif
enddef
```

FIG. 16

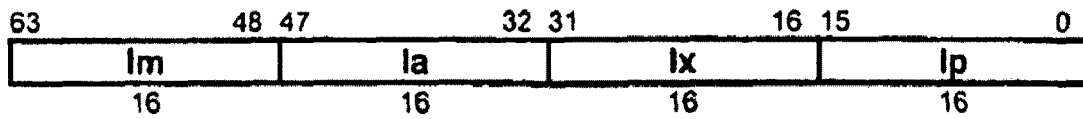


FIG. 17

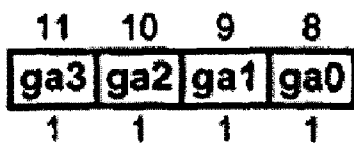


FIG. 18

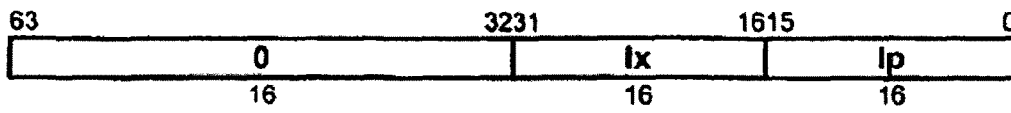


FIG. 19



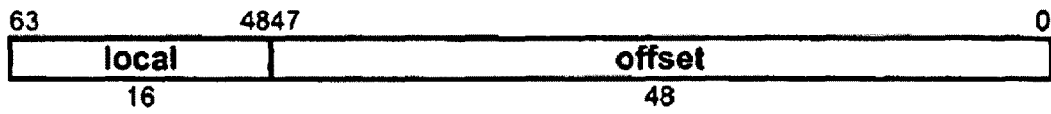


FIG. 20

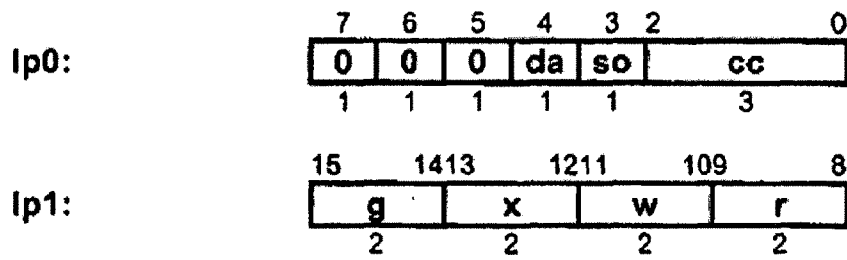


FIG. 21

```
def ga,LocalProtect ← LocalTranslation(th,ba,la,pl) as
  if LB & (ba63..48 ⊕ la63..48) then
    raise AccessDisallowedByVirtualAddress
  endif
  me ← NONE
  for i ← 0 to (1 || 0LE)-1
    if (la63..48 & ~LocalTB[th][i]63..48) = LocalTB[th][i]47..32 then
      me ← i
    endif
  endfor
  if me = NONE then
    if ~ControlRegisterpl+8 then
      raise LocalTBMiss
    endif
    ga ← la
    LocalProtect ← 0
  else
    ga ← (va63..48 ^ LocalTB[th][me]31..16) || va47..0
    LocalProtect ← LocalTB[th][me]15..0
  endif
enddef
```

FIG. 22

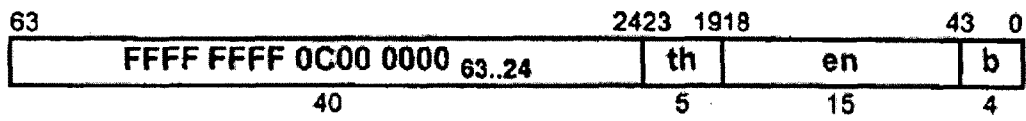


FIG. 23

```
def data, flags ← AccessPhysicalGTB(pa, op, wdata) as
  th ← pa23..19+GT || 0GT
  en ← pa18..4
  if (en < (1 || 0G)) and (th < T) and (pa18+GT..19 = 0) then
    case op of
      R:
        data ← GTBArray[th5..GT][en]
      W:
        GTBArray[th5..GT][en] ← wdata
    endcase
  else
    data ← 0
  endif
enddef
```

FIG. 24

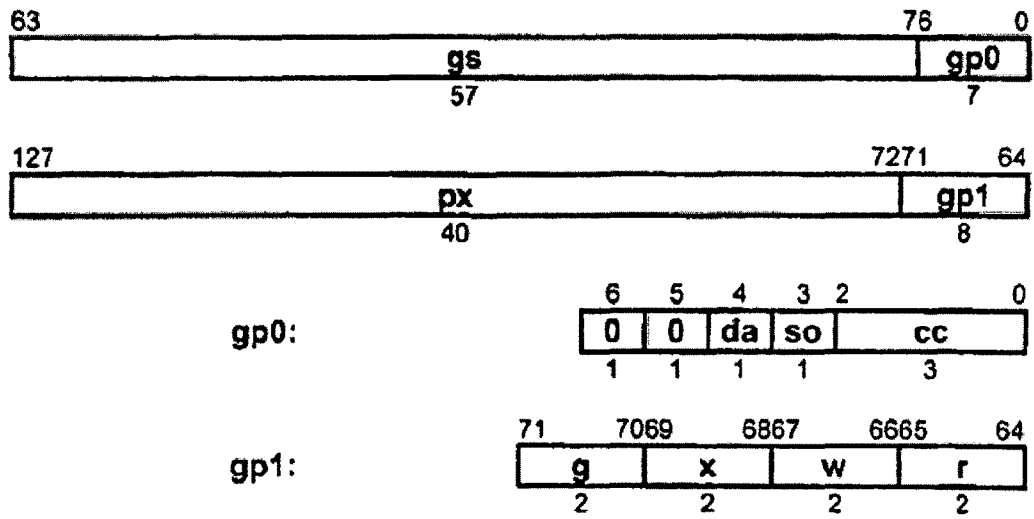


FIG. 25

```

def pa,GlobalProtect ← GlobalAddressTranslation(th,ga,pl,lda) as
  me ← NONE
  for i ← 0 to (1 || 0G) -1
    if GlobalTB[th5..GT][i] ≠ 0 then
      size ← (GlobalTB[th5..GT][i]63..7 and (064-GlobalTB[th5..GT][i]63..7)) || 08
      if ((ga63..8 || 08) ^ (GlobalTB[th5..GT][i]63..8 || 08)) and (064-size) = 0 then
        me ← GlobalTB[th5..GT][i]
      endif
    endif
  endfor
  if me = NONE then
    if lda then
      PerformAccessDetail(AccessDetailRequiredByLocalTB)
    endif
    raise GlobalTBMiss
  else
    pa ← (ga63..8 ^ GlobalTB[th5..GT][me]127..72) || ga7..0
    GlobalProtect ← GlobalTB[th5..GT][me]71..64 || 01 || GlobalTB[th5..GT][me]6..0
  endif
enddef

```

FIG. 26

```
def GTBUpdateWrite(th,fill,data) as
  me ← NONE
  for i ← 0 to (1 || 0G) - 1
    size ← (GlobalTB[th5..GT][i]63..7 and (064-GlobalTB[th5..GT][i]63..7)) || 08
    if ((data63..8 || 08) ^ (GlobalTB[th5..GT][i]63..8 || 08)) and (064-size) = 0 then
      me ← i
    endif
  endfor
  if me = NONE then
    if fill then
      GlobalTB[th5..GT][GTBLast[th5..GT]] ← data
      GTBLast[th5..GT] ← (GTBLast[th5..GT] + 1)G-1..0
      if GTBLast[th5..GT] = 0 then
        GTBLast[th5..GT] ← GTBFirst[th5..GT]
        GTBBump[th5..GT] ← 1
      endif
    endif
  else
    GlobalTB[th5..GT][me] ← data
  endif
enddef
```

FIG. 27



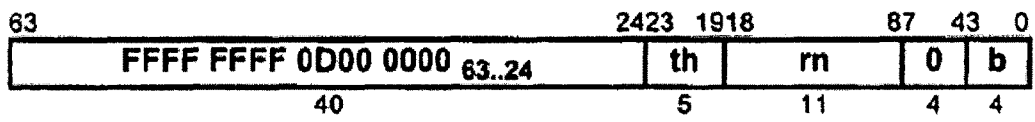


FIG. 28

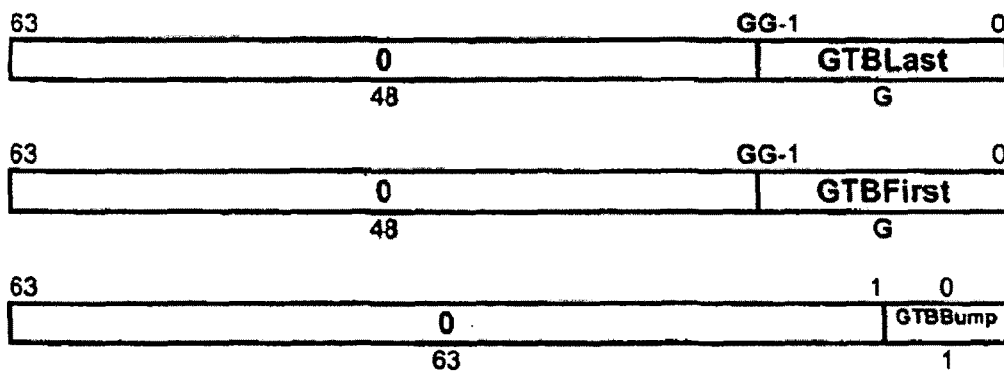


FIG. 29

```

def data,flags ← AccessPhysicalGTBRegisters(pa,op,wdata) as
  th ← pa23..19+GT || 0GT
  rn ← pa18..8
  if (rn < 5) and (th < T) and (pa18+GT..19 = 0) and (pa7..4 =
    case rn || op of
      0 || R, 1 || R:
        data ← 0
      0 || W, 1 || W:
        GTBUpdateWrite(th,rn0,wdata)
      2 || R:
        data ← 064-G || GTBLast[th5..GT]
      2 || W:
        GTBLast[th5..GT] ← wdataG-1..0
      3 || R:
        data ← 064-G || GTBFirst[th5..GT]
      3 || W:
        GTBFirst[th5..GT] ← wdataG-1..0
      3 || R:
        data ← 063 || GTBBump[th5..GT]
      3 || W:
        GTBBump[th5..GT] ← wdata0
    endcase
  else
    data ← 0
  endif
enddef

```

FIG. 30

G.BOOLEAN	Group Boolean
-----------	---------------

## Equivalencies

G.AAA	Group three-way and
G.AAA.1	Group add add add bits
G.AAS.1	Group add add subtract bits
G.ADD.1	Group add bits
G.AND	Group and
G.ANDN	Group and not
G.COPY	Group copy
G.NAAA	Group three-way nand
G.NAND	Group nand
G.NOOO	Group three-way nor
G.NOR	Group nor
G.NOT	Group not
G.NXXX	Group three-way exclusive-nor
G.OOO	Group three-way or
G.OR	Group or
G.ORN	Group or not
G.SAA.1	Group subtract add add bits
G.SAS.1	Group subtract add subtract bits
G.SET	Group set
G.SET.AND.E.1	Group set and equal zero bits
G.SET.AND.NE.1	Group set and not equal zero bits
G.SET.E.1	Group set equal bits
G.SET.G.1	Group set greater signed bits
G.SET.G.U.1	Group set greater unsigned bits
G.SET.G.Z.1	Group set greater zero signed bits
G.SET.GE.1	Group set greater equal signed bits
G.SET.GE.Z.1	Group set greater equal zero signed bits
G.SET.L.1	Group set less signed bits
G.SET.L.Z.1	Group set less zero signed bits
G.SET.LE.1	Group set less equal signed bits
G.SET.LE.U.1	Group set less equal unsigned bits
G.SET.LE.Z.1	Group set less equal zero signed bits
G.SET.NE.1	Group set not equal bits
G.SET.GE.U.1	Group set greater equal unsigned bits
G.SET.L.U.1	Group set less unsigned bits

FIG. 31A

G.SSA.1	Group subtract subtract add bits
G.SSS.1	Group subtract subtract subtract bits
G.SUB.1	Group subtract bits
G.XNOR	Group exclusive-nor
G.XOR	Group exclusive-or
G.XXX	Group three-way exclusive-or
G.ZERO	Group zero

G.AAA rd@rc,rb	←	G.BOOLEAN rd@rc,rb,0b10000000
G.AAA.1 rd@rc,rb	→	G.XXX rd@rc,rb
G.AAS.1 rd@rc,rb	→	G.XXX rd@rc,rb
G.ADD.1 rd=rc,rb	→	G.XOR rd=rc,rb
G.AND rd=rc,rb	←	G.BOOLEAN rd@rc,rb,0b10001000
G.ANDN rd=rc,rb	←	G.BOOLEAN rd@rc,rb,0b01000100
G.BOOLEAN rd@rb,rc,i	→	G.BOOLEAN rd@rc,rb,i7i5i6i4i3i1i2i0
G.COPY rd=rc	←	G.BOOLEAN rd@rc,rc,0b10001000
G.NAAA. rd@rc,rb	←	G.BOOLEAN rd@rc,rb,0b01111111
G.NAND rd=rc,rb	←	G.BOOLEAN rd@rc,rb,0b01110111
G.NOOO rd@rc,rb	←	G.BOOLEAN rd@rc,rb,0b00000001
G.NOR rd=rc,rb	←	G.BOOLEAN rd@rc,rb,0b00010001
G.NOT rd=rc	←	G.BOOLEAN rd@rc,rc,0b00010001
G.NXXX rd@rc,rb	←	G.BOOLEAN rd@rc,rb,0b01101001
G.OOO rd@rc,rb	←	G.BOOLEAN rd@rc,rb,0b11111110
G.OR rd=rc,rb	←	G.BOOLEAN rd@rc,rb,0b11101110
G.ORN rd=rc,rb	←	G.BOOLEAN rd@rc,rb,0b11011101
G.SAA.1 rd@rc,rb	→	G.XXX rd@rc,rb
G.SAS.1 rd@rc,rb	→	G.XXX rd@rc,rb
G.SET rd	←	G.BOOLEAN rd@rd,rd,0b10000001
G.SET.AND.E.1 rd=rb,rc	→	G.NAND rd=rc,rb
G.SET.AND.NE.1 rd=rb,rc	→	G.AND rd=rc,rb
G.SET.E.1 rd=rb,rc	→	G.XNOR rd=rc,rb
G.SET.G.1 rd=rb,rc	→	G.ANDN rd=rc,rb
G.SET.G.U.1 rd=rb,rc	→	G.ANDN rd=rb,rc
G.SET.G.Z.1 rd=rc	→	G.ZERO rd
G.SET.GE.1 rd=rb,rc	→	G.ORN rd=rc,rb
G.SET.GE.Z.1 rd=rc	→	G.NOT rd=rc

FIG. 31A continued

G.SET.L.1 rd=rb,rc	→	G.ANDN rd=rb,rc
G.SET.L.Z.1 rd=rc	→	G.COPY rd=rc
G.SET.LE.1 rd=rb,rc	→	G.ORN rd=rb,rc
G.SET.LE.U.1 rd=rb,rc	→	G.ORN rd=rc,rb
G.SET.LE.Z.1 rd=rc	→	G.SET rd
G.SET.NE.1 rd=rb,rc	→	G.XOR rd=rc,rb
G.SET.GE.U.1 rd=rb,rc	→	G.ORN rd=rb,rc
G.SET.L.U.1 rd=rb,rc	→	G.ANDN rd=rc,rb
G.SSA.1 rd@rc,rb	→	G.XXX rd@rc,rb
G.SSS.1 rd@rc,rb	→	G.XXX rd@rc,rb
G.SUB.1 rd=rc,rb	→	G.XOR rd=rc,rb
G.XNOR rd=rc,rb	←	G.BOOLEAN rd@rc,rb,0b10011001
G.XOR rd=rc,rb	←	G.BOOLEAN rd@rc,rb,0b01100110
G.XXX rd@rc,rb	←	G.BOOLEAN rd@rc,rb,0b10010110
G.ZERO rd	←	G.BOOLEAN rd@rd,rd,0b00000000

Selection

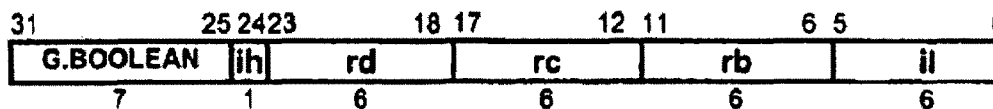
operation	function (binary)	function (decimal)
d	11110000	240
c	11001100	204
b	10101010	176
d&c&b	10000000	128
(d&c) b	11101010	234
d c b	11111110	254
d?c:b	11001010	202
d^c^b	10010110	150
~d^c^b	01101001	105
0	00000000	0

FIG. 31A continued

**Format**

G.BOOLEANrd@trc,trb,f

rd=gbooleani(rd,rc,rb,f)



```

if f6=f5 then
  if f2=f1 then
    if f2 then
      rc ← max(trc,trb)
      rb ← min(trc,trb)
    else
      rc ← min(trc,trb)
      rb ← max(trc,trb)
    endif
    ih ← 0
    il ← 0 || f6 || f7 || f4 || f3 || f0
  else
    if f2 then
      rc ← trb
      rb ← trc
    else
      rc ← trc
      rb ← trb
    endif
    ih ← 0
    il ← 1 || f6 || f7 || f4 || f3 || f0
  endif
else
  ih ← 1
  if f6 then
    rc ← trb
    rb ← trc
    il ← f1 || f2 || f7 || f4 || f3 || f0
  else
    rc ← trc
    rb ← trb
    il ← f2 || f1 || f7 || f4 || f3 || f0
  endif
endif
endif
    
```

FIG. 31B

## Definition

```
def GroupBoolean (ih,rd,rc,rb,il)
  d ← RegRead(rd, 128)
  c ← RegRead(rc, 128)
  b ← RegRead(rb, 128)
  if ih=0 then
    if il5=0 then
      f ← il3 || il4 || il4 || il2 || il1 || (rc>rb)2 || il0
    else
      f ← il3 || il4 || il4 || il2 || il1 || 0 || 1 || il0
    endif
  else
    f ← il3 || 0 || 1 || il2 || il1 || il5 || il4 || il0
  endif
  for i ← 0 to 127 by size
    ai ← f(dj||ci||bi)
  endfor
  RegWrite(rd, 128, a)
enddef
```

## Exceptions

none

FIG.31C



Operation codes

G.MUX	Group multiplex
-------	-----------------

Redundancies

G.MUX ra=rd,rc,rc	⇔	G.COPY ra=rc
G.MUX ra=ra,rc,rb	⇔	G.BOOLEAN ra@rc,rb,0x11001010
G.MUX ra=rd,ra,rb	⇔	G.BOOLEAN ra@rd,rb,0x11100010
G.MUX ra=rd,rc,ra	⇔	G.BOOLEAN ra@rd,rc,0x11011000
G.MUX ra=rd,rd,rb	⇔	G.OR ra=rd,rb
G.MUX ra=rd,rc,rd	⇔	G.AND ra=rd,rc

Format

G.MUX ra=rd,rc,rb

ra=gmux(rd,rc,rb)

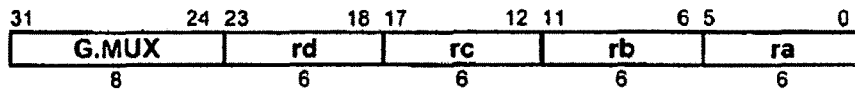


FIG. 31D

## Definition

```
def GroupTernary(op,size,rd,rc,rb,ra) as
  d ← RegRead(rd, 128)
  c ← RegRead(rc, 128)
  b ← RegRead(rb, 128)
  case op of
    G.MUX:
      a ← (c and d) or (b and not d)
  endcase
  RegWrite(ra, 128, a)
enddef
```

## Exceptions

none

FIG. 31E

Operation codes

G.ADD. 8	Group add bytes
G.ADD. 16	Group add doublets
G.ADD. 32	Group add quadlets
G.ADD. 64	Group add octlets
G.ADD.128	Group add hexlet
G.ADD.L. 8	Group add limit signed bytes
G.ADD.L. 16	Group add limit signed doublets
G.ADD.L. 32	Group add limit signed quadlets
G.ADD.L. 64	Group add limit signed octlets
G.ADD.L.128	Group add limit signed hexlet
G.ADD.L.U. 8	Group add limit unsigned bytes
G.ADD.L.U. 16	Group add limit unsigned doublets
G.ADD.L.U. 32	Group add limit unsigned quadlets
G.ADD.L.U. 64	Group add limit unsigned octlets
G.ADD.L.U.128	Group add limit unsigned hexlet
G.ADD. 8.O	Group add signed bytes check overflow
G.ADD. 16.O	Group add signed doublets check overflow
G.ADD. 32.O	Group add signed quadlets check overflow
G.ADD. 64.O	Group add signed octlets check overflow
G.ADD.128.O	Group add signed hexlet check overflow
G.ADD.U. 8.O	Group add unsigned bytes check overflow
G.ADD.U. 16.O	Group add unsigned doublets check overflow
G.ADD.U. 32.O	Group add unsigned quadlets check overflow
G.ADD.U. 64.O	Group add unsigned octlets check overflow
G.ADD.U.128.O	Group add unsigned hexlet check overflow

Redundancies

G.ADD.size rd=rc,rc	↔	G.SHL.I.size rd=rc,1
G.ADD.size.O rd=rc,rc	↔	G.SHL.I.size.O rd=rc,1
G.ADD.U.size.O rd=rc,rc	↔	G.SHL.I.U.size.O rd=rc,1

FIG. 32A

**Format**

**G.op.size rd=rc,rb**

**rd=gopsize(rc,rb)**

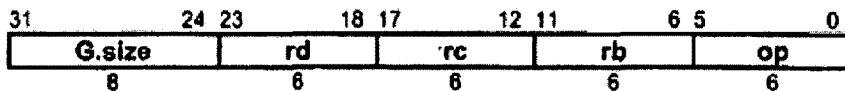


FIG 32B

**Definition**

```

def Group(op,size,rd,rc,rb)
  c ← RegRead(rc, 128)
  b ← RegRead(rb, 128)
  case op of
    G.ADD:
      for i ← 0 to 128-size by size
        ai+size-1..i ← ci+size-1..i + bi+size-1..i
      endfor
    G.ADD.L:
      for i ← 0 to 128-size by size
        t ← (ci+size-1 || ci+size-1..i) + (bi+size-1 || bi+size-1..i)
        ai+size-1..i ← (tsize ≠ tsize-1) ? (tsize || tsize-1size-1) : tsize-1..0
      endfor
    G.ADD.L.U:
      for i ← 0 to 128-size by size
        t ← (01 || ci+size-1..i) + (01 || bi+size-1..i)
        ai+size-1..i ← (tsize ≠ 0) ? (1size) : tsize-1..0
      endfor
    G.ADD.O:
      for i ← 0 to 128-size by size
        t ← (ci+size-1 || ci+size-1..i) + (bi+size-1 || bi+size-1..i)
        if tsize ≠ tsize-1 then
          raise FixedPointArithmetic
        endif
        ai+size-1..i ← tsize-1..0
      endfor
    G.ADD.U.O:
      for i ← 0 to 128-size by size
        t ← (01 || ci+size-1..i) + (01 || bi+size-1..i)
        if tsize ≠ 0 then
          raise FixedPointArithmetic
        endif
        ai+size-1..i ← tsize-1..0
      endfor
  endcase
  RegWrite(rd, 128, a)
enddef

```

**Exceptions**

Fixed-point arithmetic

FIG. 32C

## Operation codes

G.SET.AND.E.8	Group set and equal zero bytes
G.SET.AND.E.16	Group set and equal zero doublets
G.SET.AND.E.32	Group set and equal zero quadlets
G.SET.AND.E.64	Group set and equal zero octlets
G.SET.AND.E.128	Group set and equal zero hexlet
G.SET.AND.NE.8	Group set and not equal zero bytes
G.SET.AND.NE.16	Group set and not equal zero doublets
G.SET.AND.NE.32	Group set and not equal zero quadlets
G.SET.AND.NE.64	Group set and not equal zero octlets
G.SET.AND.NE.128	Group set and not equal zero hexlet
G.SET.E.8	Group set equal bytes
G.SET.E.16	Group set equal doublets
G.SET.E.32	Group set equal quadlets
G.SET.E.64	Group set equal octlets
G.SET.E.128	Group set equal hexlet
G.SET.GE.8	Group set greater equal signed bytes
G.SET.GE.16	Group set greater equal signed doublets
G.SET.GE.32	Group set greater equal signed quadlets
G.SET.GE.64	Group set greater equal signed octlets
G.SET.GE.128	Group set greater equal signed hexlet
G.SET.GE.U.8	Group set greater equal unsigned bytes
G.SET.GE.U.16	Group set greater equal unsigned doublets
G.SET.GE.U.32	Group set greater equal unsigned quadlets
G.SET.GE.U.64	Group set greater equal unsigned octlets
G.SET.GE.U.128	Group set greater equal unsigned hexlet
G.SET.L.8	Group set signed less bytes
G.SET.L.16	Group set signed less doublets
G.SET.L.32	Group set signed less quadlets
G.SET.L.64	Group set signed less octlets
G.SET.L.128	Group set signed less hexlet
G.SET.L.U.8	Group set less unsigned bytes
G.SET.L.U.16	Group set less unsigned doublets
G.SET.L.U.32	Group set less unsigned quadlets
G.SET.L.U.64	Group set less unsigned octlets
G.SET.L.U.128	Group set less unsigned hexlet
G.SET.NE.8	Group set not equal bytes
G.SET.NE.16	Group set not equal doublets

FIG 33A

G.SET.NE.32	Group set not equal quadlets
G.SET.NE.64	Group set not equal octlets
G.SET.NE.128	Group set not equal hexlet
G.SUB.8	Group subtract bytes
G.SUB.8.O	Group subtract signed bytes check overflow
G.SUB.16	Group subtract doublets
G.SUB.16.O	Group subtract signed doublets check overflow
G.SUB.32	Group subtract quadlets
G.SUB.32.O	Group subtract signed quadlets check overflow
G.SUB.64	Group subtract octlets
G.SUB.64.O	Group subtract signed octlets check overflow
G.SUB.128	Group subtract hexlet
G.SUB.128.O	Group subtract signed hexlet check overflow
G.SUB.L.8	Group subtract limit signed bytes
G.SUB.L.16	Group subtract limit signed doublets
G.SUB.L.32	Group subtract limit signed quadlets
G.SUB.L.64	Group subtract limit signed octlets
G.SUB.L.128	Group subtract limit signed hexlet
G.SUB.L.U.8	Group subtract limit unsigned bytes
G.SUB.L.U.16	Group subtract limit unsigned doublets
G.SUB.L.U.32	Group subtract limit unsigned quadlets
G.SUB.L.U.64	Group subtract limit unsigned octlets
G.SUB.L.U.128	Group subtract limit unsigned hexlet
G.SUB.U.8.O	Group subtract unsigned bytes check overflow
G.SUB.U.16.O	Group subtract unsigned doublets check overflow
G.SUB.U.32.O	Group subtract unsigned quadlets check overflow
G.SUB.U.64.O	Group subtract unsigned octlets check overflow
G.SUB.U.128.O	Group subtract unsigned hexlet check overflow

FIG 33A *continued*

## Equivalencies

G.SET.E.Z.8	Group set equal zero bytes
G.SET.E.Z.16	Group set equal zero doublets
G.SET.E.Z.32	Group set equal zero quadlets
G.SET.E.Z.64	Group set equal zero octlets
G.SET.E.Z.128	Group set equal zero hexlet
G.SET.G.Z.8	Group set greater zero signed bytes
G.SET.G.Z.16	Group set greater zero signed doublets
G.SET.G.Z.32	Group set greater zero signed quadlets
G.SET.G.Z.64	Group set greater zero signed octlets
G.SET.G.Z.128	Group set greater zero signed hexlet
G.SET.GE.Z.8	Group set greater equal zero signed bytes
G.SET.GE.Z.16	Group set greater equal zero signed doublets
G.SET.GE.Z.32	Group set greater equal zero signed quadlets
G.SET.GE.Z.64	Group set greater equal zero signed octlets
G.SET.GE.Z.128	Group set greater equal zero signed hexlet
G.SET.L.Z.8	Group set less zero signed bytes
G.SET.L.Z.16	Group set less zero signed doublets
G.SET.L.Z.32	Group set less zero signed quadlets
G.SET.L.Z.64	Group set less zero signed octlets
G.SET.L.Z.128	Group set less zero signed hexlet
G.SET.LE.Z.8	Group set less equal zero signed bytes
G.SET.LE.Z.16	Group set less equal zero signed doublets
G.SET.LE.Z.32	Group set less equal zero signed quadlets
G.SET.LE.Z.64	Group set less equal zero signed octlets
G.SET.LE.Z.128	Group set less equal zero signed hexlet
G.SET.NE.Z.8	Group set not equal zero bytes
G.SET.NE.Z.16	Group set not equal zero doublets
G.SET.NE.Z.32	Group set not equal zero quadlets
G.SET.NE.Z.64	Group set not equal zero octlets
G.SET.NE.Z.128	Group set not equal zero hexlet

FIG. 33A *continued*



<b>G.SET.LE.8</b>	Group set less equal signed bytes
<b>G.SET.LE.16</b>	Group set less equal signed doublets
<b>G.SET.LE.32</b>	Group set less equal signed quadiets
<b>G.SET.LE.64</b>	Group set less equal signed octiets
<b>G.SET.LE.128</b>	Group set less equal signed hexlet
<b>G.SET.LE.U.8</b>	Group set less equal unsigned bytes
<b>G.SET.LE.U.16</b>	Group set less equal unsigned doublets
<b>G.SET.LE.U.32</b>	Group set less equal unsigned quadiets
<b>G.SET.LE.U.64</b>	Group set less equal unsigned octiets
<b>G.SET.LE.U.128</b>	Group set less equal unsigned hexlet
<b>G.SET.G.8</b>	Group set signed greater bytes
<b>G.SET.G.16</b>	Group set signed greater doublets
<b>G.SET.G.32</b>	Group set signed greater quadiets
<b>G.SET.G.64</b>	Group set signed greater octiets
<b>G.SET.G.128</b>	Group set signed greater hexlet
<b>G.SET.G.U.8</b>	Group set greater unsigned bytes
<b>G.SET.G.U.16</b>	Group set greater unsigned doublets
<b>G.SET.G.U.32</b>	Group set greater unsigned quadiets
<b>G.SET.G.U.64</b>	Group set greater unsigned octiets
<b>G.SET.G.U.128</b>	Group set greater unsigned hexlet

<b>G.SET.E.Z.size rd=rc</b>	←	<b>G.SET.AND.E.size rd=rc,rc</b>
<b>G.SET.G.Z.size rd=rc</b>	⇐	<b>G.SET.L.U.size rd=rc,rc</b>
<b>G.SET.GE.Z.size rd=rc</b>	⇐	<b>G.SET.GE.size rd=rc,rc</b>
<b>G.SET.L.Z.size rd=rc</b>	⇐	<b>G.SET.L.size rd=rc,rc</b>
<b>G.SET.LE.Z.size rd=rc</b>	⇐	<b>G.SET.GE.U.size rd=rc,rc</b>
<b>G.SET.NE.Z.size rd=rc</b>	←	<b>G.SET.AND.NE.size rd=rc,rc</b>
<b>G.SET.G.size rd=rb,rc</b>	→	<b>G.SET.L.size rd=rc,rb</b>
<b>G.SET.G.U.size rd=rb,rc</b>	→	<b>G.SET.L.U.size rd=rc,rb</b>
<b>G.SET.LE.size rd=rb,rc</b>	→	<b>G.SET.GE.size rd=rc,rb</b>
<b>G.SET.LE.U.size rd=rb,rc</b>	→	<b>G.SET.GE.U.size rd=rc,rb</b>

FIG. 33A *continued*

**Redundancies**

G.SET.E.size rd=rc,rc	⇔	<i>G.SET rd</i>
G.SET.NE.size rd=rc,rc	⇔	<i>G.ZERO rd</i>
G.SUB.size rd=rc,rc	⇔	<i>G.ZERO rd</i>
G.SUB.L.size rd=rc,rc	⇔	<i>G.ZERO rd</i>
G.SUB.L.U.size rd=rc,rc	⇔	<i>G.ZERO rd</i>
G.SUB.size.O rd=rc,rc	⇔	<i>G.ZERO rd</i>
G.SUB.U.size.O rd=rc,rc	⇔	<i>G.ZERO rd</i>

**Selection**

class	operation	cond	operand	size	check
arithmetic	SUB			8 16 32 64 128	
			NONE U	8 16 32 64 128	O
	SUB.L		NONE U	8 16 32 64 128	
boolean	SET.AND	E		8 16 32 64 128	
	SET	NE			
	SET	L GE G LE	NONE U	8 16 32 64 128	
	SET	G GE L LE	Z	8 16 32 64 128	

**Format**

G.op.size rd=rb,rc

rd=gopsize(rb,rc)

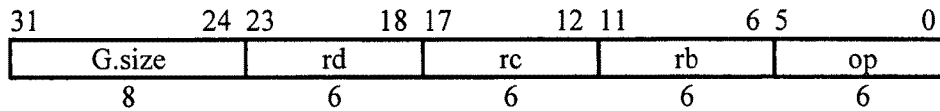


FIG. 33B

**Definition**

```

def GroupReversed(op,size,rd,rc,rb)
  c ← RegRead(rc, 128)
  b ← RegRead(rb, 128)
  case op of
    G.SUB:
      for i ← 0 to 128-size by size
        ai+size-1..i ← bi+size-1..i - ci+size-1..i
      endfor
    G.SUB.L:
      for i ← 0 to 128-size by size
        t ← (bi+size-1 || bi+size-1..i) - (ci+size-1 || ci+size-1..i)
        ai+size-1..i ← (tsize ≠ tsize-1) ? (tsize || 18[128-1]) : tsize-1..0
      endfor
    G.SUB.LU:
      for i ← 0 to 128-size by size
        t ← (01 || bi+size-1..i) - (01 || ci+size-1..i)
        ai+size-1..i ← (tsize ≠ 0) ? 0size : tsize-1..0
      endfor
    G.SUB.O:
      for i ← 0 to 128-size by size
        t ← (bi+size-1 || bi+size-1..i) - (ci+size-1 || ci+size-1..i)
        if (tsize ≠ tsize-1) then
          raise FixedPointArithmetic
        endif
        ai+size-1..i ← tsize-1..0
      endfor
    G.SUB.U.O:
      for i ← 0 to 128-size by size
        t ← (01 || bi+size-1..i) - (01 || ci+size-1..i)
        if (tsize ≠ 0) then
          raise FixedPointArithmetic
        endif
        ai+size-1..i ← tsize-1..0
      endfor
    G.SET.E:
      for i ← 0 to 128-size by size
        ai+size-1..i ← (bi+size-1..i = ci+size-1..i)size
      endfor
    G.SET.NE:
      for i ← 0 to 128-size by size
        ai+size-1..i ← (bi+size-1..i ≠ ci+size-1..i)size
      endfor
    G.SET.AND.E:
      for i ← 0 to 128-size by size
        ai+size-1..i ← ((bi+size-1..i and ci+size-1..i) = 0)size
      endfor
  endcase
enddef

```

FIG. 33C

```

G.SET.AND.NE:
  for i ← 0 to 128-size by size
    ai+size-1..i ← ((bi+size-1..i and ci+size-1..i) ≠ 0)size
  endfor
G.SET.L:
  for i ← 0 to 128-size by size
    ai+size-1..i ← ((rc = rb) ? (bi+size-1..i < 0) : (bi+size-1..i < ci+size-1..i))size
  endfor
G.SET.GE:
  for i ← 0 to 128-size by size
    ai+size-1..i ← ((rc = rb) ? (bi+size-1..i ≥ 0) : (bi+size-1..i ≥ ci+size-1..i))size
  endfor
G.SET.L.U:
  for i ← 0 to 128-size by size
    ai+size-1..i ← ((rc = rb) ? (bi+size-1..i > 0) :
      ((0 || bi+size-1..i) < (0 || ci+size-1..i))size)
  endfor
G.SET.GE.U:
  for i ← 0 to 128-size by size
    ai+size-1..i ← ((rc = rb) ? (bi+size-1..i ≤ 0) :
      ((0 || bi+size-1..i) ≥ (0 || ci+size-1..i))size)
  endfor
endcase
RegWrite(rd, 128, a)
enddef

```

**Exceptions**  
Fixed-point arithmetic

FIG. 33C *continued*

E.DIV.64	Ensemble divide signed octlets
E.DIV.U.64	Ensemble divide unsigned octlets
E.MUL.8	Ensemble multiply signed bytes
E.MUL.16	Ensemble multiply signed doublets
E.MUL.32	Ensemble multiply signed quadlets
E.MUL.64	Ensemble multiply signed octlets
E.MUL.SUM.8	Ensemble multiply sum signed bytes
E.MUL.SUM.16	Ensemble multiply sum signed doublets
E.MUL.SUM.32	Ensemble multiply sum signed quadlets
E.MUL.SUM.64	Ensemble multiply sum signed octlets
E.MUL.C.8	Ensemble complex multiply bytes
E.MUL.C.16	Ensemble complex multiply doublets
E.MUL.C.32	Ensemble complex multiply quadlets
E.MUL.M.8	Ensemble multiply mixed-signed bytes
E.MUL.M.16	Ensemble multiply mixed-signed doublets
E.MUL.M.32	Ensemble multiply mixed-signed quadlets
E.MUL.M.64	Ensemble multiply mixed-signed octlets
E.MUL.P.8	Ensemble multiply polynomial bytes
E.MUL.P.16	Ensemble multiply polynomial doublets
E.MUL.P.32	Ensemble multiply polynomial quadlets
E.MUL.P.64	Ensemble multiply polynomial octlets
E.MUL.SUM.C.8	Ensemble multiply sum complex bytes
E.MUL.SUM.C.16	Ensemble multiply sum complex doublets
E.MUL.SUM.C.32	Ensemble multiply sum complex quadlets
E.MUL.SUM.M.8	Ensemble multiply sum mixed-signed bytes
E.MUL.SUM.M.16	Ensemble multiply sum mixed-signed doublets
E.MUL.SUM.M.32	Ensemble multiply sum mixed-signed quadlets
E.MUL.SUM.M.64	Ensemble multiply sum mixed-signed octlets
E.MUL.SUM.U.8	Ensemble multiply sum unsigned bytes
E.MUL.SUM.U.16	Ensemble multiply sum unsigned doublets
E.MUL.SUM.U.32	Ensemble multiply sum unsigned quadlets
E.MUL.SUM.U.64	Ensemble multiply sum unsigned octlets
E.MUL.U.8	Ensemble multiply unsigned bytes
E.MUL.U.16	Ensemble multiply unsigned doublets
E.MUL.U.32	Ensemble multiply unsigned quadlets
E.MUL.U.64	Ensemble multiply unsigned octlets

FIG. 34A

**Format**

**E.op.size rd=rc,rb**

**rd=eopsize(rc,rb)**

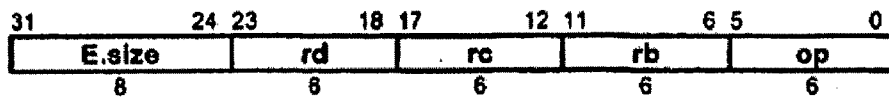


FIG. 34B

**Definition**

```

def mul(size,h,vs,vj,ws,wj) as
    mul ← ((vs&vsize-1+j)h-size || vsize-1+1..i) * ((ws&wsize-1+j)h-size || wsize-1+j..i)
enddef

def c ← PolyMultiply(size,a,b) as
    p[0] ← 02*size
    for k ← 0 to size-1
        p[k+1] ← p[k] ^ ak ? (0size-k || b || 0k) : 02*size
    endfor
    c ← p[size]
enddef

def Ensemble(op,size,rd,rc,rb)
    c ← RegRead(rc, 128)
    b ← RegRead(rb, 128)
    case op of
        E.MUL, E.MUL.C, EMULSUM, E.MUL.SUM.C, E.CON, E.CON.C, E.DIV:
            cs ← bs ← 1
        E.MUL.M, EMULSUM.M, E.CON.M:
            cs ← 0
            bs ← 1
        E.MUL.U, EMULSUM.U, E.CON.U, E.DIV.U, E.MUL.P:
            cs ← bs ← 0
    endcase
    case op of
        E.MUL, E.MUL.U, E.MUL.M:
            for i ← 0 to 64-size by size
                d2*(i+size)-1..2i ← mul(size,2*size,cs,c,i,bs,b,i)
            endfor
        E.MUL.P:
            for i ← 0 to 64-size by size
                d2*(i+size)-1..2i ← PolyMultiply(size,csize-1+1..i,bsize-1+i,i)
            endfor
        E.MUL.C:
            for i ← 0 to 64-size by size
                if (i and size) = 0 then
                    p ← mul(size,2*size,1,c,i,1,b,i) - mul(size,2*size,1,c,i+size,1,b,i+size)
                else
                    p ← mul(size,2*size,1,c,i,1,b,i+size) + mul(size,2*size,1,c,i,1,b,i+size)
                endif
                d2*(i+size)-1..2i ← P
            endfor
        E.MUL.SUM, E.MUL.SUM.U, E.MULSUM.M:
            p[0] ← 0128
            for i ← 0 to 128-size by size
                p[i+size] ← p[i] + mul(size,128,cs,c,i,bs,b,i)
            endfor
            a ← p[128]
        E.MUL.SUM.C:
            p[0] ← 064
            p[size] ← 064
            for i ← 0 to 128-size by size
                if (i and size) = 0 then
                    p[i+2*size] ← p[i] + mul(size,64,1,c,i,1,b,i)
                    - mul(size,64,1,c,i+size,1,b,i+size)
                else
                    p[i+2*size] ← p[i] + mul(size,64,1,c,i,1,b,i+size)
                    + mul(size,64,1,c,i+size,1,b,i)
                endif
            endfor
            a ← p[128+size] || p[128]
    endcase
enddef

```

FIG. 34C

```

E.CON, E.CON.U, E.CON.M:
  p[0] ← 0128
  for j ← 0 to 64-size by size
    for i ← 0 to 64-size by size
      p[j+size]2*(i+size)-1..2i ← p[0]2*(i+size)-1..2i +
        mul(size, 2*size, cs, c, i+64-j, bs, b, j)
    endfor
  endfor
  a ← p[64]
E.CON.C:
  p[0] ← 0128
  for j ← 0 to 64-size by size
    for i ← 0 to 64-size by size
      if ((-i) and j and size) = 0 then
        p[j+size]2*(i+size)-1..2i ← p[0]2*(i+size)-1..2i +
          mul(size, 2*size, 1, c, i+64-j, 1, b, j)
      else
        p[j+size]2*(i+size)-1..2i ← p[0]2*(i+size)-1..2i *
          mul(size, 2*size, 1, c, i+64-j+2*size, 1, b, j)
      endif
    endfor
  endfor
  a ← p[64]
E.DIV:
  if (b = 0) or ( (c = (1||063)) and (b = 164) ) then
    a ← undefined
  else
    q ← c / b
    r ← c - q*b
    a ← r63..0 || q63..0
  endif
E.DIV.U:
  if b = 0 then
    a ← undefined
  else
    q ← (0 || c) / (0 || b)
    r ← c - (0 || q)*(0 || b)
    a ← r63..0 || q63..0
  endif
endcase
RegWrite(rd, 128, a)
enddef

```

**Exceptions**

none



## Operation codes

G.COM.AND.E. 8	Group compare and equal zero bytes
G.COM.AND.E. 16	Group compare and equal zero doublets
G.COM.AND.E. 32	Group compare and equal zero quadlets
G.COM.AND.E. 64	Group compare and equal zero octlets
G.COM.AND.E.128	Group compare and equal zero hexlet
G.COM.AND.NE. 8	Group compare and not equal zero bytes
G.COM.AND.NE. 16	Group compare and not equal zero doublets
G.COM.AND.NE. 32	Group compare and not equal zero quadlets
G.COM.AND.NE. 64	Group compare and not equal zero octlets
G.COM.AND.NE.128	Group compare and not equal zero hexlet
G.COM.E. 8	Group compare equal bytes
G.COM.E. 16	Group compare equal doublets
G.COM.E. 32	Group compare equal quadlets
G.COM.E. 64	Group compare equal octlets
G.COM.E.128	Group compare equal hexlet
G.COM.GE. 8	Group compare greater equal signed bytes
G.COM.GE. 16	Group compare greater equal signed doublets
G.COM.GE. 32	Group compare greater equal signed quadlets
G.COM.GE. 64	Group compare greater equal signed octlets
G.COM.GE.128	Group compare greater equal signed hexlet
G.COM.GE.U. 8	Group compare greater equal unsigned bytes
G.COM.GE.U. 16	Group compare greater equal unsigned doublets
G.COM.GE.U. 32	Group compare greater equal unsigned quadlets
G.COM.GE.U. 64	Group compare greater equal unsigned octlets
G.COM.GE.U.128	Group compare greater equal unsigned hexlet
G.COM.L. 8	Group compare signed less bytes
G.COM.L. 16	Group compare signed less doublets
G.COM.L. 32	Group compare signed less quadlets
G.COM.L. 64	Group compare signed less octlets
G.COM.L.128	Group compare signed less hexlet
G.COM.L.U. 8	Group compare less unsigned bytes
G.COM.L.U. 16	Group compare less unsigned doublets
G.COM.L.U. 32	Group compare less unsigned quadlets
G.COM.L.U. 64	Group compare less unsigned octlets
G.COM.L.U.128	Group compare less unsigned hexlet
G.COM.NE. 8	Group compare not equal bytes
G.COM.NE. 16	Group compare not equal doublets
G.COM.NE. 32	Group compare not equal quadlets
G.COM.NE. 64	Group compare not equal octlets
G.COM.NE.128	Group compare not equal hexlet

FIG. 35A

**Equivalencies**

<i>G.COM.E.Z. 8</i>	Group compare equal zero signed bytes
<i>G.COM.E.Z. 16</i>	Group compare equal zero signed doublets
<i>G.COM.E.Z. 32</i>	Group compare equal zero signed quadlets
<i>G.COM.E.Z. 64</i>	Group compare equal zero signed octlets
<i>G.COM.E.Z.128</i>	Group compare equal zero signed hexlet
<i>G.COM.G. 8</i>	Group compare signed greater bytes
<i>G.COM.G. 16</i>	Group compare signed greater doublets
<i>G.COM.G. 32</i>	Group compare signed greater quadlets
<i>G.COM.G. 64</i>	Group compare signed greater octlets
<i>G.COM.G.128</i>	Group compare signed greater hexlet
<i>G.COM.G.U. 8</i>	Group compare greater unsigned bytes
<i>G.COM.G.U. 16</i>	Group compare greater unsigned doublets
<i>G.COM.G.U. 32</i>	Group compare greater unsigned quadlets
<i>G.COM.G.U. 64</i>	Group compare greater unsigned octlets
<i>G.COM.G.U.128</i>	Group compare greater unsigned hexlet
<i>G.COM.G.Z. 8</i>	Group compare greater zero signed bytes
<i>G.COM.G.Z. 16</i>	Group compare greater zero signed doublets
<i>G.COM.G.Z. 32</i>	Group compare greater zero signed quadlets
<i>G.COM.G.Z. 64</i>	Group compare greater zero signed octlets
<i>G.COM.G.Z.128</i>	Group compare greater zero signed hexlet
<i>G.COM.GE.Z. 8</i>	Group compare greater equal zero signed bytes
<i>G.COM.GE.Z. 16</i>	Group compare greater equal zero signed doublets
<i>G.COM.GE.Z. 32</i>	Group compare greater equal zero signed quadlets
<i>G.COM.GE.Z. 64</i>	Group compare greater equal zero signed octlets
<i>G.COM.GE.Z.128</i>	Group compare greater equal zero signed hexlet
<i>G.COM.L.Z. 8</i>	Group compare less zero signed bytes
<i>G.COM.L.Z. 16</i>	Group compare less zero signed doublets
<i>G.COM.L.Z. 32</i>	Group compare less zero signed quadlets
<i>G.COM.L.Z. 64</i>	Group compare less zero signed octlets
<i>G.COM.L.Z.128</i>	Group compare less zero signed hexlet
<i>G.COM.LE. 8</i>	Group compare less equal signed bytes
<i>G.COM.LE. 16</i>	Group compare less equal signed doublets
<i>G.COM.LE. 32</i>	Group compare less equal signed quadlets
<i>G.COM.LE. 64</i>	Group compare less equal signed octlets
<i>G.COM.LE.128</i>	Group compare less equal signed hexlet
<i>G.COM.LE.U. 8</i>	Group compare less equal unsigned bytes
<i>G.COM.LE.U. 16</i>	Group compare less equal unsigned doublets
<i>G.COM.LE.U. 32</i>	Group compare less equal unsigned quadlets
<i>G.COM.LE.U. 64</i>	Group compare less equal unsigned octlets
<i>G.COM.LE.U.128</i>	Group compare less equal unsigned hexlet

FIG. 35A *continued*

<i>G.COM.LE.Z. 8</i>	Group compare less equal zero signed bytes
<i>G.COM.LE.Z. 16</i>	Group compare less equal zero signed doublets
<i>G.COM.LE.Z. 32</i>	Group compare less equal zero signed quadlets
<i>G.COM.LE.Z. 64</i>	Group compare less equal zero signed octlets
<i>G.COM.LE.Z.128</i>	Group compare less equal zero signed hexlet
<i>G.COM.NE.Z. 8</i>	Group compare not equal zero signed bytes
<i>G.COM.NE.Z. 16</i>	Group compare not equal zero signed doublets
<i>G.COM.NE.Z. 32</i>	Group compare not equal zero signed quadlets
<i>G.COM.NE.Z. 64</i>	Group compare not equal zero signed octlets
<i>G.COM.NE.Z.128</i>	Group compare not equal zero signed hexlet
<i>G.FIX</i>	Group fixed point arithmetic exception
<i>G.NOP</i>	Group no operation

<i>G.COM.E.Z.size rc</i>	←	<i>G.COM.AND.E.size rc,rc</i>
<i>G.COM.G.size rd,rc</i>	→	<i>G.COM.L.size rc,rd</i>
<i>G.COM.G.U.size rd,rc</i>	→	<i>G.COM.L.U.size rc,rd</i>
<i>G.COM.G.Z.size rc</i>	⇐	<i>G.COM.L.U.size rc,rc</i>
<i>G.COM.GE.Z.size rc</i>	⇐	<i>G.COM.GE.size rc,rc</i>
<i>G.COM.L.Z.size rc</i>	⇐	<i>G.COM.L.size rc,rc</i>
<i>G.COM.LE.size rd,rc</i>	→	<i>G.COM.GE.size rc,rd</i>
<i>G.COM.LE.U.size rd,rc</i>	→	<i>G.COM.GE.U.size rc,rd</i>
<i>G.COM.LE.Z.size rc</i>	⇐	<i>G.COM.GE.U.size rc,rc</i>
<i>G.COM.NE.Z.size rc</i>	←	<i>G.COM.AND.NE.size rc,rc</i>
<i>G.FIX</i>	←	<i>G.COM.E.128 r0,r0</i>
<i>G.NOP</i>	←	<i>G.COM.NE.128 r0,r0</i>

FIG. 35A continued

**Redundancies**

G.COM.E.size rd,rd	⇔	<i>G.FIX</i>
G.COM.NE.size rd,rd	⇔	<i>G.NOP</i>

**Selection**

class	operation	cond	type	size
boolean	COM.AN D COM	E NE		8 16 32 64 128
arithmetic	COM	L GE <i>G LE</i>	NONE U	□ 16 32 64 128
	<i>COM</i>	<i>L GE G LE E NE</i>	Z	8 16 32 64 128

**Format**

G.COM.op.size rd,rc

G.COM.opz.size rcd

gcomopsize(rd,rc)

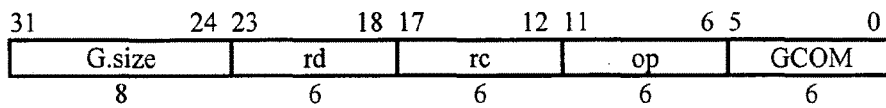


FIG. 35B

**Definition**

```

def GroupCompare(op,size,rd,rc)
  d ← RegRead(rd, 128)
  c ← RegRead(rc, 128)
  case op of
    G.COM.E:
      for i ← 0 to 128-size by size
         $a_{i+size-1..i} \leftarrow (d_{i+size-1..i} = c_{i+size-1..i})^{size}$ 
      endfor
    G.COM.NE:
      for i ← 0 to 128-size by size
         $a_{i+size-1..i} \leftarrow (d_{i+size-1..i} \neq c_{i+size-1..i})^{size}$ 
      endfor
    G.COM.AND.E:
      for i ← 0 to 128-size by size
         $a_{i+size-1..i} \leftarrow ((c_{i+size-1..i} \text{ and } d_{i+size-1..i}) = 0)^{size}$ 
      endfor
    G.COM.AND.NE:
      for i ← 0 to 128-size by size
         $a_{i+size-1..i} \leftarrow ((c_{i+size-1..i} \text{ and } d_{i+size-1..i}) \neq 0)^{size}$ 
      endfor
    G.COM.L:
      for i ← 0 to 128-size by size
         $a_{i+size-1..i} \leftarrow ((rd = rc) ? (c_{i+size-1..i} < 0) : (d_{i+size-1..i} < c_{i+size-1..i}))^{size}$ 
      endfor
    G.COM.GE:
      for i ← 0 to 128-size by size
         $a_{i+size-1..i} \leftarrow ((rd = rc) ? (c_{i+size-1..i} \geq 0) : (d_{i+size-1..i} \geq c_{i+size-1..i}))^{size}$ 
      endfor
    G.COM.L.U:
      for i ← 0 to 128-size by size
         $a_{i+size-1..i} \leftarrow ((rd = rc) ? (c_{i+size-1..i} > 0) :$ 
           $((0 \parallel d_{i+size-1..i}) < (0 \parallel c_{i+size-1..i})))^{size}$ 
      endfor
    G.COM.GE.U:
      for i ← 0 to 128-size by size
         $a_{i+size-1..i} \leftarrow ((rd = rc) ? (c_{i+size-1..i} \leq 0) :$ 
           $((0 \parallel d_{i+size-1..i}) \geq (0 \parallel c_{i+size-1..i})))^{size}$ 
      endfor
  endcase
  if (a ≠ 0) then
    raise FixedPointArithmetic
  endif
enddef

```

**Exceptions**

Fixed-point arithmetic

FIG. 35C

E.LOG.MOST.8	Ensemble log of most significant bit signed bytes
E.LOG.MOST.16	Ensemble log of most significant bit signed doublets
E.LOG.MOST.32	Ensemble log of most significant bit signed quadlets
E.LOG.MOST.64	Ensemble log of most significant bit signed octlets
E.LOG.MOST.128	Ensemble log of most significant bit signed hexlet
E.LOG.MOST.U.8	Ensemble log of most significant bit unsigned bytes
E.LOG.MOST.U.16	Ensemble log of most significant bit unsigned doublets
E.LOG.MOST.U.32	Ensemble log of most significant bit unsigned quadlets
E.LOG.MOST.U.64	Ensemble log of most significant bit unsigned octlets
E.LOG.MOST.U.128	Ensemble log of most significant bit unsigned hexlet
E.SUM.8	Ensemble sum signed bytes
E.SUM.16	Ensemble sum signed doublets
E.SUM.32	Ensemble sum signed quadlets
E.SUM.64	Ensemble sum signed octlets
E.SUM.U.1	Ensemble sum unsigned bits
E.SUM.U.8	Ensemble sum unsigned bytes
E.SUM.U.16	Ensemble sum unsigned doublets
E.SUM.U.32	Ensemble sum unsigned quadlets
E.SUM.U.64	Ensemble sum unsigned octlets

**Selection**

class	op	size
sum	SUM	8 16 32 64
	SUM.U	1 8 16 32 64
log most significant bit	LOG.MOST LOG.MOST.U	8 16 32 64 128

FIG. 36A

**Format**

E.op.size rd=rc

rd=eopsize(rc)

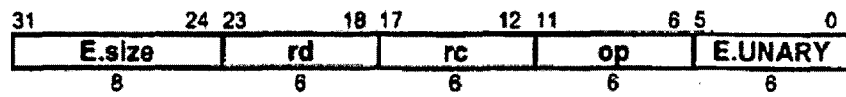


FIG. 36B

**Definition**

```

def EnsembleUnary(op,size,rd,rc)
  c ← RegRead(rc, 128)
  case op of
    E.LOG.MOST:
      for i ← 0 to 128-size by size
        if (ci+size-1..i = 0) then
          ai+size-1..i ← -1
        else
          for j ← 0 to size-1
            if csize-1+i..j+i = (csize-1+j || not csize-1+i) then
              ai+size-1..i ← j
            endif
          endfor
        endif
      endfor
    E.LOG.MOSTU:
      for i ← 0 to 128-size by size
        if (ci+size-1..i = 0) then
          ai+size-1..i ← -1
        else
          for j ← 0 to size-1
            if csize-1+i..j+i = (0size-1-j || 1) then
              ai+size-1..i ← j
            endif
          endfor
        endif
      endfor
    E.SUM:
      p[0] ← 0128
      for i ← 0 to 128-size by size
        p[i+size] ← p[i] + (csize-1+i128-size || csize-1+i..i)
      endfor
      a ← p[128]
    E.SUMU:
      p[0] ← 0128
      for i ← 0 to 128-size by size
        p[i+size] ← p[i] + (0128-size || csize-1+i..i)
      endfor
      a ← p[128]
  endcase
  RegWrite(rd, 128, a)
enddef

```

**Exceptions**

none

FIG. 36C



**Floating-point function Definitions**

```
def eb ← ebits(prec) as
  case pref of
    16:
      eb ← 5
    32:
      eb ← 8
    64:
      eb ← 11
    128:
      eb ← 15
  endcase
enddef

def eb ← ebias(prec) as
  eb ← 0 || 1ebits(prec)-1
enddef

def fb ← fbits(prec) as
  fb ← prec - 1 - eb
enddef

def a ← F(prec, ai) as
  a.s ← aiprec-1
  ae ← aiprec-2..fbits(prec)
  af ← aifbits(prec)-1..0
  if ae = 1ebits(prec) then
    if af = 0 then
      a.t ← INFINITY
    elseif affbits(prec)-1 then
      a.t ← SNaN
      a.e ← -fbits(prec)
      a.f ← 1 || affbits(prec)-2..0
    else
      a.t ← QNaN
      a.e ← -fbits(prec)
      a.f ← af
    endif
  endif
```

FIG. 37

```

elseif ae = 0 then
  if af = 0 then
    a.t ← ZERO
  else
    a.t ← NORM
    a.e ← 1 - ebias(prec) - fbits(prec)
    a.f ← 0 || af
  endif
else
  a.t ← NORM
  a.e ← ae - ebias(prec) - fbits(prec)
  a.f ← 1 || af
endif
enddef

def a ← DEFAULTQNaN as
  a.s ← 0
  a.t ← QNaN
  a.e ← -1
  a.f ← 1
enddef

def a ← DEFAULTSNAN as
  a.s ← 0
  a.t ← SNAN
  a.e ← -1
  a.f ← 1
enddef

def fadd(a,b) as faddr(a,b,N) enddef

def c ← faddr(a,b,round) as
  if a.t=NORM and b.t=NORM then
    // d,e are a,b with exponent aligned and fraction adjusted
    if a.e > b.e then
      d ← a
      e.t ← b.t
      e.s ← b.s
      e.e ← a.e
      e.f ← b.f || 0a.e-b.e
    else if a.e < b.e then
      d.t ← a.t
      d.s ← a.s
      d.e ← b.e
      d.f ← a.f || 0b.e-a.e
      e ← b
    endif
    c.t ← d.t
    c.e ← d.e
    if d.s = e.s then
      c.s ← d.s
      c.f ← d.f + e.f
    elseif d.f > e.f then
      c.s ← d.s
      c.f ← d.f - e.f

```

FIG. 37 continued

```

elseif d.f < e.f then
    c.s ← e.s
    c.f ← e.f - d.f
else
    c.e ← r=F
    c.l ← ZERO
endif
// priority is given to b operand for NaN propagation
elseif (b.t=SNAN) or (b.t=QNAN) then
    c ← b
elseif (a.t=SNAN) or (a.t=QNAN) then
    c ← a
elseif a.t=ZERO and b.t=ZERO then
    c.l ← ZERO
    c.s ← (a.s and b.s) or (round=F and (a.s or b.s))
// NULL values are like zero, but do not combine with ZERO to alter sign
elseif a.t=ZERO or a.t=NULL then
    c ← b
elseif b.t=ZERO or b.t=NULL then
    c ← a
elseif a.t=INFINITY and b.t=INFINITY then
    if a.s ≠ b.s then
        c ← DEFAULTSNAN // Invalid
    else
        c ← a
    endif
elseif a.t=INFINITY then
    c ← a
elseif b.t=INFINITY then
    c ← b
else
    assert FALSE // should have covered all the cases above
endif
enddef

def b ← fneg(a) as
    b.s ← -a.s
    b.t ← a.t
    b.e ← a.e
    b.f ← a.f
enddef

def fsub(a,b) as fsub(a,b,N) enddef

def fsubr(a,b,round) as faddr(fneg(b),round) enddef

def frsub(a,b) as frsubr(a,b,N) enddef

def frsubr(a,b,round) as faddr(fneg(a),b,round) enddef

def c ← fcom(a,b) as
    if (a.t=SNAN) or (a.t=QNAN) or (b.t=SNAN) or (b.t=QNAN) then
        c ← U
    elseif a.t=INFINITY and b.t=INFINITY then
        if a.s ≠ b.s then
            c ← (a.s=0) ? G: L

```

FIG. 37 continued

```

    else
        c ← E
    endif
elseif a.t=INFINITY then
    c ← (a.s=0) ? G: L
elseif b.t=INFINITY then
    c ← (b.s=0) ? G: L
elseif a.t=NORM and b.t=NORM then
    if a.s ≠ b.s then
        c ← (a.s=0) ? G: L
    else
        if a.e > b.e then
            af ← a.f
            bf ← b.f || 0a.e-b.e
        else
            af ← a.f || 0b.e-a.e
            bf ← b.f
        endif
        if af = bf then
            c ← E
        else
            c ← ((a.s=0) ^ (af > bf)) ? G : L
        endif
    endif
elseif a.t=NORM then
    c ← (a.s=0) ? G: L
elseif b.t=NORM then
    c ← (b.s=0) ? G: L
elseif a.t=ZERO and b.t=ZERO then
    c ← E
else
    assert FALSE // should have covered all the cases above
endif
enddef

def c ← fmul(a,b) as
    if a.t=NORM and b.t=NORM then
        c.s ← a.s ^ b.s
        c.t ← NORM
        c.e ← a.e + b.e
        c.f ← a.f * b.f
        // priority is given to b operand for NaN propagation
    elseif (b.t=SNAN) or (b.t=QNAN) then
        c.s ← a.s ^ b.s
        c.t ← b.t
        c.e ← b.e
        c.f ← b.f
    elseif (a.t=SNAN) or (a.t=QNAN) then
        c.s ← a.s ^ b.s
        c.t ← a.t
        c.e ← a.e
        c.f ← a.f
    elseif a.t=ZERO and b.t=INFINITY then
        c ← DEFAULTSNAN // Invalid
    elseif a.t=INFINITY and b.t=ZERO then
        c ← DEFAULTSNAN // Invalid
    end
enddef

```

FIG. 37 continued