IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

LAKE CHEROKEE HARD DRIVE TECHNOLOGIES, LLC,	§	
Plaintiff,	§	
v.	§	CASE NO. 2:10-CV-216-JRG
BASS COMPUTERS, INC., et al.,	§	
Defendants.	§	

MEMORANDUM OPINION AND ORDER

Before the Court is the construction of the parties' disputed claim terms, which the Court previously addressed in its May 23, 2012 Provisional *Markman* Order. (Dkt. No. 255.) That Provisional Order is superseded by this expanded claim construction order; and this Order is and shall be effective as of May 23, 2012.

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BACKGROUND

Plaintiff filed suit on June 30, 2010, asserting United States Patents No. 5,844,738, titled "Synchronous Read Channel Employing a Sequence Detector with Programmable Detector Levels" ("the '738 Patent"), and 5,978,162, titled "Synchronous Read Channel Integrated Circuit Employing a Channel Quality Circuit for Calibration" ("the '162 Patent") (collectively "the patents-in-suit").[1] The parties have characterized these patents as relating to "read channels in magnetic storage devices, such as a hard disk drive." (Dkt. No. 217, at 1.)

The Abstract of the '738 Patent states:

> A synchronous read channel is disclosed which samples an analog read signal from a magnetic read head positioned over a magnetic disk medium, filters the sample values according to a desired partial response, extracts timing information from the filtered sample values, and detects an estimated data sequence from the filtered sample values using a trellis type sequence detector matched to the partial response. The trellis sequence detector comprises programmable detector levels which allows for maximum flexibility in matching the sequence detector to the partial response.

The Abstract of the '162 Patent states:

> A synchronous read channel is disclosed which samples an analog read signal from a magnetic read head positioned over a magnetic disk medium, filters the sample values according to a desired partial response, extracts timing information from the filtered sample values, and detects an estimated data sequence from the filtered sample values using a discrete time sequence detector. A Channel Quality circuit accumulates various signals generated by the read channel, such as sample errors, gain errors, timing errors, etc., for use in calibrating the read channel components and estimating the bit error rate.

The Background of the Invention describes various concerns in magnetic media read channels, that is, systems that read data from magnetic media. Data is represented by the presence or absence of "transitions" between magnetizations on the disk, such as a transition between a North-South magnetized region and a South-North magnetized region. This transition

[1] The '738 Patent and the '162 Patent are both divisionals of a prior application, so the '738 Patent and the '162 Patent have substantially similar specifications. The '162 Patent has an additional figure, Figure 7. References to the specification herein shall be to the '162 Patent unless otherwise indicated.

produces a voltage at the read head, which is sampled as the read head travels across the medium. One design objective is to maximize storage by putting data as close together as possible. The challenges include distortion, noise, timing variations, defects in the media, defects in how data was written to the media, and the limited sampling rate that can be achieved.

The Background of the Invention also mentions "zoned recording," which helps account for the spin speed of the disk drive being kept constant but the data transfer rate varying to at least partially account for the radius of the disk. That is, data tracks near the outside of the disk hold more data because the circumference near the outside of the disk is greater than the circumference near the center of the disk. The use of "zones" of tracks, however, still means that the transition spacing will vary between tracks within the same zone because of the difference in radius.

The Detailed Description of the Invention discloses techniques for sampling and filtering and, in particular: (1) a "partial response" sequence detector, which "allows the analog response of the read channel to a storage medium transition to overlap with the response to adjacent transitions associated with subsequent information bits," which "allows higher information storage densities" because the spacing between transitions can be reduced; (2) a modified "Viterbi detector," which "keeps a running tally of the error between the actual sample sequence and the sample sequence that would be expected if the medium had been written with a particular sequence of transitions. As more samples are taken, less likely choices for transition sequences are pruned from consideration"; and (3) the use of a "Channel Quality circuit 46," which can, for example, write a known data sequence to the medium and then, by reading the known data, "allow the microcontroller to find the best detector sample level sets (those which produce the minimum error rate) for each disk drive, head, and zone." ('162 Patent, at 9:49-60, 10:5-12 &

13:61-63.) The Channel Quality circuit, in other words, "provides not only quantitative channel evaluation, but in addition allows selection of read channel parameters . . . to best adapt the read channel to the characteristics of the storage medium and the pulse form and characteristics being read therefrom." (*Id.*, at 9:14-19.)

Plaintiff asserts Claims 1-10 of the '738 Patent (disputed terms are italicized):

> 1. A synchronous read channel for reading data recorded on a magnetic disk storage medium by detecting *binary data* from a sequence of *discrete time* sample values generated by sampling pulses in an analog read signal from a magnetic read head positioned over the magnetic disk storage medium, comprising:
>
> > (a) a sampling device for sampling the analog read signal to generate the *discrete time* time sample values;
> >
> > (b) a *discrete time* filter for filtering the *discrete time* sample values according to a partial response;
> >
> > (c) *discrete time* timing recovery for extracting timing information from the *discrete time* sample values; and
> >
> > (d) a *trellis type sequence detector for detecting the binary data from the sample values*, comprising programmable detector levels associated with a *state transition diagram* for matching the sequence detector to the partial response.
>
> 2. The synchronous read channel as recited in claim 1, wherein the programmable detector levels correspond to ideal sample values of an isolated pulse generated by an isolated magnetic transition.
>
> 3. The synchronous read channel as recited in claim 2, wherein there are two ideal sample values for the isolated pulse.
>
> 4. The synchronous read channel as recited in claim 2, wherein there are three ideal sample values for the isolated pulse.
>
> 5. The synchronous read channel as recited in claim 2, wherein there are four ideal sample values for the isolated pulse.
>
> 6. A synchronous read channel for reading data recorded on a magnetic disk storage medium by detecting *binary data* from a sequence of *discrete time* sample values generated by sampling pulses in an analog read signal from a magnetic read head positioned over the magnetic disk storage medium, comprising:

(a) a sampling device for sampling the analog read signal to generate the *discrete time* time sample values;

(b) a *discrete time* filter for filtering the *discrete time* sample values according to a partial response;

(c) a *trellis type sequence detector for detecting the binary data from the sample values*, comprising programmable detector levels associated with a *state transition diagram* for matching the sequence detector to the partial response.

7. The synchronous read channel as recited in claim 1, wherein the programmable detector levels correspond to ideal sample values of an isolated pulse generated by an isolated magnetic transition.

8. The synchronous read channel as recited in claim 2, wherein there are two ideal sample values for the isolated pulse.

9. The synchronous read channel as recited in claim 2, wherein there are three ideal sample values for the isolated pulse.

10. The synchronous read channel as recited in claim 2, wherein there are four ideal sample values for the isolated pulse.

Plaintiff asserts Claims 1-13 of the '162 Patent (disputed terms are italicized):

1. A synchronous read channel for reading data recorded on a magnetic disk storage medium by detecting *binary data* from a sequence of *discrete time* sample values generated by sampling pulses in an analog read signal from a magnetic read head positioned over the magnetic disk storage medium, comprising:

(a) a sampling device, responsive to a sampling clock, for sampling the analog read signal to generate the *discrete time* sample values;

(b) a timing recovery circuit, *responsive to the discrete time sample values*, for extracting timing information;

(c) a *discrete time sequence detector, responsive to the discrete time sample values, for detecting the binary data*; and

(d) a *channel quality circuit, responsive to the discrete time sample values*, for *calibrating the synchronous read channel*.

2. The synchronous read channel as recited in claim 1, wherein the *channel quality circuit* generates sample errors as the difference between the *discrete time* sample values and ideal sample values, the sample errors for use in *calibrating the synchronous read channel*.

3. The synchronous read channel as recited in claim 1, wherein:

(a) the timing recovery circuit comprises a phase-locked loop; and

(b) the *channel quality circuit* is used to calibrate the phase-locked loop.

4. The synchronous read channel as recited in claim 2, wherein the phase-locked loop comprises a phase error detector for generating a phase error used by the *channel quality circuit*.

5. The synchronous read channel as recited in claim 3, further comprising a *discrete time* gain control circuit, *responsive to the discrete time sample values*, for adjusting a magnitude of the analog read signal, wherein the *channel quality circuit* is used to calibrate the gain control circuit.

6. The synchronous read channel as recited in claim 5, wherein the *discrete time* gain control circuit generates a gain error used by the *channel quality circuit*.

7. The synchronous read channel as recited in claim 1, wherein:

(a) the *discrete time sequence detector* generates an error metric between the *discrete time* sample values and ideal sample values; and

(b) the *channel quality circuit* uses the error metric to calibrate the synchronous read channel.

8. The synchronous read channel as recited in claim 1, further comprising a *discrete time* equalizer for equalizing the *discrete time* sample values according to a predetermined partial response, wherein the *channel quality circuit* is used to calibrate the *discrete time* equalizer.

9. The synchronous read channel as recited in claim 8, wherein the predetermined partial response is an EPR4 response.

10. The synchronous read channel as recited in claim 1, further comprising a zero phase start circuit for decreasing the time needed to acquire an acquisition preamble, wherein the *channel quality circuit* is used to calibrate the zero phase start circuit.

11. The synchronous read channel as recited in claim 1, further comprising a test pattern generator for generating a test pattern written to the magnetic disk storage medium and used during a read operation to generate measurement signals for use in *calibrating the synchronous read channel*.

12. The synchronous read channel as recited in claim 1, wherein the *channel quality circuit* calibrates detector sample levels in the *discrete time sequence detector*.

13. A synchronous read channel for reading data recorded on a magnetic disk storage medium by detecting *binary data* from a sequence of *discrete time* sample values generated by sampling pulses in an analog read signal from a magnetic read head positioned over the magnetic disk storage medium, comprising:

(a) a timing recovery circuit, *responsive to the discrete time sample values*, for extracting timing information;

(b) a *discrete time* equalizer for equalizing the *discrete time* sample values according to a predetermined partial response to generate equalized sample values;

(c) a *discrete time sequence detector*, responsive to the equalized sample values, *for detecting the binary data*; and

(d) a *channel quality circuit*, responsive to the equalized sample values, for *calibrating the synchronous read channel*.

LEGAL PRINCIPLES

It is understood that "[a] claim in a patent provides the metes and bounds of the right which the patent confers on the patentee to exclude others from making, using or selling the protected invention." *Burke, Inc. v. Bruno Indep. Living Aids, Inc.*, 183 F.3d 1334, 1340 (Fed. Cir. 1999). Claim construction is clearly an issue of law for the court to decide. *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 970-71 (Fed. Cir. 1995) (en banc), *aff'd*, 517 U.S. 370 (1996).

To ascertain the meaning of claims, courts look to three primary sources: the claims, the specification, and the prosecution history. *Markman*, 52 F.3d at 979. The specification must contain a written description of the invention that enables one of ordinary skill in the art to make and use the invention. *Id.* A patent's claims must be read in view of the specification, of which they are a part. *Id.* For claim construction purposes, the description may act as a sort of dictionary, which explains the invention and may define terms used in the claims. *Id.* "One

purpose for examining the specification is to determine if the patentee has limited the scope of the claims." *Watts v. XL Sys., Inc.*, 232 F.3d 877, 882 (Fed. Cir. 2000).

Nonetheless, it is the function of the claims, not the specification, to set forth the limits of the patentee's invention. Otherwise, there would be no need for claims. *SRI Int'l v. Matsushita Elec. Corp.*, 775 F.2d 1107, 1121 (Fed. Cir. 1985) (en banc). The patentee is free to be his own lexicographer, but any special definition given to a word must be clearly set forth in the specification. *Intellicall, Inc. v. Phonometrics, Inc.*, 952 F.2d 1384, 1388 (Fed. Cir. 1992). Although the specification may indicate that certain embodiments are preferred, particular embodiments appearing in the specification will not be read into the claims when the claim language is broader than the embodiments. *Electro Med. Sys., S.A. v. Cooper Life Sciences, Inc.*, 34 F.3d 1048, 1054 (Fed. Cir. 1994).

This Court's claim construction analysis is substantially guided by the Federal Circuit's decision in *Phillips v. AWH Corporation*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). In *Phillips*, the court set forth several guideposts that courts should follow when construing claims. In particular, the court reiterated that "the claims of a patent define the invention to which the patentee is entitled the right to exclude." 415 F.3d at 1312 (emphasis added) (quoting *Innova/Pure Water, Inc. v. Safari Water Filtration Systems, Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)). To that end, the words used in a claim are generally given their ordinary and customary meaning. *Id.* The ordinary and customary meaning of a claim term "is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." *Id.* at 1313. This principle of patent law flows naturally from the recognition that inventors are usually persons who are skilled in the

field of the invention and that patents are addressed to, and intended to be read by, others skilled in the particular art. *Id.*

Despite the importance of claim terms, *Phillips* made clear that "the person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification." *Id.* Although the claims themselves may provide guidance as to the meaning of particular terms, those terms are part of "a fully integrated written instrument." *Id.* at 1315 (quoting *Markman*, 52 F.3d at 978). Thus, the *Phillips* court emphasized the specification as being the best guide for construing the claims. *Id.* at 1314-17. As the Supreme Court stated long ago, "in case of doubt or ambiguity it is proper in all cases to refer back to the descriptive portions of the specification to aid in solving the doubt or in ascertaining the true intent and meaning of the language employed in the claims." *Bates v. Coe*, 98 U.S. 31, 38 (1878). In addressing the role of the specification, the *Phillips* court quoted with approval its earlier observations from *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998):

> Ultimately, the interpretation to be given a term can only be determined and confirmed with a full understanding of what the inventors actually invented and intended to envelop with the claim. The construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be, in the end, the correct construction.

Phillips, 415 F.3d at 1316. Consequently, *Phillips* emphasized the important role the specification plays in the claim construction process.

The prosecution history also continues to play an important role in claim interpretation. Like the specification, the prosecution history helps to demonstrate how the inventor and the Patent and Trademark Office ("PTO") understood the patent. *Id.* at 1317. Because the file

history, however, "represents an ongoing negotiation between the PTO and the applicant," it may lack the clarity of the specification and thus be less useful in claim construction proceedings. *Id.* Nevertheless, the prosecution history is intrinsic evidence that is relevant to the determination of how the inventor understood the invention and whether the inventor limited the invention during prosecution by narrowing the scope of the claims. *Id.*

Phillips rejected any claim construction approach that sacrificed the intrinsic record in favor of extrinsic evidence, such as dictionary definitions or expert testimony. The *en banc* court condemned the suggestion made by *Texas Digital Systems, Inc. v. Telegenix, Inc.*, 308 F.3d 1193 (Fed. Cir. 2002), that a court should discern the ordinary meaning of the claim terms (through dictionaries or otherwise) before resorting to the specification for certain limited purposes. *Phillips*, 415 F.3d at 1319-24. According to *Phillips*, reliance on dictionary definitions at the expense of the specification had the effect of "focus[ing] the inquiry on the abstract meaning of words rather than on the meaning of claim terms within the context of the patent." *Id.* at 1321. *Phillips* emphasized that the patent system is based on the proposition that the claims cover only the invented subject matter. *Id.*

Phillips does not preclude all uses of dictionaries in claim construction proceedings. Instead, the court assigned dictionaries a role subordinate to the intrinsic record. In doing so, the court emphasized that claim construction issues are not resolved by any magic formula. The court did not impose any particular sequence of steps for a court to follow when it considers disputed claim language. *Id.* at 1323-25. Rather, *Phillips* held that a court must attach the appropriate weight to the intrinsic sources offered in support of a proposed claim construction, bearing in mind the general rule that the claims measure the scope of the patent grant.

CONSTRUCTION OF AGREED TERMS

The parties have agreed to the construction of the following terms:

Claim Term/Phrase/Clause	Agreed Definition
Discrete time sample values	A digital value representing the amplitude of the analog read signal at the time the signal is sampled
Synchronous read channel	Integrated circuit whose function is to process the analog read or receive signal coming from a media into estimated user data bits, and that includes circuitry for synchronizing the sampling rate with the spacing of the bits written on the media.
For detecting the binary data	No construction necessary
For detecting the binary data from the sample values.	No construction necessary
Extracting timing information from the discrete time sample values	Extracting timing information from the digital values representing the amplitudes of the analog read signal at the time it is sampled
Detector levels	Expected sample levels that the sequence detector receives

(*See* Dkt. No. 207). In view of the parties' agreements on the proper construction of each of the identified terms, the Court adopts the parties' agreed-upon constructions as set forth above. These agreed-upon constructions govern in this case as to these particular terms.

CONSTRUCTION OF DISPUTED TERMS

The parties have presented nine disputed terms for construction. In line with the parties' briefing, the Court uses Roman numerals to identify the disputed terms.

A. "Binary Data"

Plaintiff's Proposed Construction	Defendants' Proposed Construction
"Data that has two possible states (such as 0 or 1), also known as data bits"	"User-data that has two possible states"

This term appears in Claims 1 and 6 of the '738 Patent and Claims 1 and 13 of the '162 Patent.

(a) The Parties' Positions

Plaintiff proposes this term means "data that has two possible states (such as 0 or 1), also known as data bits." (Dkt. No. 237-1, at 1) Defendants propose this term means "user-data that has two possible states." (*Id.*)

Plaintiff argues that "binary data" should not be limited to "user" data because the ordinary meaning of "binary data" is not so limited and because the specification sets forth no such limitation. (Dkt. No. 217, at 1-2.) Plaintiff also argues that the term "user-data," proposed by Defendants, "is unclear and introduces ambiguity." (*Id.*, at 2.) Plaintiff further argues that the example set forth in Plaintiff's proposed construction is accurate, is taken from the specification, and would be useful to the jury. (*Id.*)

Defendants argue that the specification discloses, in Defendants words, that "the read channel does not detect just any arbitrary binary data; its whole purpose is to detect the estimated 'user' data bits." (Dkt. No. 225, at 2 (citing '162 Patent, at 1:12-26).) Defendants also note that the parties' agreed construction for "synchronous read channel" refers to "user data bits." (Dkt. No. 225, at 2.) Defendants emphasize that "a read channel would be worthless if all it could detect was any arbitrary stream of binary data bits" rather than "the actual data written on the magnetic disks by the user who saved the data." (*Id.*, at 3.) Finally, Defendants argue that the

example in Plaintiff's proposal is "potentially confusing," particularly because even though "[b]inary data is sometimes modeled as ones and zeroes, . . . in reality, data stored on the magnetic disk takes the form of transitions between 'North' or 'South' magnetization." (*Id.*, at 4.) Moreover, Defendants argue that Plaintiff's reference to "data bits" is redundant and "creates potential confusion." (*Id.*)

Plaintiff replies that its proposal of "such as 0 or 1" is merely an example and that "the jury is more likely to be familiar with data bits, consisting of 0s and 1s, than the abstract notion of 'data that has two possible states.'" (Dkt. No. 235, at 1.) Plaintiff's reply brief does not address Defendants' argument that Plaintiff already agreed to limit the term "synchronous read channel" to "user data bits." (*See* Dkt. No. 235.)

Defendants' sur-reply does not address this term. (*See* Dkt. No. 242.)

(b) Analysis

In their March 6, 2012 Joint Claim Construction and Prehearing Statement Pursuant to Patent Local Rule 4-3, the parties submitted their agreement that the term "synchronous read channel" means "integrated circuit whose function is to process the analog read or receive signal coming from a media into estimated *user* data bits, and that includes circuitry for synchronizing the sampling rate with the spacing of the bits written on the media." (Dkt. No. 207, at Ex. A (emphasis added).) The term "synchronous read channel" appears in the preamble of every claim of the patents-in-suit. The term "binary data" appears in the preamble of every claim in which "binary data" appears in the body, that is, Claims 1 and 6 of the '738 Patent and Claims 1 and 13 of the '162 Patent. As an example, Claim 1 of the '162 Patent recites (emphasis added):

> 1. A *synchronous read channel* for reading data recorded on a magnetic disk storage medium by detecting *binary data* from a sequence of discrete time sample values generated by sampling pulses in an analog read signal from a magnetic read head positioned over the magnetic disk storage medium, comprising:

> (a) a sampling device, responsive to a sampling clock, for sampling the analog read signal to generate the discrete time sample values;
>
> (b) a timing recovery circuit, responsive to the discrete time sample values, for extracting timing information;
>
> (c) a discrete time sequence detector, responsive to the discrete time sample values, for detecting *the binary data*; and
>
> (d) a channel quality circuit, responsive to the discrete time sample values, for calibrating the synchronous read channel.

On one hand, the parties' agreed construction, together with the context of "binary data" appearing in the preamble together with "synchronous read channel," suggests that the recited "binary data" is user data. On the other hand, the specification explains that user data is modified before being recorded onto a magnetic medium:

> The analog read or receive signal coming from the media is demodulated to detect or extract estimated channel bits, which are then decoded into estimated user-data bits.
> * * *
> It is common to use run-length-limited (RLL) encoding of the original user data bits, which are arbitrary or unconstrained, into an RLL-encoded stream of channel bits. It may be desirable that there be no less than d zeroes between ones; that is, that the media transitions be spaced by at least d+1 channel bit times. This constraint can help keep to a manageable level the interference effects among the pulses in the analog read signal. On the other hand, because media transitions provide timing information that must be extracted from the read signal to ensure synchronization of the demodulator with the pulses in the read signal, it may be desirable that there be no more than k zeroes between ones; that is, that there be a media transition at least every k'th channel bit time. An RLL(d,k) code is a code that can encode an arbitrary stream of original user-data bits into a stream of channel bits such that the encoded channel bit stream satisfies these two constraints. An RLL code has a theoretical capacity which limits the number of user bits which can be represented in a given number of RLL bits. The capacity is a function of the d and k constraints with d=0 and k=infinite being the limiting (unconstrained) case with a capacity of exactly one. The capacity of an RLL (1,7) code for example is just slightly greater than 2/3 and is exactly 2/3 for any practical implementation, meaning that every pair of user bits will map to exactly three RLL bits.

('162 Patent at 1:20-24 & 1:47-2:4.) In other words, the "original user data bits" are encoded into "RLL bits," and RLL encoding limits the minimum and maximum number of consecutive bits of the same value. At the May 14, 2012 hearing, Defendants argued that if the construction of "binary data" is not limited to *user* data bits, then the term "binary data" would improperly cover the "estimated channel bits," which Defendants submit are not "binary data." On balance, the better reading of the above-quoted passage and the claims is that RLL channel bits are a type of "binary data" that is "detect[ed]." (*Id.*; *see* '162 Patent at Claim 1(c).) Including the phrase "user-data" in the construction would therefore be misleading or inaccurate because the channel bits are different from the user data bits. The Court therefore rejects Defendants' proposed construction.

Next, the "example" of "0 or 1" in Plaintiff's proposed construction would be useful to the jury in understanding the meaning of "binary," but Defendants have legitimate concern that the phrase "such as 0 or 1" might be read by the jury as limiting. The Court therefore replaces "such as" with "for example."

Finally, the "example" of "also known as data bits" in Plaintiff's proposed construction is redundant and could be confusing and potentially inaccurate. This proposed example should therefore be omitted from the Court's construction.

The Court therefore hereby construes **"binary data"** to mean **"data that has two possible states (for example, 0 or 1)."**

B. "Discrete Time"

Plaintiff's Proposed Construction	**Defendants' Proposed Construction**
"time represented in discrete intervals, also known as digital time"	No construction is necessary

This term appears in Claims 1 and 6 of the '738 Patent and Claims 1, 2, 5, 6, 7, 8, 12, 13 and 15 of the '162 Patent.

(a) The Parties' Positions

Plaintiff proposes this term means "time represented at discrete intervals, also known as digital time." (Dkt. No. 237-1, at 1-2 & 12.) Defendants propose that "[n]o construction is necessary." (*Id.*)

Plaintiff argues that its proposal is "consistent with the ordinary meaning." (Dkt. No. 217, at 8.) Plaintiff cites a dictionary definition as well as testimony of a technical employee of Defendant Marvell Semiconductor, Inc. (*Id.*) Plaintiff submits that jurors would much more easily understand the term "digital time" than the term "discrete time." (*Id.*, at 9.)

Defendants respond that "[d]iscrete' and 'time' are common words" that need no construction. (Dkt. No. 225, at 9.) Defendants argue that even assuming that "discrete" and "digital" are interchangeable terms, interchanging them would serve no useful purpose. (*Id.*)

Plaintiff replies that this term requires construction because "discrete time" has no ordinary, commonly understood meaning and because the ordinary meanings of "discrete" and "time," when combined, would not yield the proper meaning. (Dkt. No. 235, at 3.) Plaintiff also argues that "[b]ecause every lay juror will be familiar with a digital clock, including the phrase 'also known as digital time' will improve a juror's ability to understand the concept of 'discrete time.'" (*Id.*, at 3-4.)

(b) Analysis

Although Defendants argue that this term should not be construed, the briefing demonstrates that the parties have a "fundamental dispute regarding the scope of a claim term,"

and the Court has a duty to resolve the dispute. *O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co.*, 521 F.3d 1351, 1362-63 (Fed. Cir. 2008).

Plaintiff cites a dictionary definition of "digital" as "[r]epresenting or operating on data or information in numerical form. A digital clock uses a series of changing digits to represent time at discrete intervals, for example, every second." (Dkt. No. 217, Ex. 7, *The American Heritage Science Dictionary* 176 (1st ed. 2005).) Plaintiff's reliance on extrinsic evidence, particularly a dictionary definition, is disfavored. *See Phillips*, 415 F.3d at 1319. Unfortunately, the term "discrete time" appears nowhere outside the claims except for one instance in the Abstract of the '162 Patent (emphasis added):

> A synchronous read channel is disclosed which samples an analog read signal from a magnetic read head positioned over a magnetic disk medium, filters the sample values according to a desired partial response, extracts timing information from the filtered sample values, and detects an estimated data sequence from the filtered sample values using a *discrete time* sequence detector. A Channel Quality circuit accumulates various signals generated by the read channel, such as sample errors, gain errors, timing errors, etc., for use in calibrating the read channel components and estimating the bit error rate.

The meaning of "discrete time" is illuminated, however, by the phrase "bit time," which appears nine times in the specification to describe the unit of time in which a bit is written to the medium or read from the medium, such as follows (emphasis added):

> It is common to use run-length-limited (RLL) encoding of the original user data bits, which are arbitrary or unconstrained, into an RLL-encoded stream of channel bits. It may be desirable that there be no less than d zeroes between ones; that is, that the media transitions be spaced by at least d+1 channel *bit times*. ('162 Patent, at 1:47-52.)
> * * *
> . . . samples are taken at roughly equal time intervals, each a single channel *bit time*. (*Id.*, at 2:17-18.)
> * * *
> The digitized read data signal DRD0 is a digitized read signal sample effectively taken near the center of a channel *bit time* (defined by the VFO frequency) . . . . (*Id.*, at 5:54-57.)
> * * *

> The output of the transition detector is a low or high level during the respective *bit times* (delayed as described in the co-pending application) depending upon whether a transition (providing a high level output) or no transition (providing a low level output) was detected. (*Id.*, at 6:24-28.)
> * * *
> [I]n general the output of the sequence detector, when used, should be more accurate in ultimately determining whether a transition occurred at a particular *bit time* . . . . (*Id.*, at 10:22-25.)
> * * *
> If the present invention is realized in an embodiment wherein digitized read data is processed a single *bit time's* worth at a time, a Viterbi detector of a conventional design may be used, or if two or more *bit time's* worth of samples are to be processed simultaneously, as in the preferred embodiment of the present invention, a conventional Viterbi detector could be modified for that purpose. (*Id.*, at 10:35-41.)
> * * *
> The d=1 constraint . . . prevent[s] magnetic transitions in two consecutive channel *bit times*. (Id., at 11:19-21.)

Although Plaintiff's reliance on a dictionary definition is disfavored, as noted above, that extrinsic evidence comports with the above-quoted usages of the similar term "bit time" in the specification and is useful to "confirm" the Court's understanding of the term. *L.B. Plastics, Inc. v. Amerimax Home Products, Inc.*, 499 F.3d 1303, 1308 (Fed. Cir. 2007). To be clear, the Court does not find that "bit time" is synonymous with "discrete time." Rather, the usages of "bit time" in the specification inform how a person of ordinary skill in the art would read the similar term "discrete time" in the claims.

In light of the intrinsic evidence, a person of ordinary skill in the art would read "discrete time" to refer to distinct units of time. Plaintiff's proposal to include the word "discrete" in the construction of "discrete time" would not adequately assist a jury in understanding the term. Plaintiff submits that the ordinary definition of "discrete" includes "distinct." (Dkt. No. 235, at 3 (citing the *New Oxford American Dictionary* 488.) Although Plaintiff opposes using the word "distinct" in the construction, a person of ordinary skill in the art reading the patent as a whole would understand "discrete time" to mean "time represented at distinct intervals."

Finally, Plaintiff's proposal to include "also known as digital time" is rejected as redundant, potentially confusing, and unsupported by the specification.

The Court hereby construes **"discrete time"** to mean **"time represented at distinct intervals."**

C. "Responsive to the Discrete Time Sample Values"

Plaintiff's Proposed Construction	**Defendants' Proposed Construction**
"responsive to the digital values representing the amplitudes of the analog read signal at the time it is sampled"	"operating in response to the digital values representing the amplitudes of the analog read signal at the time it is sampled"

This term appears in Claims 1, 5, and 13 of the '162 Patent.

Plaintiff proposed this term means "responsive to the digital values representing the amplitudes of the analog read signal at the time it is sampled." (Dkt. No. 237-1, at 2.) Defendants proposed this term means "operating in response to the digital values representing the amplitudes of the analog read signal at the time it is sampled." (*Id.*)

Defendants argued that "replacing 'responsive to' with 'operating in response to' would aid the jury's understanding of the invention." (Dkt. No. 225, at 10.)

Plaintiff replied that Defendants' proposal of "operating" adds a new limitation that "is not part of the ordinary meaning of any term in the phrase, does not clarify anything, and is inserted by Defendants only for the purpose of mischief." (Dkt. No. 235, at 4.)

In sur-reply, Defendants submitted that Plaintiff "has agreed to adopt Defendants' construction for this term." (Dkt. No. 242, at 1.)

Based on the demonstrative slides submitted by Defendants at the May 14, 2012 hearing, the parties are now in agreement that Defendants' proposed construction should be adopted. The Court therefore hereby construes **"responsive to the discrete time sample values"** to mean

"operating in response to the digital values representing the amplitudes of the analog read signal at the time it is sampled."

D. "Discrete Time Sequence Detector"

Plaintiff's Proposed Construction	**Defendants' Proposed Construction**
"sequence detector that receives input in discrete time" "Sequence detector" means "circuit that recovers sequences of bits, for example a Verterbi detector"	"a sequence detector including an add, compare, select module (ACS module) that has two or more sequence model states dynamically associate with it" No construction necessary for "sequence detector."

This term appears in Claims 1, 7, 12, and 13 of the '162 Patent.

(a) The Parties' Positions

Plaintiff proposes this term means "sequence detector that receives input in discrete time." (Dkt. No. 237-1, at 2.) The constituent term "discrete time" is discussed in Section IV., above. Plaintiff also proposes that the constituent term "sequence detector" means "circuit that recovers sequences of bits, for example a Viterbi detector." (*Id.*) Defendants propose this term means "a sequence detector including an add, compare, select module (ACS module) that has two or more sequence model states dynamically associated with it." (*Id.*) Defendants have not proposed any construction for the constituent term "sequence detector." (*Id.*)

Plaintiff argues that in the context of the patents-in-suit, "detecting" means "recovering." (Dkt. No. 217, at 15.) Plaintiff concludes that a "sequence detector" is a circuit that recovers a sequence of bits. (*Id.*) Plaintiff also argues that because the patents-in-suit discuss a Viterbi detector, it would be helpful to the jury to include in the construction that an example of a "sequence detector" is a Viterbi detector. (*Id.*, at 15-16.) Finally, Plaintiff argues that

Defendants' proposal of including an "ACS module" in the construction should be rejected as an attempt to import a limitation from a preferred embodiment. (*Id.*, at 16.)

Defendants respond that Plaintiff's proposal should be rejected as reading on the prior art discussed in the patents-in-suit. (Dkt. No. 225, at 12-13.) Defendants argue that the "discrete time sequence detector" "must relate to and reflect the properties of the uniquely modified form of Viterbi detector disclosed in the Asserted Patents" because the patents-in-suit disclose that the "basic" Viterbi detector is prior art. (*Id.*) The patentee, according to Defendants, expressly defined the "sequence detector used in the present invention" as a "uniquely modified form of Viterbi detector." (*Id.* (quoting '162 Patent at 10:53-56).) Defendants also note that the patents-in-suit incorporate by reference United States Patent No. 5,291,499 ("the '499 Patent"), which discloses a uniquely modified Viterbi detector and which was used as the basis for rejections during prosecution of the '738 Patent. (*Id.*, at 13-14.) As to the ACS module, Defendants argue that the patents-in-suit "disparaged" the use of an ACS module for each state and instead disclosed saving size and complexity by using one ACS module for multiple states. (*Id.*, at 15.) In other words, "if all ACS modules of a sequence detector were associated with only one sequence model state each, then the sequence detector would be the 'basic' prior art Viterbi detector." (*Id.*, at 16.)

Plaintiff replies that the "uniquely modified form of Viterbi detector" disclosed in the specification is merely a preferred embodiment because, for example, "the specification teaches that the claimed sequence detector may be used in an embodiment that uses a conventional Viterbi detector." (Dkt. No. 235, at 5-6.) Plaintiff also submits that the specification discloses that "in the preferred embodiment . . . an ACS module may have two or more sequence model states dynamically associated with it," not "must have." (*Id.*, at 6.)

In sur-reply, Defendants reiterate that during prosecution the patentee characterized the conventional Viterbi detector as prior art and disparaged it as being too complex and using too much hardware. (Dkt. No. 242, at 2-3.) Defendants also argue that "there is no need to separately construe the term 'sequence detector' because sequence detectors were well known in the art decades before the patents." (*Id.*, at 3.) Alternatively, Defendants re-urge that "the sequence detection described by the Asserted Patents" contemplates "looking before and after a particular bit to determine the sequence." (*Id.*)

(b) Analysis

The parties dispute whether the constituent term "sequence detector" should be construed and whether the patentee made a special, limited use of the term "sequence detector" so as to require the ACS limitation proposed by Defendants.

Plaintiff proposes a construction for the constituent term "sequence detector," but Defendants propose none. Defendants' briefing does not substantively address Plaintiff's proposed construction. (*See* Dkt. No. 225, at 11-17; *see also* Dkt. No. 242.) On balance, Plaintiff's proposed construction is helpful and appropriate except that Plaintiff's proposal to include the Viterbi detector as an example in the construction is rejected as unnecessary and potentially confusing. Also, construing the constituent term "sequence detector" separately might introduce unnecessary confusion or difficulty in applying the Court's claim construction, so the Court construes "sequence detector" as part of the entire disputed term.

As to ACS modules, only one paragraph of the patents-in-suit discusses ACS:

> In a typical Viterbi detector implemented using the ADD, COMPARE, SELECT (ACS) method, each state in the expected sample sequence model is associated with a hardware module to perform the functions of adding new branch error metrics to path error metrics, comparing path error metrics, and selecting the path having the lowest path metric. In the sequence detector used in the preferred embodiment in accordance with the co-pending application, *an ACS module may*

> *have two or more sequence model states dynamically associated with it* such that at some times, one sequence model state is associated with it, and at other times, another sequence model is associated with it. This reduces the number of ACS modules required and also reduces the size and complexity of the detector path memories which must store one path for each ACS module. Groups of sequence model states may be chosen to share an ACS module without significant loss in performance as compared to the conventional Viterbi detector. These detectors support a wide range of sample models by making the expected sample sequence of an isolated medium transition programmable through control 44. By way of specific example, the sequence detector used in the CL-SH4400 disclosed herein will support the PR4, EPR4 and EEPR4 sample models, among others. In addition, the alternating polarity of pulses is enforced, as is a minimum run length constraint of d=1.

('162 Patent, at 10:47-11:5 (emphasis added).) The patents-in-suit incorporate by reference United States Patent No. 5,291,499, which focuses on ACS modules and which discloses as follows in the first paragraph of the Brief Summary of the Invention:

> In a typical Viterbi demodulator implemented using the add, compare, select method, each state in the expected sample sequence model is associated with a hardware module to perform the functions of adding new branch error metrics to path error metrics, comparing path error metrics, and selecting the path having the lowest path error metric. In the prior art, the required number of these add, compare, select (ACS) modules is equal to the number of sequence-model states. *In this invention, an ACS module may have two or more sequence-model states dynamically associated with it*, such that at some times one sequence-model state is associated with it and at other times another sequence-model state is associated with it. The present invention reduces the number of ACS modules required and also reduces the size/complexity of the demodulator's path memories which must store one path for each ACS module. Groups of sequence-model states may be chosen to share an ACS module without significant loss in performance as compared to the original, unreduced Viterbi demodulator.

('499 Patent, at 12:54-13:11 (emphasis added).) This disclosure in the '499 Patent is deemed part of the specification of the patents-in-suit. *Telemac Cellular Corp. v. Topp Telecom, Inc.*, 247 F.3d 1316, 1329 (Fed. Cir. 2001). Defendants rely upon the following disclosure in the patents-in-suit as tying the discrete time sequence detector to the "reduced complexity sequence detector" set forth in the '499 Patent:

> *The particular sequence detector used in the present invention is a uniquely modified form of Viterbi detector which substantially preserves the full performance of the Viterbi algorithm in a substantially reduced complexity sequence detector.* The basic Viterbi algorithm is described in the book "Fast Algorithms for Digital Signal Processing" by Richard E. Blahut, 1985, pages 387-399. In accordance with the Viterbi algorithm, a Viterbi detector does not attempt to decide whether a medium transition has occurred immediately upon receipt of the read sample or samples that correspond to that transition. Rather, as samples are taken from the read signal, the Viterbi detector keeps a running tally of the error between the actual sample sequence and the sample sequence that would be expected if the medium had been written with a particular sequence of transitions. Such an error tally is simultaneously kept for several possible transition sequences. As more samples are taken, less likely choices for transition sequences are pruned from consideration.

('162 Patent, at 9:61-10:12 (emphasis added).)

The parties' dispute centers on the meaning of the word "may" as it appears in the patents-in-suit: "an ACS module *may* have two or more sequence model states dynamically associated with it." ('162 Patent, at 10:55-56 (emphasis added).) Plaintiff argues that this "may" is permissive and not limiting. Defendants argue:

> The use of "may" in this sentence refers to any one ACS module, not the collective group of ACS modules. The statement does not in any way change the inventors' clear expression that there must be at least one ACS module that complies with "the present invention."

(Dkt. No. 225, at 16.) Defendants also cite a similar statement in the '499 Patent. (*Id.*, at 16 n.5.)

On one hand, the patents-in-suit, as well as the '499 Patent incorporated by reference therein, disparage the "typical" Viterbi detector in which an ACS module has only one state associated with it. Efforts to disparage and distinguish the prior art can sometimes justify finding a disclaimer. *Revolution Eyewear, Inc. v. Aspex Eyewear, Inc.*, 563 F.3d 1358, 1368 (Fed. Cir. 2009) ("[A]ny limitation based on [specification] disclaimer must be shown with reasonable clarity and deliberateness."); *see also Chicago Bd. Options Exch., Inc. v. Int'l Sec. Exch., LLC*,

Nos. 2011-1267, -1298, 2012 WL 1570989, at *9 (Fed. Cir. May 7, 2012) (regarding trading systems, "the specification goes well beyond expressing the patentee's preference for a fully automated exchange over a manual or a partially automated one, and its repeated derogatory statements about the latter reasonably may be viewed as a disavowal of that subject matter from the scope of the Patent's claims") (citing *Honeywell Int'l, Inc. v. ITT Indus., Inc.*, 452 F.3d 1312, 1319 (Fed. Cir. 2006)). The patentee also specified that "the particular sequence detector used in *the present invention* is a uniquely modified form of Viterbi detector," as quoted above, which weighs in favor of a limited construction. *Verizon Service Corp. v. Vonage Holdings Corp.*, 503 F.3d 1295, 1308 (Fed. Cir. 2007) ("When a patent thus describes the features of the 'present invention' as a whole, this description limits the scope of the invention.")

On the other hand, such a finding of specification disclaimer must be based upon "expressions of manifest exclusion or restriction, representing a clear disavowal of claim scope." *Retractable Techs., Inc. v. Becton, Dickenson & Co.*, 653 F.3d 1296, 1306 (Fed. Cir. 2011) (quoting *Epistar Corp. v ITC*, 566 F.3d 1321, 1336 (Fed. Cir. 2009)); *August Tech. Corp. v. Camtek, Ltd.*, 655 F.3d 1278, 1286 (Fed. Cir. 2011) ("Absent a clear disavowal or contrary definition in the specification or the prosecution history, the patentee is entitled to the full scope of its claim language.") (citation and internal quotation marks omitted). Further, "discussion of the shortcomings of certain techniques is not a disavowal of the use of those techniques in a manner consistent with the claimed invention." *Epistar*, 566 F.3d at 1336.

Thus, although the patents-in-suit criticize conventional sequence detectors for being more complex than the sequence detector disclosed in the '499 Patent, such "criticism does not rise to the level of a disavowal." *Id.*

Alternatively, even assuming for the sake of argument that the language cited by Defendants can be read as a "disavowal," the patentee made no "clear" disavowal because the patentee disclosed that in "the present invention," "a Viterbi detector of a conventional design may be used." ('162 Patent, at 10:35-46.) At the May 14, 2012 hearing, Defendants criticized Plaintiff's reliance on this disclosure as pertaining to a "single bit time" embodiment that is not covered by the claims. In particular, Defendants argued that because a "single bit time" embodiment determines the value of a bit at the time the bit is read rather than at a later time after subsequent bits have been detected, that embodiment is not covered by the claims. On balance, the Court believes that Defendants misread the disclosure, which refers to sequence detection that processes one bit at a time but that, like all Viterbi detectors, does not decide the value of a particular bit until subsequent bits have been detected.

In sum, Defendants have failed to show any clear disavowal that would justify adopting Defendants' proposed construction requiring "an add, compare, select module (ACS module) that has two or more sequence model states dynamically associated with it."

Finally, the word "recovers" proposed by Plaintiff would be helpful to the jury in understanding the disputed term, and the technical dictionary definition cited by Plaintiff "confirm[s]" that "recover" is an appropriate word to use in the Court's construction. *L.B. Plastics*, 499 F.3d at 1308; (Dkt. No. 217, Ex. 9, *McGraw Hill Dictionary of Scientific and Technical Terms*, 571, 582 (6th ed. 2003) ("Detect" defined as "*See* demodulate; "Demodulate" defined as "To recover the modulating wave from a modulated carrier. Also known as decode; detect"). At the May 14, 2012 hearing, Defendants challenged the dates of publication of Plaintiff's dictionaries as being too long after the priority date of the patents-in-suit, but Defendants have not submitted evidence of any relevant change in definition.

The Court therefore hereby construes **"discrete time sequence detector"** to mean **"circuit that uses a sequence model to recover sequences of bits based on input received in discrete time."**

E. "Trellis Type Sequence Detector"

Plaintiff's Proposed Construction	**Defendants' Proposed Construction**
No construction necessary apart from the construction of "sequence detector"	"a trellis sequence detector including an add, compare, select module (ACS module) that has two or more sequence model states dynamically associated with it."

This term appears in Claims 1 and 6 of the '738 Patent.

Plaintiff proposes that this term requires no construction apart from the construction of the constituent term "sequence detector," which is discussed in Section VII., above. (Dkt. No. 237-1, at 13.) Defendants propose that this term means "a trellis sequence detector including an add, compare, select module (ACS module) that has two or more sequence model states dynamically associated with it," which is similar to the construction Defendants proposed as to the term "discrete time sequence detector," discussed in Section VII., above. (*Id.*)

Neither party proposes any construction for the constituent term "trellis" or "trellis type." (*See* Dkt. No. 217, at 17-18; Dkt. No. 225 at 11-17; Dkt. No. 235, at 7.) The parties rely on their arguments as to the related term "discrete time sequence detector" (*see id.*), discussed in Section VII., above, so the Court conducts no separate analysis as to this term.

The Court accordingly hereby construes **"trellis type sequence detector"** to mean **"circuit that uses a trellis-type sequence model to recover sequences of bits based on input received in discrete time."**

F. "State Transition Diagram"

Plaintiff's Proposed Construction	Defendants' Proposed Construction
"diagram that indicates the possible states and the transitions between the possible states"	"a diagram illustrating the transitions between possible states, having the states and properties of the diagram illustrated in Fig. 7""

This term appears in Claims 1 and 6 of the '738 Patent.

(a) The Parties' Positions

Plaintiff proposes this term means "diagram that indicates the possible states and the transitions between the possible states." (Dkt. No. 237-1, at 14.) Defendants propose this term means "a diagram illustrating the transitions between possible states, having the states and properties of the diagram illustrated in Fig. 7." (*Id.*)

Plaintiff argues that its proposed construction is the ordinary meaning, that the specification contains no explicit limitation or disavowal, and that the figure cited by Defendants is only an example. (Dkt. No. 217, at 20.)

Defendants respond that the specification identifies Figure 7 as "a state transition diagram of the sequence detector employed in the synchronous read channel or [*sic*, of] the present invention." (Dkt. No. 225, at 19.) Defendants conclude that the patentee thereby restricted the scope of the claims to the disclosure in Figure 7, which is further supported by disclosure that the "d=1" constraint for "RLL" encoding "is an important constraint in the present invention." (*Id.* (quoting '738 Patent, at 11:11-12).) RLL encoding is discussed in Sections I. and IV., above. Defendants further note that United States Patent No. 5,291,499, which the '738 Patent incorporates by reference, "show[s] that different state transition diagrams embody different kinds of information and have different mathematical implications." (Dkt. No. 225, at 20.)

Defendants urge that Plaintiff's proposed construction is overbroad because it would cover the state transition diagrams in the '499 Patent, which "do *not* have the same RLL constraints and therefore would not fit the requirements of the specification of the '738 Patent." (*Id.*)

Plaintiff replies that although Defendants assert that the patentee limited the term at issue to Figure 7 of the '738 Patent, "Defendants provide zero support for that assertion and it is simply false." (Dkt. No. 235, at 7-8.) Plaintiff also notes that United States Patent No. 5,291,499, which the patents-in-suit incorporate by reference, includes state transition diagrams that differ from Figure 7 of the '738 Patent. (*Id.*, at 8.)

In sur-reply, Defendants argue that they are not attempting to limit the construction to the diagram in Figure 7 but rather are arguing that "the state transition diagram must have the states and properties of Figure 7." (Dkt. No. 242, at 4).

(b) Analysis

Claims 1 and 6 of the '738 Patent recite a "state transition diagram" (emphasis added):

> 1. A synchronous read channel for reading data recorded on a magnetic disk storage medium by detecting binary data from a sequence of discrete time sample values generated by sampling pulses in an analog read signal from a magnetic read head positioned over the magnetic disk storage medium, comprising:
>
> (a) a sampling device for sampling the analog read signal to generate the discrete time time sample values;
>
> (b) a discrete time filter for filtering the discrete time sample values according to a partial response;
>
> (c) discrete time timing recovery for extracting timing information from the discrete time sample values; and
>
> (d) a trellis type sequence detector for detecting the binary data from the sample values, comprising programmable detector levels associated with a *state transition diagram* for matching the sequence detector to the partial response.

> 6. A synchronous read channel for reading data recorded on a magnetic disk storage medium by detecting binary data from a sequence of discrete time sample values generated by sampling pulses in an analog read signal from a magnetic read head positioned over the magnetic disk storage medium, comprising:
>
> > (a) a sampling device for sampling the analog read signal to generate the discrete time time sample values;
> >
> > (b) a discrete time filter for filtering the discrete time sample values according to a partial response;
> >
> > (c) a trellis type sequence detector for detecting the binary data from the sample values, comprising programmable detector levels associated with a *state transition diagram* for matching the sequence detector to the partial response.

The parties dispute whether a "state transition diagram" includes the possible states and whether the "state transition diagram" must include the states and properties of the diagram illustrated in Figure 7 of the '738 Patent. As to Figure 7, Defendants rely on the Brief Description of the Drawings, as well as the discussion of Figure 7 in the Detailed Description of the Invention:

> FIG. 7 is a state transition diagram of the sequence detector employed in the synchronous read channel or [*sic*, of] the present invention.
> * * *
> The state machine model for the partial response sequence detector 40 is shown in FIG. 7. Note that the model embodies several kinds of information. First, the isolated pulse sample values a, b, 1, and c are included. Second, the alternating polarity of pulses constraint is enforced. Third, the minimum run-length constraint of d=1 is enforced.

('738 Patent, at 5:3-5 & 12:8-13.) "[A]ny limitation based on [specification] disclaimer must be shown with reasonable clarity and deliberateness." *Revolution Eyewear*, 563 F.3d at 1368; *see Chicago Bd.*, 2012 WL 1570989, at *8-*9. On balance, the Court concludes that no clear and deliberate disclaimer has been shown. In particular, as Plaintiff emphasized at the May 14, 2012 hearing, the above-quoted Brief Description of the Drawings states "FIG. 7 is *a* state transition diagram," not "*the* state transition diagram." Further, whereas Figure 7 represents one type of

partial response channel, the specification discloses that "the present invention supports a broad class of partial response channels, including but not limited to PR4 (1,7), EPR4 (1,7) and EEPR4 (1,7)." ('738 Patent, at 13:55-60; *see id.*, at 11:7-8.)

At the May 14, 2012 hearing, Defendants urged that when the patentee added Figure 7 to the application that led to the '738 Patent, the patentee stated that Figure 7 "shows the state machine model for the partial response sequence detector *of the present invention*." (3/19/1997 Request for Drawing Change, at 1 (emphasis added).) The specification and the claims should be afforded more weight than the prosecution history, and both the specification and the claims better comport with a reading of "state transition diagram" that is not constrained to the specific model depicted in Figure 7. *See Phillips*, 415 F.3d at 1317.

As to the "possible states" language proposed by Plaintiff, Defendants present no counter-argument, and Plaintiff's proposal comports with the disclosure of the patents-in-suit and the '499 Patent incorporated by reference therein, as well as the treatise cited by Plaintiff:

> The maximum likelihood detection can be best understood based on the concept of *state diagram*, which describes all the possible states of the magnetic recording system and the transitions between these states. The state diagram consists of two distinct parts: *states* and *transitions*.

(Dkt. No. 246, Ex. 19, Shan X. Wang & Alexander M. Taratorin, *Magnetic Information Storage Technology* 393 (1999).)

The Court hereby construes **"state transition diagram"** to mean **"diagram that indicates the possible states and the transitions between possible states."**

G. "Channel Quality Circuit"

Plaintiff's Proposed Construction	**Defendants' Proposed Construction**
"circuit that measures a quality of the channel by gathering performance data on channel components"	"circuit that calibrates detector levels based on the quality of a signal"

This term appears in Claims 1-8, 10, 12, 13, and 15 of the '162 Patent.

(a) The Parties' Positions

Plaintiff proposes this term means "circuit that measures a quality of the channel by gathering performance data on channel components." (Dkt. No. 237-1, at 3.) Defendants propose this term means "circuit that calibrates detector levels based on the quality of a signal." (*Id.*)

Plaintiff cites disclosure in the specification that "the present invention includes a channel quality circuit 46 for measuring the quality of the read channel." (Dkt. No. 217, at 22 (quoting '162 Patent at 9:12-19 (emphasis omitted).) Plaintiff also argues that the prosecution history limits the term to Plaintiff's proposal because the patentee distinguished the "multi-mode timing loop" of the "Johnson" prior art reference (United States Patent No. 5,258,933) by arguing that "the claimed channel quality circuit [in the '162 patent] is used to gather performance data on the channel components." (*Id.*, at 23 (quoting Ex. 4, Response to First Office Action, at LC000144-145) (emphasis omitted).) Further, Plaintiff cites disclosure in the Abstract of the '162 Patent that "[a] Channel Quality circuit accumulates various signals generated by the read channel, such as sample errors, gain errors, timing errors, etc., for use in calibrating the read channel components and estimating the bit error rate." (Dkt. No. 217, at 23.) Finally, Plaintiff argues that Defendants' proposed construction should be rejected because "[i]n the preferred embodiment, the microcontroller, not the 'channel quality circuit,' calibrates . . . detector levels" and because "where a function is mentioned in connection with a claim element, that function cannot be read into the claim element." (*Id.*, at 24-25.)

Defendants respond by emphasizing the disclosure that "'[u]sing the channel quality circuit,' a microcontroller can 'adapt the detector levels . . . to find the best detector sample level sets (those which produce the minimum error rate) for each disk drive, head, and zone.'" (Dkt. No. 225, at 21 (quoting '162 Patent at 16:58-63).) Defendants cite documentation for the Cirrus Logic chip CL-SH4400 (disclosed by the patents-in-suit as a commercial embodiment), which "repeatedly describes that the quality channel circuit is used for calibration." (Dkt. No. 225, at 21-22 (citing Ex. D).) Defendants also urge that Plaintiff's proposal encompasses functions disclosed as prior art in the Background of the Invention. (Dkt. No. 225, at 22.) Further, Defendants submit that the patentee overcame prior art rejections during prosecution by repeatedly explaining that the quality circuit is used for calibrating the read channel parameters. (*Id.*, at 22-23 (discussing Ex. C, 10/15/1998 Response to Office Action, at 5).) Finally, Defendants note that surrounding claim language in Claims 1 and 13, from which all of the asserted claims depend, explains that the "channel quality circuit" is "for calibrating the synchronous read channel." (Dkt. No. 225, at 23 & 24.) As to any claim differentiation argument based on Claims 1 and 12, Defendants respond that "[d]ependent claim 12 is narrower because it requires calibration specifically of the samples within a signal model." (*Id.*, at 25.) Defendants conclude that their proposal of the word "calibrates" best comports with both the intrinsic and extrinsic evidence. (Dkt. No. 225, at 21.)

Plaintiff replies that "[t]he parties agree that the quality channel circuit is used in the process of calibration." (Dkt. No. 235, at 10.) Plaintiff argues that the quality channel circuit need not always be used to calibrate but instead "Plaintiff contends the quality channel circuit always measures and may (or may not) calibrate." (*Id.*) Plaintiff submits that "the circuit enables calibration by measuring performance data. That data is then used for calibration, which

may be done by the quality channel circuit or by another component." (*Id.*, at 11.) As to the prosecution history, Plaintiff argues that "the patentee [wa]s distinguishing a prior art circuit that measured one component to adjust one parameter, as contrasted with the quality channel circuit that measures 'components' (plural) to adjust 'parameters' (plural)." (*Id.*; *see id.* at 12-13.) Plaintiff concludes that this was "a clear and unambiguous disavowal" that "must be reflected in the claim construction." (*Id.*, at 13.) Plaintiff argues that the prosecution history cited by Defendants pertains to a different aspect of Johnson, a "programmable coefficient," which Plaintiff argued was never calibrated in Johnson. (*Id.*) Plaintiff submits that the patentee distinguished Johnson based on the "for calibrating" language of the claims, *not* the "channel quality circuit itself." (*Id.*) Finally, Plaintiff urges that limiting the claims to calibration of "detector levels," as Defendants propose, would improperly import a limitation from a preferred embodiment. (*Id.*) In support, Plaintiff cites disclosure in the specification of, in Plaintiff's words, "five categories of parameters other than detector levels that may be adjusted using data from the channel quality circuit." (*Id.* (emphasis omitted).)

In sur-reply, Defendants acknowledge that "[t]he idea of measurement is inherent in Defendants' construction," but Defendants argue that "the inventors specifically cited calibration as the inventive step over the Johnson reference." (Dkt. No. 242, at 5-6 (footnote omitted).) Defendants reiterate that Plaintiff's proposal that the channel quality circuit merely "measures for calibrating," as Defendants put it, is "unsupported and is inconsistent with the intrinsic evidence, which requires that the channel quality circuit both measures and calibrates." (*Id.*, at 6.)

(b) Analysis

Although Defendants stated at the May 14, 2012 hearing that they would prefer to leave "measuring" out of the construction of "channel quality circuit," the parties essentially agree that the "channel quality circuit" takes measurements regarding the quality of the read channel. (*See* Dkt. No. 225, at 22.) Such a reading is supported by the specification. (*See, e.g.,* '162 Patent, at Abstract & Summary of the Invention, 4:33-38.) The patentee's statements in the prosecution history lend additional support:

> Thus, the claimed channel quality circuit is used to gather performance data on the channel components and then to adjust or calibrate the channel component parameters.

(Dkt. No. 225, Ex. C, 10/15/1998 Response to First Office Action, at 5.) Thus, the Court's construction of "channel quality circuit" should include the concept of "measuring."

The parties principal dispute, then, is whether calibration must be done by the "channel quality circuit" or may be done by some other component.

Plaintiff has emphasized disclosure in the specification that calibration may be performed by a microcontroller rather than by the "channel quality circuit':

> In addition to the various retry strategies described above, the nature and quality of the channel comprising the head/disk interface, preamp, tunable active filter, ADC, and digital equalizer can be measured with the Channel Quality circuit 46, which is provided so that the variable channel parameters (e.g., analog and digital equalization parameters, gain and timing set points, gain control and timing recovery coefficients, and detector levels) may be adjusted to provide the lowest possible error rate. The Channel Quality circuit 46 is a very powerful and flexible measurement tool, providing numerous options to facilitate different kinds of measurements of the channel. By selecting appropriate options, it is possible to measure mean squared error (MSE), determine the equalized pulse shape, characterize asymmetries between positive and negative pulses, perform margin testing, scan the media for defects, measure DC offset, and measure the performance of the Gain Control and Timing Recovery loops and the zero phase restart. Furthermore, using the Channel Quality circuit 46, a procedure is provided *whereby the microcontroller may adapt the detector levels*. *The intent of this*

> *feature is to allow the microcontroller to find the best detector sample level sets* (those which produce the minimum error rate) for each disk drive, head, and zone.

('162 Patent, at 13:41-63 (emphasis added).)

On the one hand, a construction that excludes a preferred embodiment is "rarely, if ever, correct." *Pfizer, Inc. v. Teva Pharms., USA, Inc.*, 429 F.3d 1364, 1374 (Fed. Cir. 2005) (citation and internal quotation marks omitted).

On the other hand, although Plaintiff argues that the presence of "for calibrating" in the claims demands that "calibrating" is not part of the "channel quality circuit," a person of ordinary skill in the art would read the claims as teaching that the "channel quality circuit" is "for calibrating." (*See, e.g.*, '162 Patent, at Claims 1 & 13.) Such a reading also comports with the patentee's statement during prosecution that "the claimed channel quality circuit is used to gather performance data on the channel components *and then to adjust or calibrate the channel component parameters.*" (Dkt. No. 225, Ex. C, 10/15/1998 Response to First Office Action, at 5.) Finally, as Defendants submitted during the May 14, 2012 hearing, the Cirrus Logic document attached as Appendix 1 to the '738 Patent identifies as a "Feature[]" the "Channel quality circuitry for error rate testing and filter/detector calibration." (Dkt. No. 225, Ex. D, at 1.)

As to whether "detector levels" must be calibrated, as Defendants propose, Plaintiff cites a list of examples from the specification:

> Channel Quality circuit . . . is provided so that the variable channel parameters (e.g., analog and digital equalization parameters, gain and timing set points, gain control and timing recovery coefficients, and detector levels) may be adjusted.

('162 Patent, at 13:44-48.) During the May 14, 2012 hearing, Defendants emphasized prosecution history in which the patentee distinguished the Johnson prior art reference by purportedly disclaiming calibration of the "discrete-time equalizer," "timing recovery circuit for

synchronizing," and "gain control circuit." (*See* Dkt. No. 225, Ex. C, 10/15/1998 Response to First Office Action, at 4, 8 & 9.)

On balance, however, neither the specification nor the prosecution history contain any "clear" disavowal that would require the "channel quality circuit" to calibrate detector levels. *Retractable Techs.*, 653 F.3d at 1306; *Omega Eng'g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1325-26 (Fed. Cir. 2003).

The Court therefore hereby construes **"channel quality circuit"** to mean **"circuit that measures a quality of the channel by gathering performance data on channel components and that calibrates channel parameters based on the quality of a signal."**

H. "Calibrating the Synchronous Read Channel"

Plaintiff's Proposed Construction	**Defendants' Proposed Construction**
"adapting or adjusting parameters of the synchronous read channel"	"adjusting variable detector levels of the discrete time sequence detector of the synchronous read channel during normal operation to generate the lowest possible error rate"

This term appears in Claims 1, 2, 11, and 13 of the '162 Patent.

(a) The Parties' Positions

Plaintiff proposes this term means "adapting or adjusting parameters of the synchronous read channel." (Dkt. No. 237-1, at 3.) Defendants propose this term means "adjusting variable detector levels of the discrete time sequence detector of the synchronous read channel during normal operation to generate the lowest possible error rate." (*Id.*)

Plaintiff submits that during prosecution, in response to a rejection based on the "Johnson" prior art reference (also discussed in Section XI., above), the patentee explained that "the claimed channel quality circuit is used to gather performance data on the channel

components and then to adjust or calibrate the channel component parameters." (Dkt. No. 217, at 26 (quoting Ex. 4, Response to First Office Action, at LC000145).) The patentee argued, according to Plaintiff, that whereas "the multi-mode timing loop in Johnson was used to adjust only a single parameter," "the channel quality circuit in the '162 Patent is used . . . 'to adjust or calibrate the channel component parameters' (plural)." (Dkt. No. 217, at 26.) Plaintiff cites several uses of "adapt" and "adjusted" in the written description. (*Id.*, at 26-27.) Plaintiff also argues that Defendants' proposed construction improperly limits the term to calibrating "detector levels," which Plaintiff submits is only a limitation of Claim 12 and not any other claim. (*Id.*, at 28.) Plaintiff also notes that the word "calibrating" appears only once in the written description and is not given any special meaning. (*Id.*, at 29.) Plaintiff further argues that because "[t]he concept of generating the lowest possible error rate is not in the ordinary meaning of 'calibrating,'" Defendants' proposal in that regard should be rejected. (*Id.*) Finally, Plaintiff cites a dictionary definition of "calibrating" as "[t]o make corrections in; adjust." (*Id.* (quoting Ex. 6, *The American Heritage Dictionary* 264 (4th ed. 2000)).)

Defendants respond by incorporating their argument on "channel quality circuit" as to Defendants' proposed requirement that what is calibrated are "detector levels." (Dkt. No. 225, at 26.) Defendants argue that during prosecution the patentee limited the claim scope to require that calibration occurs during normal operation. (*Id.*, at 27.) Defendants also cite disclosure in the specification that "[i]n addition to the various retry strategies discussed above . . . the Channel Quality circuit 46 . . . is provided so that the variable channel parameters . . . may be adjusted to provide the lowest possible error rate." (*Id.* (quoting '162 Patent, at 13:41-49).) As to Plaintiff's argument that Johnson disclosed adjusting only a single parameter rather than multiple parameters, Defendants argue that the patentee "overcame Johnson based on the manner

in which Johnson set the value of the parameter . . ., not based on number of parameters . . . ." (Dkt. No. 225, at 28.)

Plaintiff replies by reiterating its claim differentiation argument as to Claim 12, which recites "calibrating the detector levels," and by re-urging that "to generate the lowest possible error rate" "does not represent the ordinary meaning of any of the concepts in the claim language." (Dkt. No. 235, at 14.)

In sur-reply, Defendants argue that "[i]f the term 'calibrating the synchronous read channel' were read to cover adjusting any parameter, then the claims would cover prior art and would be invalid." (Dkt. No. 242, at 8.) Defendants also emphasize "the main problem that the claimed calibration (and, in fact, the patent itself), seeks to solve," to wit, the "variation in the physical spacing of transitions between the inside and outside diameters of each zone resulting in a variation in pulse shape." (*Id.*; '162 Patent, at 3:64-67.) Defendants conclude that "[c]alibrating the synchronous read channels must mean adapting the detector levels to generate the lowest error rate notwithstanding the variation in physical spacing in the inside and outside diameters of the magnetic disk because it is the sequence detector that reads the information that the read channel seeks to output correctly." (Dkt. No. 242, at 8.) As to Plaintiff's claim differentiation argument regarding Claim 12, Defendants reply that the "detector levels" in Defendants' proposed construction refer to "signal models, *e.g.*, PR4, EPR4, EEPR," whereas the "detector sample level" in Claim 12 "refers to sample sequences that make up the signal models." (*Id.*)

(b) Analysis

The parties dispute: (1) whether what is calibrated must be detector levels; (2) whether calibration must occur during normal operation; and (3) whether calibration is done "to generate the lowest possible error rate."

Defendants' proposed "detector levels" limitation has been rejected by the Court in Section XI., above. In short, the patentee made no "clear and unmistakable" disclaimer as to detector levels because detector levels are disclosed as one of several types of parameters that may be calibrated. *Omega Eng'g*, 334 F.3d at 1324.

As to Defendants' proposed "during normal operation" limitation, Defendants rely on the following prosecution history:

> Johnson does not disclose a channel quality circuit for calibrating the read channel . . . However, Johnson does not disclose how the optimum value for the parameter α is determined for a particular zone. The optimum settings could be determined during manufacturing using external test and measurement equipment, stored in the 'register file 804,' and then used to initialize the parameter α during normal operation.

(Dkt. No. 225, Ex. C, 10/15/1998 Response to First Office Action, at 4-5.) Since, in the Court's view, the patentee made no "clear and unmistakable" statement that calibration must be performed "during normal operation" and Defendants' proposal in that regard is rejected. *Omega Eng'g*, 334 F.3d at 1324.

As to Defendants' proposal of "to generate the lowest possible error rate," the specification discloses that "[i]n addition to the various retry strategies described above . . . the Channel Quality circuit 46 . . . is provided so that the variable channel parameters . . . may be adjusted to provide the lowest possible error rate." (Dkt. No. 225, at 27 (quoting '162 Patent, at 13:41-49).) On balance, this disclosure reflects a desired objective of the preferred embodiment,

and no clear and deliberate disclaimer is evident. *Revolution Eyewear*, 563 F.3d at 1368. Defendants' proposal in this regard is therefore rejected.

As to Plaintiff's proposal of the phrase "adapting or adjusting," Defendants' proposed construction uses "adjusting," and the word "adapting" is supported by the specification (emphasis added):

> "using the Channel Quality circuit 46, a procedure is provided whereby the microcontroller may *adapt* the detector levels" ('162 Patent, at 13:58-60.)
> * * *
> "*adapt* the channel parameters" ('162 Patent, at 14:19 & 14:27.)

The word "adapting" should be included in the Court's construction, and the Court views its inclusion as helpful to the jury in understanding this claim term.

The Court therefore hereby construes **"calibrating the synchronous read channel"** to mean **"adapting or adjusting parameters of the synchronous read channel."**

I. "a," "an," and "the"

Plaintiff's Proposed Construction	**Defendants' Proposed Construction**
"one or more"	No construction necessary

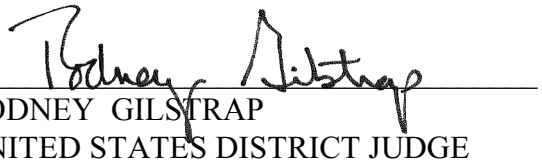
These terms are disputed in all of the independent claims of the patents-in-suit. (*See* Dkt. No. 217, at 30.) Plaintiff proposes that these terms mean "one or more," in accordance with the general "rule" noted in *Baldwin Graphic Systems, Inc. v. Siebert, Inc.*, 512 F.3d 1338, 1342-43 (Fed. Cir. 2008). (Dkt. No. 237-1, at 1.) Defendants agree with the general principle but argue that "[t]he Court should not construe all of the indefinite articles 'a' and 'an' in a vacuum, without reference to any of the nouns to which each particular article pertains." (Dkt. No. 225, at 30.) Defendants urge that the Court should consider the claims, the specification, and the prosecution history as to each instance. (*Id.*) Plaintiff replied that "Defendants now agreed [*sic*]

with Plaintiffs' proposed construction" (Dkt. No. 235, at 15), but at the May 14, 2012 hearing, the parties continued to dispute whether these terms should be construed. The Court is persuaded by Defendants position and declines to construe "a," "an," and "the."

CONCLUSION

The Court adopts the constructions set forth in this opinion for the disputed terms of the patent-in-suit. The parties are ordered that they may not refer, directly or indirectly, to each other's claim construction positions in the presence of the jury. Likewise, the parties are ordered to refrain from mentioning any portion of this opinion, other than the actual definitions adopted by the Court, in the presence of the jury. Any reference to claim construction proceedings is limited to informing the jury of the definitions adopted by the Court.

So ORDERED and SIGNED this 6th day of August, 2012.



RODNEY GILSTRAP
UNITED STATES DISTRICT JUDGE