

**IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION**

HITACHI CONSUMER ELECTRONICS	§	
CO. LTD, et al.	§	
<i>Plaintiffs,</i>	§	
	§	
v.	§	CASE NO. 2:10-CV-260-JRG
	§	
TOP VICTORY ELECTRONICS	§	
(TAIWAN) CO., LTD, et al.,	§	
<i>Defendants.</i>	§	

MEMORANDUM OPINION AND ORDER

Before the Court are Plaintiffs Hitachi Consumer Electronics Co., Ltd., and Hitachi Advanced Digital, Inc.’s (collectively, “Plaintiff’s” or “Hitachi’s”) Opening Brief in Support of Plaintiff’s Claim Constructions (Dkt. No. 137), and exhibits thereto (Dkt. Nos. 138-140), regarding patents asserted by Hitachi. Also before the Court are Defendants Top Victory Electronics (Taiwan) Co., Ltd., TPV International (USA), Inc., Envision Peripherals, Inc., Top Victory Electronics (Fujian) Co., Ltd., TPV Electronics (Fujian) Co., Ltd., TPV Technology, Ltd., and VIZIO, Inc.’s (collectively, “Defendants”) Responsive Claim Construction Brief (Dkt. No. 145) and exhibits thereto (Dkt. No. 147). Further before the Court is Hitachi’s Reply Brief in Support of Plaintiff’s Proposed Constructions (Dkt. No. 148).

Before the Court is Defendant/Counterclaim-Plaintiff VIZIO, Inc.’s (“VIZIO’s”) Opening Claim Construction Brief (Dkt. No. 142) regarding patents asserted by VIZIO. Also before the Court are Hitachi’s Responsive Claim Construction Brief for VIZIO Patents (Dkt. No. 143) and VIZIO’s Reply Claim Construction Brief (Dkt. No. 149).

The Court held a claim construction hearing on October 23, 2012.

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I. BACKGROUND

Hitachi brings suit alleging infringement of the following United States Patents

(collectively, “the Hitachi patents”):

5,502,497 (“the ‘497 Patent”)
5,534,934 (“the ‘934 Patent”)
6,037,995 (“the ‘995 Patent”)
6,144,412 (“the ‘412 Patent”)
6,388,713 (“the ‘713 Patent”)
6,549,243 (“the ‘243 Patent”)
7,012,769 (“the ‘769 Patent”)
7,286,310 (“the ‘310 Patent”)
7,889,281 (“the ‘281 Patent”)
8,009,375 (“the ‘375 Patent”)

(Dkt. No. 150, P.R. 4-5(d) Joint Submission, at 2.)

Defendant VIZIO, Inc. (“VIZIO”) has counterclaimed, alleging infringement by Hitachi of the following United States Patents (collectively, “the VIZIO patents”):

5,233,629 (“the ‘629 Patent”)
5,396,518 (“the ‘518 Patent”)
5,511,082 (“the ‘082 Patent”)
5,511,096 (“the ‘096 Patent”)
5,621,761 (“the ‘761 Patent”)
5,703,887 (“the ‘887 Patent”)
5,745,522 (“the ‘522 Patent”)

(*Id.*; see Dkt. No. 108, 6/22/2012 VIZIO Inc.’s Answer to First Amended Complaint and Counterclaims, at ¶¶ 124-186.)

A. Technical Background Regarding Over-the-Air Television and “ATSC”

The Hitachi patents relate to the ATSC standard for high definition digital television (“HDTV”). “ATSC” is an abbreviation for the Advanced Televisions Standards Committee and refers to a standard developed by a group of television manufacturers and researchers. The

ATSC standard is sometimes referred to as a “terrestrial,” “earth-based,” or “over-the-air” television standard, as contrasted with cable television or satellite television.

Traditional analog television standards, such as the “NTSC” standard previously used in North America, use an analog information signal to modify a “carrier wave.” Modifying a carrier wave so as to convey information is a process known as “modulation.” The modulated carrier wave is then received by a television and used to reproduce the audio and video.

In the ATSC standard, by contrast, a digital signal is used to represent the audio and video. Even though this signal is digital, an analog carrier wave must be used to carry the signal over the air. The digital signal is therefore used to modulate the analog carrier wave.

A carrier wave is a waveform, such as a sinusoidal wave, that propagates through a medium and that carries information. A waveform is typically graphed as a series of “peaks” and “valleys” in amplitude along the vertical axis with time along the horizontal axis. The properties of the carrier wave that can be modulated may include frequency, amplitude, and phase. Frequency is typically expressed as the number of cycles per second, known as hertz. NTSC or ATSC television signals, for example, are in the range of megahertz (“MHz”), where one MHz is equal to one million hertz, that is, one million cycles per second. Amplitude refers to the strength of the wave, which may be represented in volts. Phase can refer to the position of the wave with respect to time. For example, phase can be altered by making peaks occur sooner or later with respect to some reference time.

Modulation techniques can include amplitude shift keying (“ASK”), frequency shift keying (“FSK”), and phase shift keying (“PSK”). These techniques modify the amplitude, frequency, and phase of the carrier wave, respectively, in order to represent data, such as binary

digital data. For example in an amplitude shift keying technique, a binary “0” can be represented by reducing the amplitude of the carrier wave to a specified lower amplitude, and a binary “1” can be represented by increasing the amplitude of the carrier wave to a specified higher amplitude. As another example, a phase shift keying technique can represent a binary “1” by maintaining the phase of the carrier wave at the so-called “reference” phase and can represent a binary “0” by shifting the phase of the carrier wave 180° from the reference phase. With such modulation, the portions of the carrier wave that represent binary “0s” appear to be “upside down” when compared with the portions of the carrier wave that represent binary “1s.”

The modulated carrier wave is received by a receiver (either within the television itself or within a separate “set top box”), which then detects the modulation of the carrier wave so as to reproduce the information signal. That information signal is then converted back into audio and video signals and any other associated data.

In addition to audio and video, television signals typically include control data and other program-related data. Control data can include information used to assist in decoding the signal. Other program-related data can include television program title, start time, end time, and other similar information relating to the content of the program.

In the ATSC standard, audio data, video data, other program-related data, and control data are multiplexed to create “transport packets” that will be transmitted as a television signal. Multiplexing is a process whereby multiple independent streams of data are combined into a single stream. Each transport packet includes a “header,” which identifies the content of the packet, and a “payload,” which contains the actual audio, video, or other data. The series of transport packets is sometimes referred to as the “transport stream.”

The transport stream is then “error-coded” by a coder using two layers of coding, namely Reed Solomon coding and Trellis coding. After coding, the data is modulated onto a carrier wave and broadcast over the air. Reception then goes through these steps in reverse to recover the audio data, video data, other program-related data, and control data.

“Scanning” is another part of defining a television signal. In the NTSC standard for standard definition television, for example, the 525 lines of image data are “interlaced,” meaning that each image “field” contains only half of the lines. One field contains all of the odd-numbered lines and the other field contains the even-numbered lines. A new field is “scanned” onto the display about every 1/60th of a second under the NTSC standard. Because the two fields are displayed so close in time to one another, a human viewer does not perceive the gaps in between the rows in each field. Because a full image-worth of lines results from displaying of two fields, the NTSC frame rate is generally regarded as about 1/30th of a second.

Under the ATSC standard, scanning can be either interlaced, as described above, or “progressive.” In progressive scanning, each field contains all rows. Most modern televisions use progressive scanning. If a television signal is interlaced, the television must convert the interlaced signal to a progressive signal so that it may be displayed. This conversion is known as “de-interlacing” and involves filling in the missing rows in each field. One such method involves analyzing the corresponding lines in adjacent fields, which is known as “interfield” de-interlacing or “temporal” de-interlacing. Another method involves analyzing adjacent lines in a particular field, which is known as “intrafield” de-interlacing or “spatial” de-interlacing. In general, interfield de-interlacing produces better quality for low-motion video, and intrafield de-interlacing produces better quality for high-motion video. In some implementations, interfield

and intrafield techniques can be combined in varying proportions depending on the degree of motion.

Scaling is another common consideration in high definition televisions. Most such televisions have a 16:9 aspect ratio, meaning that the ratio of width to height is 16:9. Standard definition television signals, by contrast, have an aspect ratio of 4:3. To display 4:3 video without displaying black bars on either side of it, the 4:3 video can be “scaled” to fill the extra width available on the 16:9 television, such as by stretching or zooming.

B. Technical Background Regarding Digital Cable and “QAM”

The VIZIO patents pertain to cable television transmission and reception. Television programs are transmitted over fiber optic cables and coaxial cables to a customer location, such as a residence, where the cable signal is processed by either a “set top box” connected to a television or, in the case of a “cable-ready” television, by the television itself. The cable television signal itself is similar to the over-the-air signal discussed above, but the signal is carried over a cable rather than being broadcast over the air.

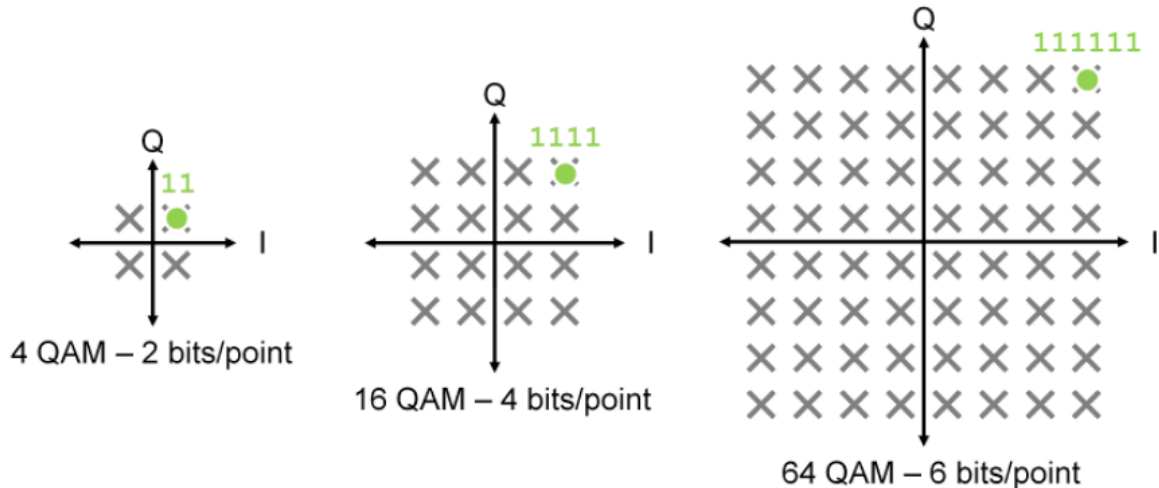
As in broadcast television, signals are limited by the bandwidth of each channel. Each so-called “physical” channel is typically 6 MHz wide, and the electromagnetic spectrum for these channels is regulated by the government. In traditional analog cable television, each 6 MHz channel could carry one programming service (for example, CNN, ESPN, HBO, etc.). Using multiplexing, many television programs can be transmitted within each physical channel. The meaning of the term “channel” in modern television therefore depends on context. One type of “channel” is the communication channel, that is, the portion of the electromagnetic spectrum that is used to carry the signal. The other usage of the term “channel,” which is the meaning

commonly understood by television viewers, refers to the particular programming service (for example, CNN, ESPN, HBO, etc.) that is obtained from the multiplexed signal transmitted in each 6 MHz channel. Increasing the amount of data transmitted on each 6 MHz channel is sometimes referred to as increasing “spectral efficiency.”

Digital cable television programs are encoded and transmitted using quadrature amplitude modulation (“QAM,” sometimes pronounced “quam”), which is analogous to the encoding used in the ATSC standard for over-the-air broadcasting. QAM uses amplitude shift keying of two carrier wave components, namely an in-phase component (“I component”) and a quadrature component (“Q component”). In other words, the amplitude of each component is varied in order to convey information. The QAM carrier wave is a combination of the I component and the Q component. Depending on the type of QAM encoding, such as 4-QAM, 16-QAM, or 64-QAM, particular carrier waveforms can be associated with groups of two bits, four bits, or six bits, respectively. A “QAM constellation” is a graph that depicts each grouping of bits with respect to the amplitudes of its I and Q components. The following illustration is from Hitachi’s technical tutorial to the Court regarding the VIZIO patents:

Modulation: Quadrature Amplitude Modulation

- To send data at a higher rate, use a signal constellation with more points



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To reduce the likelihood of errors that could be caused by interference during transmission, the encoded data may include “forward error correction,” also known as “channel coding.” In cable television, two such techniques include “block coding” and “convolutional coding.” In a simple “repetition” block code, a single binary “1,” for example, is encoded as a block of multiple “1s.” These redundant bits added by the block coder are sometimes referred to as “parity bits.” For example, if “1s” and “0s” are blocked as “111” and “000,” respectively, then if something else is received, such as “101,” then the receiver recognizes that “101” is an error and would correct it (by “majority vote”) to “111”. Reed Solomon coding, which is also used in the ATSC standard, is a form of block coding. Reed Solomon coding for cable television

typically has a rate of 121/127 or 121/128. The rate of 121/127, for example, means that for every 121 symbols that enter the encoder, 127 symbols are outputted, 6 of which are “redundant” symbols used for error detection and correction. The group of 127 Reed Solomon symbols is referred to as a “Reed Solomon block.”

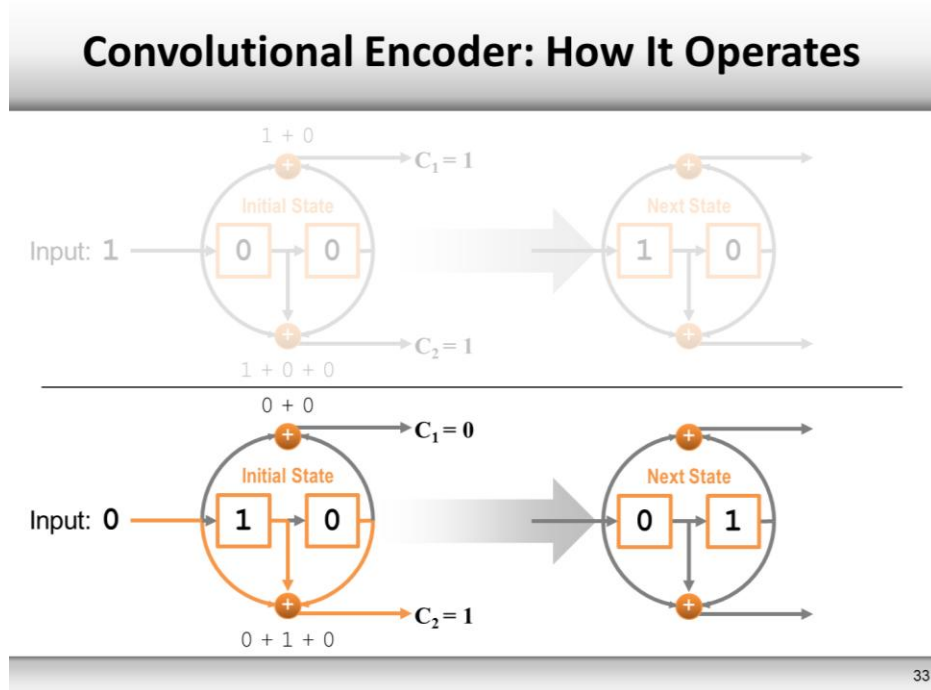
Convolutional coding, by contrast, acts upon individual bits rather than blocks. The convolution coder for cable television encoding uses a combination of exclusive OR (“XOR”) gates and shift register stages.

In general, an XOR gate will output a “1” if either one of its binary inputs, but not both, is “1.” Otherwise, the XOR gate will output a “0.” Stated another way, an XOR gate will produce a “1” if the sum of the inputs is odd and a zero if the sum of the inputs is even. For example, an XOR gate that receives two binary inputs will produce a “1” if the input bits are different (a “1” and a “0”) and will produce a “0” if the input bits are the same (two “1s” or two “0s”).

A shift register is a series of stages that can each hold, for example, one bit. Upon receiving a clock signal, the content of each stage is advanced to the next stage. In other words, each bit is shifted over to the next stage. With each clock signal, a new bit enters the shift register and the bit contained in the last shift register stage is discarded.

In a convolutional code, some of the shift register stages are used to represent a “state” associated with the bits present in those stages. As the next bit in a stream of bits enters the shift register, the bits in each stage are shifted to the next stage. The shift register thereby enters a new “state.” A change between states is referred to as a “transition.” The bits in certain stages are applied to XOR gates in order to generate the convolutional code, which for purposes of the

above-captioned case comprises two streams of bits. The following illustration is from Hitachi's technical tutorial to the Court regarding the VIZIO patents:



The “rate” of the convolutional encoder is the ratio between the number of input bits and the number of output bits. For example, if two bits are generated for every one bit that is inputted, as in the illustration above, the encoder is a “Rate 1/2” convolutional encoder.

The convolutional code is decoded by the receiver using a “Trellis diagram.” The Trellis diagram illustrates all of the possible states of the convolutional encoder as well as all of the possible transitions between states. Using the “Viterbi” algorithm, the receiver can determine the path through the Trellis diagram that has the least likelihood of error. That path determines the data stream that is recovered from the convolutional code.

The number of bits in the convolutional code can be reduced by a process known as “puncturing,” which removes certain bits from the convolutional code in accordance with a

“puncture map.” In the embodiments discussed in the VIZIO patents, three out of every eight convolutional bits are removed. In this manner, a Rate 1/2 convolutional encoder can be converted into a Rate 4/5 punctured convolutional encoder.

“Interleaving” is another technique for reducing errors. Interleaving involves rearranging the bits or blocks in a data stream so that bursts of errors are less likely to affect adjacent bits or blocks. In other words, when the receiver de-interleaves the signal, the bits or blocks that were affected by a burst of errors during transmission are no longer adjacent, which gives the receiver a better chance of using adjacent bits or blocks to correct the errors.

Similarly, “randomization” or “scrambling” refers to a process whereby certain bits are changed in accordance with a “scrambling sequence,” which specifies which bits will be “flipped” before transmission. Upon reception, the signal can be “de-randomized” or “descrambled” by applying the same scrambling sequence so as to return the flipped bits to their original state. The scrambling sequence can be generated by a “linear feedback shift register” (“LFSR”), in which the term “feedback” means that the contents of certain register stages are used to generate input that is fed back into the shift register as input. Scrambling avoids long runs of “0s” or “1s” that could disrupt synchronization of the receiver with the signal. Scrambling can also be used to prevent access by unauthorized receivers.

The various coding and error correction techniques described above are applied so as to encode and decode a television signal. This usage of multiple different techniques on the same signal is referred to as “concatenated coding.” The first coding process is referred to as the “outer code,” and the last coding process is referred to as the “inner code.”

Convolutional coding can be combined with QAM modulation in a process known as “Trellis coded modulation” (“TCM”) or simply “coded modulation.” In TCM, redundancy is achieved by using a larger QAM signal constellation.

Much like ATSC television signals, cable television signals consist of “transport packets,” each of which includes a header and a payload. The header includes a “sync byte,” which is a set of bits that is the same for all transport packets and that is used to synchronize the receiver with the transport stream, that is, the stream of packets being received. Alternatively, the “sync byte” can be replaced with a “parity byte,” which serves the same purpose as the “sync byte” but which varies depending upon the payload of the preceding transport packet. Ultimately, the receiver can reverse the modulation and coding techniques so as to recover the transport packets, extract the payloads, and reproduce audio, video, and program-associated information for the television viewer.

II. LEGAL PRINCIPLES

It is understood that “[a] claim in a patent provides the metes and bounds of the right which the patent confers on the patentee to exclude others from making, using or selling the protected invention.” *Burke, Inc. v. Bruno Indep. Living Aids, Inc.*, 183 F.3d 1334, 1340 (Fed. Cir. 1999). Claim construction is clearly an issue of law for the court to decide. *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 970-71 (Fed. Cir. 1995) (en banc), *aff’d*, 517 U.S. 370 (1996).

To ascertain the meaning of claims, courts look to three primary sources: the claims, the specification, and the prosecution history. *Markman*, 52 F.3d at 979. The specification must contain a written description of the invention that enables one of ordinary skill in the art to make

and use the invention. *Id.* A patent's claims must be read in view of the specification, of which they are a part. *Id.* For claim construction purposes, the description may act as a sort of dictionary, which explains the invention and may define terms used in the claims. *Id.* "One purpose for examining the specification is to determine if the patentee has limited the scope of the claims." *Watts v. XL Sys., Inc.*, 232 F.3d 877, 882 (Fed. Cir. 2000).

Nonetheless, it is the function of the claims, not the specification, to set forth the limits of the patentee's invention. Otherwise, there would be no need for claims. *SRI Int'l v. Matsushita Elec. Corp.*, 775 F.2d 1107, 1121 (Fed. Cir. 1985) (en banc). The patentee is free to be his own lexicographer, but any special definition given to a word must be clearly set forth in the specification. *Intellicall, Inc. v. Phonometrics, Inc.*, 952 F.2d 1384, 1388 (Fed. Cir. 1992). Although the specification may indicate that certain embodiments are preferred, particular embodiments appearing in the specification will not be read into the claims when the claim language is broader than the embodiments. *Electro Med. Sys., S.A. v. Cooper Life Sciences, Inc.*, 34 F.3d 1048, 1054 (Fed. Cir. 1994).

This Court's claim construction analysis is substantially guided by the Federal Circuit's decision in *Phillips v. AWH Corporation*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). In *Phillips*, the court set forth several guideposts that courts should follow when construing claims. In particular, the court reiterated that "the claims of a patent define the invention to which the patentee is entitled the right to exclude." 415 F.3d at 1312 (emphasis added) (quoting *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)). To that end, the words used in a claim are generally given their ordinary and customary meaning. *Id.* The ordinary and customary meaning of a claim term "is the meaning that the term

would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application.” *Id.* at 1313. This principle of patent law flows naturally from the recognition that inventors are usually persons who are skilled in the field of the invention and that patents are addressed to, and intended to be read by, others skilled in the particular art. *Id.*

Despite the importance of claim terms, *Phillips* made clear that “the person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification.” *Id.* Although the claims themselves may provide guidance as to the meaning of particular terms, those terms are part of “a fully integrated written instrument.” *Id.* at 1315 (quoting *Markman*, 52 F.3d at 978). Thus, the *Phillips* court emphasized the specification as being the primary basis for construing the claims. *Id.* at 1314-17. As the Supreme Court stated long ago, “in case of doubt or ambiguity it is proper in all cases to refer back to the descriptive portions of the specification to aid in solving the doubt or in ascertaining the true intent and meaning of the language employed in the claims.” *Bates v. Coe*, 98 U.S. 31, 38 (1878). In addressing the role of the specification, the *Phillips* court quoted with approval its earlier observations from *Renishaw PLC v. Marposs Societa’ per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998):

Ultimately, the interpretation to be given a term can only be determined and confirmed with a full understanding of what the inventors actually invented and intended to envelop with the claim. The construction that stays true to the claim language and most naturally aligns with the patent’s description of the invention will be, in the end, the correct construction.

Phillips, 415 F.3d at 1316. Consequently, *Phillips* emphasized the important role the specification plays in the claim construction process.

The prosecution history also continues to play an important role in claim interpretation. Like the specification, the prosecution history helps to demonstrate how the inventor and the Patent and Trademark Office (“PTO”) understood the patent. *Id.* at 1317. Because the file history, however, “represents an ongoing negotiation between the PTO and the applicant,” it may lack the clarity of the specification and thus be less useful in claim construction proceedings. *Id.* Nevertheless, the prosecution history is intrinsic evidence that is relevant to the determination of how the inventor understood the invention and whether the inventor limited the invention during prosecution by narrowing the scope of the claims. *Id.*; see *Microsoft Corp. v. Multi-Tech Sys., Inc.*, 357 F.3d 1340, 1350 (Fed. Cir. 2004) (noting that “a patentee’s statements during prosecution, whether relied on by the examiner or not, are relevant to claim interpretation”).

Phillips rejected any claim construction approach that sacrificed the intrinsic record in favor of extrinsic evidence, such as dictionary definitions or expert testimony. The *en banc* court condemned the suggestion made by *Texas Digital Systems, Inc. v. Telegenix, Inc.*, 308 F.3d 1193 (Fed. Cir. 2002), that a court should discern the ordinary meaning of the claim terms (through dictionaries or otherwise) before resorting to the specification for certain limited purposes.

Phillips, 415 F.3d at 1319-24. According to *Phillips*, reliance on dictionary definitions at the expense of the specification had the effect of “focus[ing] the inquiry on the abstract meaning of words rather than on the meaning of claim terms within the context of the patent.” *Id.* at 1321.

Phillips emphasized that the patent system is based on the proposition that the claims cover only the invented subject matter. *Id.*

Phillips does not preclude all uses of dictionaries in claim construction proceedings. Instead, the court assigned dictionaries a role subordinate to the intrinsic record. In doing so, the court emphasized that claim construction issues are not resolved by any magic formula. The court did not impose any particular sequence of steps for a court to follow when it considers disputed claim language. *Id.* at 1323-25. Rather, *Phillips* held that a court must attach the appropriate weight to the intrinsic sources offered in support of a proposed claim construction, bearing in mind the general rule that the claims measure the scope of the patent grant.

III. CONSTRUCTION OF AGREED TERMS IN THE “HITACHI” PATENTS

The parties have submitted the following agreed-upon constructions for terms in the Hitachi Patents, which the Court hereby adopts:

Term	Patent/ Claims	Agreed Construction
“reception means for receiving a broadcast program picture and control information which are broadcasted in accordance with a predetermined format, said control information specifying a broadcast system standard”	‘497: claim 13	Governed by [35 U.S.C.] §112 ¶6. <u>Function:</u> receiving a broadcast program picture and control information which are broadcasted in accordance with a predetermined format, said control information specifying a broadcast system standard <u>Corresponding Structure:</u> a reception module (108)
“wherein said reception means receives a plurality of broadcast program pictures multiplexed in a time division manner”	‘497: claim 15	Governed by §112 ¶6. <u>Function:</u> receives a plurality of broadcast program pictures multiplexed in a time division manner <u>Corresponding Structure:</u> a reception module (108)

<p>“broadcast content processing means for controlling and displaying said broadcast program picture in accordance with said broadcast system standard specified by said control information received by said reception means”</p>	<p>‘497: claim 13</p>	<p>Governed by §112 ¶6.</p> <p><u>Function:</u> controlling and displaying said broadcast program picture in accordance with said broadcast system standard specified by said control information received by said reception means</p> <p><u>Corresponding Structure:</u> a reception controller (114)</p>
<p>“control means for specifying a decoding system for said broadcast program picture in accordance with said control information received by said reception means”</p>	<p>‘497: claim 14</p>	<p>Governed by §112 ¶6.</p> <p><u>Function:</u> specifying a decoding system for said broadcast program picture in accordance with said control information received by said reception means</p> <p><u>Structure:</u> a reception controller (114)</p>
<p>“decoder means for decoding said broadcast program picture in accordance with said decoding system specified by said control means”</p>	<p>‘497: claim 14</p>	<p>Governed by §112 ¶6.</p> <p><u>Function:</u> decoding said broadcast program picture in accordance with said decoding system specified by said control means</p> <p><u>Corresponding Structure:</u> a decoder (110)</p>
<p>“display means for displaying said broadcast program picture decoded by said decoder means”</p> <p>“display means for displaying a subject broadcast program picture separated by said separation means”</p>	<p>‘497: claims 14, 15</p>	<p>Governed by §112 ¶6.</p> <p><u>Functions:</u> (1) displaying said broadcast program picture decoded by said decoder means; (2) displaying a subject broadcast program picture separated by said separation means</p> <p><u>Corresponding Structure:</u> a display unit (111)</p>

<p>“control means for specifying said time-division multiplexing system in accordance with said multiplex information item included in said control information received by said reception means”</p>	<p>‘497: claim 15</p>	<p>Governed by §112 ¶6.</p> <p><u>Function:</u> specifying said time-division multiplexing system in accordance with said multiplex information item included in said control information received by said reception means</p> <p><u>Corresponding Structure:</u> a reception controller (114)</p>
<p>“a separation means for selecting a subject broadcast program picture to be displayed and separating said subject broadcast program picture in accordance with said time-division multiplexing system specified by said control means”</p>	<p>‘497: claim 15</p>	<p>Governed by §112 ¶6.</p> <p><u>Function:</u> selecting a subject broadcast program picture to be displayed and separating said subject broadcast program picture in accordance with said time-division multiplexing system specified by said control means</p> <p><u>Corresponding Structure:</u> a signal separator (109)</p>
<p>“control means operates to display said contents of said plurality of broadcast program pictures indicated by said content information items on said display means on a basis of a received said control information, operates to accept selection of a subject broadcast program picture to be displayed, and operates to display a selected said subject broadcast program picture on said display means”</p>	<p>‘497: claim 16</p>	<p>Governed by §112 ¶6.</p> <p><u>Function:</u> operates to display said contents of said plurality of broadcast program pictures indicated by said content information items on said display means on a basis of a received said control information, operates to accept selection of a subject broadcast program picture to be displayed, and operates to display a selected said subject broadcast program picture on said display means</p> <p><u>Corresponding Structure:</u> a reception controller (114)</p>
<p>“receiving means for receiving digital information from a transmission path”</p>	<p>‘375: claims 15, 23</p>	<p>Governed by §112 ¶6.</p> <p><u>Function:</u> receiving digital information from a transmission path</p> <p><u>Corresponding Structure:</u> a reception circuit (30)</p>

<p>“demodulating means for demodulating the digital information received by the receiving means”</p> <p>“demodulating means for demodulating a digital information which is previously received by the receiving means”</p>	<p>‘375: claims 15, 23</p>	<p>Governed by §112 ¶6.</p> <p><u>Function:</u> (1) demodulating the digital information received by the receiving means (2) demodulating a digital information which is previously received by the receiving means</p> <p><u>Corresponding Structure:</u> a demodulation circuit (31)</p>
<p>“error correcting means for correcting an error of the digital information demodulated by the demodulation means based on the error correction information”</p> <p>“error correcting means for correcting an error of a digital information which is previously demodulated by the demodulating means based on the error correction information”</p>	<p>‘375: claims 15, 23</p>	<p>Governed by §112 ¶6.</p> <p><u>Function:</u> (1) correcting an error of the digital information demodulated by the demodulation means based on the error correction information (2) correcting an error of a digital information which is previously demodulated by the demodulating means based on the error correction information</p> <p><u>Corresponding Structure:</u> an error correction circuit (61)</p>
<p>“first expanding means for bit-expanding the video information of the digital information error corrected by the error correcting means in accordance with a first expansion method corresponding to the first compression method”</p> <p>“first expanding means for bit-expanding the video information of a digital information which is previously error corrected by the error correcting means in accordance with a first expansion method corresponding to the first compression method”</p>	<p>‘375: claims 15, 23</p>	<p>Governed by §112 ¶6.</p> <p><u>Function:</u> (1) bit-expanding the video information of the digital information error corrected by the error correcting means in accordance with a first expansion method corresponding to the first compression method (2) bit-expanding the video information of a digital information which is previously error corrected by the error correcting means in accordance with a first expansion method corresponding to the first compression method</p> <p><u>Corresponding Structure:</u> an expansion circuit (62)</p>

<p>“second expanding means for bit-expanding the audio information of the digital information error corrected by the error correcting means in accordance with a second expansion method corresponding to the second compression method”</p> <p>“second expanding means for bit-expanding the audio information of a digital information which is previously error corrected by the error correcting means in accordance with a second expansion method corresponding to the second compression method”</p>	<p>‘375: claims 15, 23</p>	<p>Governed by §112 ¶6.</p> <p><u>Function:</u> (1) bit-expanding the audio information of the digital information error corrected by the error correcting means in accordance with a second expansion method corresponding to the second compression method (2) bit-expanding the audio information of a digital information which is previously error corrected by the error correcting means in accordance with a second expansion method corresponding to the second compression method</p> <p><u>Corresponding Structure:</u> an expansion circuit (63)</p>
<p>“selectively enabling (said one video processor section) while disabling other ones of said video processor sections”</p>	<p>‘243: claim 8</p>	<p>“selectively enabling said one video processor section while disabling other ones of said video processor sections”</p>
<p>“decoding means to decode said audio signal and said video signal from said multiplex isolation means”</p>	<p>‘243: claim 24</p>	<p>Governed by §112 ¶6.</p> <p><u>Function:</u> to decode said audio signal and said video signal from said multiplex isolation means.</p> <p><u>Corresponding Structure:</u> an MPEG decoder (11)</p>
<p>“demodulation means for tuning in a channel of a received signal and performing demodulation thereof”</p>	<p>‘243: claim 24</p>	<p>Governed by §112 ¶6.</p> <p><u>Function:</u> tuning in a channel of a received signal and performing demodulation thereof.</p> <p><u>Corresponding Structure:</u> a demodulator</p>

<p>“multiplex isolation means to isolate an audio signal, a video signal and other types of data coded from said multiplexed signals output from said demodulation means”</p>	<p>’243: claim 24</p>	<p>Governed by §112 ¶6.</p> <p><u>Function:</u> to isolate an audio signal, a video signal and other types of data coded from said multiplexed signals output from said demodulation means.</p> <p><u>Corresponding Structure:</u> a multiplex isolator</p>
<p>“repeatedly read the same line with a line period depending upon a first preset value when said video signal is read from said memory”</p>	<p>’934: claim 1</p>	<p>“repeatedly read the same line with a line period, the line period depending upon a first preset value, when said video signal is read from said memory”</p>
<p>“repeatedly read the same pixel from said memory with a predetermined pixel period depending upon a second preset value when said video signal is read from said memory”</p>	<p>’934: claim 1</p>	<p>“repeatedly read the same pixel from said memory with a predetermined pixel period, said pixel period depending upon a second preset value, when said video signal is read from said memory”</p>
<p>“a clock generator generating a clock having a frequency not less than that of a write clock signal from a writing clock for wiring a video signal in said memory and for outputting a read clock for reading said written video signal from said memory”</p>	<p>’934: claim 1</p>	<p>“a clock generator (i) generating a clock having a frequency not less than that of a write clock signal from a writing clock for writing a video signal in said memory and (ii) for outputting a read clock for reading said written video signal from said memory”</p>
<p>“. . . to thereby provide a video signal representing an image which is compressed and enlarged in horizontal and vertical directions to a desired size as a video signal read from said memory”</p>	<p>’934: claim 1</p>	<p>“to thereby provide a video signal representing an image which is compressed and enlarged in horizontal and vertical directions to a desired size, said video signal being read from said memory”</p>
<p>“generates and outputs an interpolation coefficient depending upon said first preset value as well as the signal for controlling said memory”</p>	<p>’934: claims 2, 3</p>	<p>“generates and outputs: (i) an interpolation coefficient depending upon said first preset value as well as (ii) the signal for controlling said memory”</p>
<p>“at a stage downstream of”</p>	<p>’934: claims 2, 3</p>	<p>“directly or indirectly connected to the output of”</p>

“generates and outputs an interpolation coefficient depending upon said second preset value as well as the signal for controlling said memory”	’934: claim 2	“generates and outputs (i) an interpolation coefficient depending upon said second present value as well as (ii) the signal for controlling said memory.
“it” in the phrase “a line memory for delaying said video signal read from said memory by one line and outputting it”	’934: claim 2	“said delayed video signal read from said memory”
“it” in the phrase “pixel delay means for delaying by one pixel said video signal read from said memory and for outputting it”	’934: claim 3	“said delayed video signal read from said memory”
“means for delaying and outputting the signal and the interpolation coefficient output from said horizontal enlargement controller”	’934: claim 2	Governed by 35 U.S.C. § 112 ¶6. <u>Function:</u> “delaying and outputting the signal and the interpolation coefficient output from said horizontal enlargement controller” <u>Corresponding Structure:</u> delay circuits (116 and 117)
“delaying and outputting the signal and the interpolation coefficient output from said horizontal enlargement controller”	’934: claims 2, 3	“delaying and outputting the signal from said horizontal enlargement controller and delaying and outputting the interpolation coefficient output from said horizontal enlargement controller”
“generating and outputting a horizontal interpolation signal in accordance with the interpolation coefficient output from said means for delaying by using output signals from said vertical interpolator and said pixel delay means”	’934: claims 2, 4	“generating and outputting a horizontal interpolation signal in accordance with (i) the interpolation coefficient output from said means for delaying and (ii) output signals from said vertical interpolator and said pixel delay means”
“generating and outputting an interpolation signal in accordance with an interpolation coefficient output from said vertical enlargement controller by using said video signal read from said memory and the output signal from said line memory”	’934: claims 2, 4	“generating and outputting an interpolation signal in accordance with (i) an interpolation coefficient output from said vertical enlargement controller, (ii) said video signal read from said memory (iii) and the output signal from said line memory”

<p>“generating and outputting an interpolation signal in accordance with the interpolation coefficient output from said first means for delaying by using said video signal read from said memory and the output signal from said pixel delay means”</p>	<p>’934: claim 3</p>	<p>“generating and outputting an interpolation signal in accordance with (i) the interpolation coefficient output from said first means for delaying, (ii) said video signal read from memory and (iii) the output signal from said pixel delay means”</p>
<p>“generating and outputting a vertical interpolation signal in accordance with the interpolation coefficient output from said means for delaying by using the output signal from said horizontal interpolator and the output signal from said line memory”</p>	<p>’934: claim 3</p>	<p>“generating and outputting a vertical interpolation signal in accordance with (i) the interpolation coefficient output from said second means for delaying, (ii) the output signals from said horizontal interpolator and (iii) the output signal from said line memory”</p>
<p>“pixel delay means for delaying the output signal from said vertical interpolator”</p> <p>“pixel delay means for delaying by one pixel said video signal read from said memory and for outputting it, the operation of said pixel delay means being controlled in accordance with an output signal from said first means for delaying”</p>	<p>’934: claims 2, 3, 4</p>	<p>Governed by §112 ¶6.</p> <p><u>Function:</u> “pixel delay means for delaying the output signal from said vertical interpolator” “pixel delay means for delaying by one pixel said video signal read from said memory and for outputting it, the operation of said pixel delay means being controlled in accordance with an output signal from said first means for delaying”¹</p> <p><u>Corresponding Structure:</u> a pixel delay circuit (108)</p>
<p>“first means for delaying and outputting the signal and the interpolation coefficient output from said horizontal enlargement controller”</p>	<p>’934: claim 3</p>	<p>Governed by 35 U.S.C. § 112 ¶6.</p> <p><u>Function:</u> “delaying an outputting the signal and the interpolation coefficient output from said horizontal enlargement controller”</p> <p><u>Corresponding Structure:</u> delay circuits (503 and 504)</p>

¹ This repetition of the claim terms as the “Function” of those claim terms appears in the parties’ submission. (Dkt. No. 127, 8/17/2012 Joint Claim Construction and Pre-Hearing Statement Regarding Hitachi Patents, Ex. A, at 13.)

<p>“delaying and outputting the signal and the interpolation coefficient output from said vertical enlargement controller”</p>	<p>’934: claim 3</p>	<p>“delaying and outputting the signal from said vertical enlargement controller and delaying and outputting the interpolation coefficient output from said vertical enlargement controller”</p>
<p>“second means for delaying and outputting the signal and the interpolation coefficient output from said vertical enlargement controller”</p>	<p>’934: claim 3</p>	<p>Governed by 35 U.S.C. § 112 ¶6.</p> <p><u>Function:</u> “delaying and outputting the signal and the interpolation coefficient output from said vertical enlargement controller”</p> <p><u>Corresponding Structure:</u> delay circuits (501 and 502)</p>
<p>“receiver means for receiving program-associated information including a title, a start time, and an end time of a broadcast program together with a video signal and an audio signal”</p>	<p>’995: claim 1</p>	<p>This term is governed by 35 U.S.C. § 112(6)</p> <p><u>Function:</u> “receiving program-associated information including at tile [sic, a title], a start time, and an end time of a broadcast program together with a video signal and an audio signal”</p> <p><u>Corresponding Structure:</u> a receiver (118)</p>
<p>“decoder means for decoding the program-associated information from the received signal”</p>	<p>’995: claim 1</p>	<p>This term is governed by 35 U.S.C. § 112(6)</p> <p><u>Function:</u> “decoding the program-associated information from the received signal”</p> <p><u>Corresponding Structure:</u> an information decoder (107)</p>
<p>“display controller means for controlling the display screen based on the input signal”</p>	<p>’995: claim 1</p>	<p>This term is governed by 35 U.S.C. § 112(6)</p> <p><u>Function:</u> “controlling the display screen based on the input signal”</p> <p><u>Corresponding Structure:</u> a display controller (109)</p>

<p>“command receiver means for receiving an input signal from a remote controller or from a key or keys provided to a main body of the receiver apparatus”</p>	<p>’995: claim 1</p>	<p>This term is governed by 35 U.S.C. § 112(6)</p> <p><u>Function:</u> “receiving an input signal from a remote controller or from a key or keys provided to a main body of the receiver apparatus”</p> <p><u>Corresponding Structure:</u> a command receiver (106)</p>
<p>“data quantity comparator means for comparing a magnitude of the first display zone with a quantity of display data...”</p>	<p>’995: claim 1</p>	<p>Governed by 35 U.S.C. § 112 ¶6.</p> <p><u>Function:</u> “comparing a magnitude of the first display zone with a quantity of display data”</p> <p><u>Corresponding Structure:</u> a comparator (112)</p>
<p>“said portions” in the phrase “adjusting at least said portions of said displayed image containing said information image based on said control signal”</p>	<p>’713: claims 1, 8, 15</p>	<p>“each portion”</p>
<p>“detection means for detecting a portion of said displayed image containing said information image and outputting a control signal according to said detected portion”</p>	<p>’713: claim 8</p>	<p>This term is governed by 35 U.S.C. § 112(6)</p> <p><u>Function:</u> “detecting a portion of said displayed image containing said information image and outputting a control signal according to said detected portion”</p> <p><u>Corresponding Structure:</u> a decoder (4 or 1206), an EPG processor (1204), a CPU (1220), or a separator (7c)</p>

(Dkt. No. 127, 8/17/2012 Joint Claim Construction and Pre-Hearing Statement Regarding Hitachi Patents, at Ex. A.)

IV. CONSTRUCTION OF DISPUTED TERMS IN THE “HITACHI” PATENTS

A. “broadcast system standard” (‘497 Patent, Claim 13)

Hitachi’s Proposed Construction	Defendants’ Proposed Construction
“a specified set of technical parameter(s) describing how a program is broadcast”	“a regionally adopted standard for broadcast transmissions, such as NTSC, PAL, SECAM, or ISDB”

(Dkt. No. 150-1, 10/3/2012 Joint Claim Construction Chart for Hitachi Patents (“Hitachi Patents JCCC”), at 1.)

(1) The Parties’ Positions

Hitachi submits that its proposed construction is consistent with extrinsic evidence showing how the constituent term “standard” is used by the technical community. (Dkt. No. 137, at 1.) Hitachi also argues that its proposal is “consistent with the purpose of the ‘497 invention,” which includes that “the broadcast program standard (i.e., the technical characteristics describing how a program is broadcast) can be flexibly varied between different channels.” (*Id.*, at 2.) Hitachi argues that Defendants improperly seek to limit the disputed term to “regionally adopted” standards and to the specific set of “NTSC, PAL, SECAM, or ISDB.” (*Id.*) For example, Hitachi notes that the ‘497 Patent refers to ISDB as being “studied” rather than having been adopted, and Hitachi argues that although NTSC, PAL, SECAM and ISDB are examples of broadcast system standards, they are not even specified as part of the preferred embodiment. (*Id.*, at 3.)

Defendants respond that the “specification provides that the standard is country specific (i.e., regionally adopted)” and that examples include NTSC, PAL, SECAM and ISDB. (Dkt. No. 145, at 1 (citing ‘497 Patent at 1:20-30).) As to Hitachi’s criticism of their proposed listing of

standards, Defendants respond that their “construction explicitly provides that NTSC, PAL, SECAM, and ISDB are but examples of broadcast system standards, as stated in the specification.” (*Id.*) Defendants also argue that “[t]echnical dictionaries from the relevant time period consistently show that ‘standards’ are the result of national or international agreements, and are therefore ‘regionally adopted.’” (*Id.*, at 1-2 (footnote omitted).)

Defendants also cite prosecution history during which the United States Patent and Trademark Office (“PTO”) rejected the patentee’s attempt to recite “protocol information” as being unsupported by the specification. (*Id.*, at 2.) The patentee then replaced the term “protocol information” with the now-disputed term “broadcast system standard.” (*Id.*)

Defendants further urge that Hitachi’s proposed construction fails to give meaning to the constituent term “standard” because “[t]he patent’s reference to regionally adopted technical specifications demonstrate the patentee’s view that a standard is not just a set of parameters in isolation.” (*Id.*, at 3.) As to Hitachi’s reliance on dictionary definitions, Defendants respond that “the claim construction does not begin with an analysis of dictionary definitions. Instead, terms are construed in light of the claims, the specification, and the file history.” (*Id.*)

Hitachi replies that Defendants’ proposed term “regionally adopted” appears nowhere in the specification. (Dkt. No. 148, at 1.) Hitachi also argues that Defendants “have no response to the fact that the patent does not describe ISDB as being adopted or deployed in any country; instead it was being ‘studied.’” (*Id.* (citing ‘497 Patent at 1:27).) Hitachi submits that “the drafting of a standard and the adoption of a standard are entirely different things.” (*Id.*) As to the prosecution history cited by Defendants, Hitachi replies that the term at issue is “broadcast system standard,” not “protocol,” and that the patentee defined neither term during prosecution.

(*Id.*, at 2.) Hitachi further argues that “Defendants do not dispute that their construction excludes the only embodiment, as the control information in Figure 3 does not identify NTSC, PAL, SECAM, ISDB, or any ‘regionally adopted’ standard.” (*Id.*) Finally, Hitachi argues that including Defendants’ proposed list of examples “is likely to confuse the jury into thinking that they are required elements.” (*Id.*)

(2) Analysis

Claim 13 recites (emphasis added):

13. A television reception equipment comprising a reception means for receiving a broadcast program picture and control information which are broadcasted in accordance with a predetermined format, said control information specifying a *broadcast system standard*, and a broadcast content processing means for controlling and displaying said broadcast program picture in accordance with said *broadcast system standard* specified by said control information received by said reception means.

The Background of the Invention discloses (emphasis added):

Various broadcasting systems are adopted for present-day television broadcasting.

By way of example, the NTSC system is a *broadcast system standard* generally employed in Japan. In addition to the NTSC system, the PAL system and the SECAM system are employed in many other countries.

Besides, the ISDB (Integrated Services Digital Broadcasting) system has been studied wherein video signals are digitized and then turned into compressed codes, which are subjected to time-division multiplexed transmission.

(‘497 Patent at 1:20-30.)

Defendants also cite prosecution history in which claims were first amended to recite a “protocol” but were then amended to replace the term “protocol information” with the term “broadcast system standard.” (*See* Dkt. No. 147, Ex. A, 1/13/1994 Amendment at 2; *id.*, Ex. C, 6/6/1995 Preliminary Amendment at 2.) This amendment arose out of the examiner’s rejection

of “protocol” as unsupported by the specification, followed by agreement during an examiner interview that “broadcasting system standard” was supported by the specification. (*See id.*, Ex. B, 6/6/1994 Examiner’s Action; *id.*, Ex. C, 6/6/1995 “Preliminary Amendment”² at 8.) As part of this amendment, the patentee also inserted into the written description the lone reference to a “broadcast system standard,” which was added to a pre-existing sentence, as quoted above. (‘497 Patent at 1:22-23.)

On balance, the patentee made no “definitive statements” during prosecution that would limit the term “broadcast system standard” to “a regionally adopted standard for broadcast transmissions.” *Omega Eng. v. Raytek Corp.*, 334 F.3d 1314, 1324 (Fed. Cir. 2003)).

Turning to the extrinsic evidence, Defendants submit that the constituent term “standard” is defined as “a publicly available definition of a hardware or software component, resulting from international, national, or industrial agreement” (Dkt. No. 147, Ex. L, *Dictionary of Computing* 437 (3d ed. 1990)) or as “an instrument source, or other system or device maintained and promulgated by the U.S. National Bureau of Standards as such” (*id.*, Ex. M, *IEEE Standard Dictionary of Electrical and Electronics Terms* 875 (3d ed. 1984)). First, this extrinsic evidence regarding only the constituent term “standard” is disfavored as “focus[ing] the inquiry on the abstract meaning of words rather than on the meaning of claim terms within the context of the patent.” *Phillips*, 415 F.3d at 1321. Second, even these definitions submitted by Defendants do not require a “regionally adopted” standard. Further, using the word “regionally” in the construction would be vague and confusing, and Defendants’ proposal of the word “adopted”

² Although this document is titled “Preliminary Amendment,” it states it is “[i]n response to the Final Office Action dated June 6, 1994.” (*Id.*, at 1.)

would imply some sort of government or industry action, which is not relevant to the claim. In sum, Defendants’ proposed construction should be rejected.

Finally, although Hitachi agreed at the October 23, 2012 hearing that the standards identified in Defendants’ proposed list of examples, “such as NTSC, PAL, SECAM, or ISDB,” are accurate examples of broadcast system standards, such a list of examples is unnecessary and might be read as limiting. Defendants’ proposed list of examples should therefore be omitted from the construction.

The Court therefore hereby construes “**broadcast system standard**” to mean “**a specified set of technical parameter(s) describing how a program is broadcast.**”

B. “control signal information” (‘375 Patent, Claim 32)

Hitachi’s Proposed Construction	Defendants’ Proposed Construction
Plain meaning, no construction necessary	“data used to control a recording process”

(Dkt. No. 150-1, 10/3/2012 Hitachi Patents JCCC, at 26.)

(1) The Parties’ Positions

Hitachi argues that “the ‘375 Patent uses the term ‘control signal’ in contexts other than ‘recording data,’” such as “a ‘speed control signal,’ where the control signal controls the speed of the processing circuitry.” (Dkt. No. 137, at 4.) Hitachi submits that the varied use in the specification supports a broader rather than narrower construction. (*Id.*) Hitachi also cites a January 11, 2011 Amendment in which the patentee referred to “control signal information, which is other than the video signal information and the audio signal information.” (*Id.*) Hitachi further notes that “claim 24 of U.S. Patent No. 5,671,095, a grandparent to the ‘375 patent having the same specification, recites ‘a control signal for recording the digital information

signal.” (Id.) Finally, Hitachi submits that Claim 1 of the ‘375 Patent, from which Claim 32 depends, recites that there is “no recording process.” (Id.)

Defendants respond that “every figure depicting the apparatuses of the disclosed invention shows a recording device” and that the specification states that “the present invention” relates to recording. (Dkt. No. 145, at 4 (citing ‘375 Patent at 1:42-49; citing *Netword, LLC v. Central Corp.*, 242 F.3d 1347, 1352 (Fed. Cir. 2001)).) Defendants also cite the prosecution history, arguing that “Hitachi should not be permitted to argue during prosecution that the term ‘control signal information’ pertains to data used to control a recording process, and now argue for a broader construction.” (Id., at 5.) Defendants further note that Hitachi’s reliance on the disclosure of a “speed control signal” fails because the “processing circuitry” identified in that disclosure is a “recording signal processing circuit.” (Id. (citing ‘375 Patent at Fig. 12, ref. num. 350).) As to Hitachi’s reliance on Claim 1 of the ‘375 Patent, Defendants respond that the claim “merely states that the *transmission path* has no recording process.” (Id.)

In reply, Hitachi cites disclosure in Figure 4 of the ‘375 Patent of a TV signal being “viewed in real-time when switch 132 is in the ‘R’ position, without any intervening recording process.” (Dkt. No. 148, at 1-2.) Hitachi argues that the disclosures cited by Defendants “are typical descriptions of a preferred embodiment and do not purport to define ‘control signal information’ as recording data.” (Id., at 2.)

(2) Analysis

Although Hitachi proposes plain and ordinary meaning, the parties have presented a “fundamental dispute regarding the scope of a claim term,” and the Court has a duty to resolve

that dispute. *O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co.*, 521 F.3d 1351, 1362-63 (Fed. Cir. 2008).

Claim 32 of the '375 Patent, which is the claim at issue, depends from Claim 31, which in turn depends from Claim 1 (emphasis added):

1. A digital information receiving apparatus, comprising:
 - a receiver configured to receive digital information from a transmission path, wherein the digital information includes video information bit-compressed by a first compression method, audio information bit-compressed by a second compression method which is different from the first compression method, and error detection information added to the video information and separately added to the audio information, respectively;
 - a demodulator configured to demodulate the digital information received by the receiver;
 - an error detector configured to detect an error which occurs in the transmission path of the digital information demodulated by the demodulator based on the error detection information, the error being the error which occurs in the transmission path having no recording process of the digital information therein;
 - a first expander configured to bit-expand the video information of the digital information error detected by the error detector in accordance with a first expansion method corresponding to the first compression method; and
 - a second expander configured to bit-expand the audio information of the digital information error detected by the error detector in accordance with a second expansion method corresponding to the second compression method.

* * *

31. A digital information receiving apparatus, according to claim 1, further comprising:
 - a control signal detector configured to detect *control signal information* generated by a control signal generator.
32. A digital information receiving apparatus, according to claim 31, further comprising:
 - a parity addition circuit configured to add parities to the *control signal information*.

The specification discloses that time-compressed “high-speed recording onto a tape,” as well as control of multiple recording devices, can be achieved using control signals:

Further, *control signals* indicative of the start of recording and the stop of recording may be transmitted. The transmitted signals are received and error-corrected, and controls of the standby for recording, the start of recording and the stop of recording are made on the basis of the control signals.

. . . Simultaneous and selective control of the start/stop of recording for a multiplicity of VTR's can be made in such a manner that the address signals corresponding to the VTR's are transmitted prior to a signal to be recorded, the correction for an error of the received signal is made, required VTR's are brought into recording standby conditions by the corrected address signals, and the controls of the start of recording and the stop of recording are made by the transmitted *control signals*.

(‘375 Patent at 2:33-3:7 (emphasis added).)

According to one of [the] applications of the present invention, it is possible to transmit a signal from a transmission signal processing system to a multiplicity of VTR's through a transmission path simultaneously and at a high speed, as has already been mentioned. In this case, it is difficult to control a multiplicity of []VTR's simultaneously. Further, it is required to make a control which causes specified ones of the VTR's to perform recording operations and specified others of the VTR's not to perform recording operations. A technique for realizing such a control will be shown just below.

For the above purpose, *control signals* are transmitted prior to transmission of a signal to be recorded. One example of the *control signals* is shown in FIG. 6. In the figure, reference numeral 110 denotes a synchronizing signal, numeral 111 an ID signal indicative of a control to be made, numeral 112 an address signal indicative of a VTR to be controlled, numeral 113 a *control signal* for bringing a VTR designated by the address signal 112 into a recording mode, numeral 114 a *control signal* for stopping the recording, numerals 115 and 116 blank signals, and numeral 120 a recording signal to be actually recorded.

The ID signal 111 indicating the transmission of the address signals 112 indicative of VTR's in which a signal is to be recorded, is transmitted at a predetermined position relative to the synchronizing signal 110 to bring each VTR into a standby condition. After all the address signals have been transmitted, the ID signal 113 is transmitted to start the recording of the signal 120 in the designated VTR's. After the signal 120 has been transmitted, the ID signal 114 to control the stop of recording is transmitted. Each of the blank signals 115 and 116 is a signal for conforming a signal transmission format to the other transmission signal and is therefore an insignificant signal portion.

In the embodiments shown in FIGS. 1 and 5, those *control signals* are produced by a *control signal* generation circuit 130 and are transmitted with parities which are added by the parity addition circuit 24 for making correction for an error produced during transmission.

In the VTR shown in FIG. 1, *the control signals* are detected by a control circuit 131 after the reception by the reception circuit 30, the demodulation by the demodulation circuit 31 and the correction by the error correction circuit 32 for an error produced during transmission to make a control for the recording and the stop of recording in the recording/reproducing system.

(‘375 Patent at 9:4-48 (emphasis added).) Although Hitachi relies on disclosure of a “speed control signal” as evidence that “control signal” should be construed broadly, the “speed” in that disclosure is the speed of the tape in the recording or playback system. (See, e.g., *id.* at 14:34-55 & Fig. 18.)

On one hand, the Federal Circuit has “expressly rejected the contention that if a patent describes only a single embodiment, the claims of the patent must be construed as being limited to that embodiment.” *Phillips*, 415 F.3d at 1323.

On the other hand, the claims must be construed in the context of the specification:

The claims are directed to the invention that is described in the specification; they do not have meaning removed from the context from which they arose. Thus the claims are construed to state the legal scope of each patented invention, on examination of the language of the claims, the description in the specification, and the prosecution history. See *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1250, 48 USPQ2d 1117, 1122 (Fed. Cir. 1998) (“[T]he interpretation to be given a term can only be determined and confirmed with a full understanding of what the inventors actually invented and intended to envelop with the claim.”). Although the specification need not present every embodiment or permutation of the invention and the claims are not limited to the preferred embodiment of the invention, see *Comark Communications, Inc. v. Harris Corp.*, 156 F.3d 1182, 1186, 48 USPQ2d 1001, 1005 (Fed. Cir. 1998), neither do the claims enlarge what is patented beyond what the inventor has described as the invention.

Netword, LLC v. Centraal Corp., 242 F.3d 1347, 1352 (Fed. Cir. 2001).

The “consistent[] and exclusive[]” disclosure of “control signals” as controlling a recording or playback process “is clearly what the inventors of the . . . patent conceived of” and should inform the proper construction of the disputed term. *Hologic, Inc. v. SenoRx, Inc.*, 639 F.3d 1329, 1338 (Fed. Cir. 2011); *Nystrom v. TREX Co., Inc.*, 424 F.3d 1136, 1144-45 (Fed. Cir. 2005) (construing term “board” to mean “wood cut from a log” in light of the patentee’s consistent usage of the term; noting that patentee “is not entitled to a claim construction divorced from the context of the written description and prosecution history.”).

The Court therefore hereby construes “**control signal information**” to mean “**data used to control a recording or playback process.**”

C. “error-detection information” (‘310 Patent, Claim 1; ‘375 Patent, Claim 1)

Hitachi’s Proposed Construction	Defendants’ Proposed Construction
Plain meaning, no construction necessary	“information that can detect but not correct an error”

(Dkt. No. 150-1, 10/3/2012 Hitachi Patents JCCC, at 26.) The ‘310 Patent and the ‘375 Patent are in the same patent family and are both continuations of the ‘769 Patent, which has also been asserted by Hitachi in the above-captioned case. The ‘310 Patent and the ‘375 Patent therefore share a common set of figures and a common written description.

(1) The Parties’ Positions

Hitachi argues that by their proposed negative limitation, “Defendants attempt to evade a basic tenet of patent law that ‘an accused device that contains the same feature as the patented device [here error detection] cannot escape infringement because in it that feature performs an additional function [error correction]” (Dkt. No. 137, at 5 (quoting *Radio Steel & Mfg. Co. v. MTD Prods., Inc.*, 731 F.2d 840, 848 (Fed. Cir. 1984)).) Hitachi argues that Defendants’

proposal would exclude the preferred embodiments because “the specification discloses that both error detection and error correction are performed with the same information – a parity signal.”

(*Id.* (citing ‘375 Patent at 2:46-48, 2:59-61, 5:37-41, 5:46-50, 6:8-12 & 7:11-14).) Finally, Hitachi submits that “U.S. Patent No. 5,172,380 (cited on face of ‘375 Patent) recites an ‘error detection code’ used for both error detection and correction” and that “U.S. Patent No. 4,211,997 describes ‘error detection information’ being used to detect, correct, and conceal errors.” (*Id.*)

Defendants respond that “Claim 1 [of the ‘375 Patent] uses ‘detection’ and Claim 3 [of the ‘375 Patent] uses ‘correction,’ and variants thereof. The choice of different words in these two independent claims gives rise to the presumption that they have different meanings.” (Dkt. No. 145, at 6 (citing *Seachange Int’l, Inc. v. C-COR, Inc.*, 413 F.3d 1361, 1368-69 (Fed. Cir. 2005); *Andersen Corp. v. Fiber Composites, LLC*, 474 F.3d 1361, 1370 (Fed. Cir. 2007) (“To the extent that the absence of such difference in meaning and scope would make a claim superfluous, the doctrine of claim differentiation states the presumption that the difference between claims is significant.”); 37 C.F.R § 1.75(b) (“More than one claim may be presented provided they differ substantially from each other and are not unduly multiplied.”)).) As to the disclosure of a “parity signal,” Defendants argue that “[a]t most, a ‘parity signal’ can be equated with the claim element ‘error correction information’” because “[t]he specification never equates the ‘parity signal’ with ‘error detection information’ alone.” (*Id.*, at 7.) As to the other patents cited by Hitachi, Defendants respond that there “the patentees acted as their own lexicographers, and properly defined ‘error detection [code/information]’ to include error correction,” whereas “[t]he patents-in-suit provide no such definition.” (*Id.* (footnote omitted).) Defendants urge that “Hitachi had

the opportunity to explicitly define ‘error detection information,’ just as was done by the unrelated patentees, but it failed to do so.” (*Id.*, at 8.)

Hitachi replies that the usage of “error correction information” in the claims does not preclude “error detection information” from performing error correction. (Dkt. No. 148, at 3.) Specifically, Hitachi argues that “[e]rror detection information’ must at least perform error detection but is neither required nor precluded from performing error correction. In contrast ‘error correction information’ must perform error correction.” (*Id.*) Hitachi further reiterates that “the only signal described in the patent for detecting errors (i.e., the parity signal) is also the only signal described as correcting errors. (*Id.* (citing ‘375 Patent at 7:11-14).)

(2) Analysis

Claim 1 of the ‘375 Patent recites (emphasis added):

1. A digital information receiving apparatus, comprising:
 - a receiver configured to receive digital information from a transmission path, wherein the digital information includes video information bit-compressed by a first compression method, audio information bit-compressed by a second compression method which is different from the first compression method, and *error detection information* added to the video information and separately added to the audio information, respectively;
 - a demodulator configured to demodulate the digital information received by the receiver;
 - an error detector configured to detect an error which occurs in the transmission path of the digital information demodulated by the demodulator based on the *error detection information*, the error being the error which occurs in the transmission path having no recording process of the digital information therein;
 - a first expander configured to bit-expand the video information of the digital information error detected by the error detector in accordance with a first expansion method corresponding to the first compression method; and
 - a second expander configured to bit-expand the audio information of the digital information error detected by the error detector in accordance with a second expansion method corresponding to the second compression method.

Claim 1 of the ‘310 Patent recites “error-detection information” in a similar manner:

1. An apparatus for receiving digital information including at least one of digital video information and digital audio information, comprising:
 - a receiver which receives the digital information that has digital video information bit-compressed by a first compression system, digital audio information bit-compressed by a second compression system, and *error-detection information* added to both the digital video information and the digital audio information;
 - a demodulator which demodulates the digital information received by the receiver;
 - an error detector which detects an error of digital information demodulated by the demodulator by use of the *error-detection information*;
 - a first expander which bit-expands video information among the digital information error detected by the error detector corresponding system; and
 - a second expander which bit-expands audio information among the digital information error detected by the error detector corresponding to the second compression system.

The specification discloses (emphasis added):

The detection of an error produced in a transmitting system and the correction for the error can be made using the added parity signal. The error-corrected signal is added with a parity signal for correction for an error produced in a magnetic recording/reproducing system and is modulated to a code adapted for the magnetic recording/reproducing system. Upon recording, since the rotation frequency of the cylinder and the travel speed of the magnetic tape are increased by m times, the recording onto the magnetic tape can be made at an m-tuple speed. Upon reproduction, by setting the rotation frequency of the cylinder and the travel speed of the magnetic tape to normal ones, the reproduction at a normal speed can be made. The reproduced signal is code-demodulated. The detection of an error produced in the magnetic recording/reproducing system and the correction for the error can be made on the basis of the parity signal.

(‘375 Patent at 2:46-61.)

Next, explanation will be made of the operation of the VTR for receiving and recording the transmitted signal. The signal transmitted from the transmission signal processing system is received by the reception circuit 30. The received signal is inputted to the demodulation circuit 31. The demodulation circuit 31 is provided corresponding to the modulation and demodulates the signal to the original signal. The demodulated signal is inputted to the *error correction circuit 32 in which the detection of and the correction for an error produced in the transmission path 27 are made on the basis of the parity signal added by the parity addition circuit 24*. At this time, in the case where the S/N [(signal-to-noise)] ratio of the transmission system is not sufficient so that complete

correction for the error is impossible, correction is made through, for example, signal replacement, by use of the signal correlation.

An output signal of the error correction circuit 32 is inputted to the parity addition circuit 33. *In the parity addition circuit 33, a parity signal for detecting an error produced in a recording/reproducing process and making correction for the error is added.* The parity-added signal is inputted to the modulation circuit 34. In the modulation circuit 34, the signal is modulated to scrambled NRZ [(non-return-to-zero)] code, M² code or the like as mentioned above. The modulated signal is recorded on the magnetic tape 40 by the magnetic heads 41 and 42 mounted on the cylinder 43.

(*Id.* at 5:37-55.)

Upon reproduction, the travel speed of the magnetic tape 40 and the rotation frequency of the cylinder 43 are set to those upon normal reproduction. The reproduced signal is inputted to the demodulation circuit 60. The demodulation circuit 60 is provided corresponding to the modulation circuit 34 and demodulates the modulated signal. The demodulated signal is inputted to the *error correction circuit 61 in which the detection of an error produced in the magnetic recording/reproducing system and the correction for the error are made on the basis of the parity signal added by the parity addition circuit 33.*

(*Id.* at 6:2-12.)

In the embodiment shown in FIG. 1, the *parity signal is added in order to make the detection of and the correction for an error* which may be produced in the transmission system or the magnetic recording/reproducing system.

(*Id.* at 7:11-14).

On balance, these disclosures of information that can be used both to detect errors and to correct errors outweigh any claim differentiation argument regarding the use of “error detection information” as opposed to “error correction information” in Claims 1 and 3 of the ‘375 Patent, respectively. *Edwards Lifesciences LLC v. Cook Inc.*, 582 F.3d 1322, 1331 (Fed. Cir. 2009) (“[C]laim differentiation is a rule of thumb that does not trump the clear import of the specification.”). Moreover, nothing in the above-quoted claims excludes correction as a use of error “detection” information. Finally, Defendants have identified no disclaimer in the

specification or the prosecution history that would justify limiting the claim scope. The Court therefore hereby expressly rejects Defendants’ proposed negative limitation in their proposal of “information that can detect but not correct an error.”

Having resolved the parties’ dispute, “error detection information” need not be construed any further. *O2 Micro*, 521 F.3d at 1362 (“[D]istrict courts are not (and should not be) required to construe *every* limitation present in a patent’s asserted claims.”).

The Court accordingly hereby construes “**error detection information**” to have its plain and ordinary meaning.

D. “processing” (‘243 Patent, Claims 1 & 24; ‘281 Patent, Claims 6 & 14)

Hitachi’s Proposed Construction	Defendants’ Proposed Construction
Plain meaning, no construction necessary	“conversion into an appropriate analog video signal”

(Dkt. No. 150-1, 10/3/2012 Hitachi Patents JCCC, at 30.) The ‘243 Patent and the ‘281 Patent are in the same patent family. Specifically, the ‘281 Patent is one of a string of continuations based on the ‘243 Patent, so the ‘243 Patent and the ‘281 Patent share a common set of figures and a common written description.

(1) The Parties’ Positions

Hitachi argues that Defendants’ proposed construction improperly “import examples from the specification into the claims.” (Dkt. No. 137, at 6.) To the contrary, Hitachi argues, “the patent broadly uses the term ‘processing’ in various ways.” (*Id.* (citing ‘281 Patent at Abstract, 2:6-18, 2:42-44 & 6:57-59).) Hitachi also submits that “the file history broadly uses the term ‘processing’ in relation to different video formats, without regard to analog or digital.” (*Id.*) Hitachi also cites the usage of “processing” in several prior patents, including a prior art

reference cited in the prosecution history of the '281 Patent, to “confirm that a person skilled in the art would understand that ‘processing’ could include purely digital processing without any digital to analog conversion.” (*Id.*, at 7.) Hitachi concludes that “[w]hile video encoders 141, 142, and 143 are described in a preferred embodiment as converting video signals into analog format . . . there is no indication that the patentee defined ‘processing’ to be synonymous with such conversion or that the patentee ‘unequivocally disavowed a certain meaning to obtain his patent’ using ‘clear and unmistakable’ statements.” (*Id.* (citing ‘281 Patent at 3:20-30; citing *Omega Eng.*, 334 F.3d at 1324-25).)

Defendants respond that Figures 4B and 11, relied upon by Hitachi, “pertain to processing ‘scanning information packets’ and ‘scanning-method data,’ neither of which has anything to do with processing the video signal.” (Dkt. No. 145, at 8.) Defendants also argue that “[d]uring prosecution of the ‘243 patent, the claims were rejected over the Reitmeier reference, and Hitachi argued that the reference failed to disclose ‘processing’ because it ‘do[es] not convert a video signal format, but instead, simply resize[s] within a same video signal format.’” (*Id.*, at 9 (citing Dkt. No. 147, Ex. D, 9/20/2001 Response, at 4-5).) Defendants conclude that “Hitachi cannot now argue that the term ‘processing’ broadly means any type of processing” because “[a]s admitted during prosecution of the ‘243 patent, ‘processing’ involves ‘conversion,’ and not just any conversion, but ‘conversion into an appropriate analog video signal,’ as described in the specification.” (Dkt. No. 145, at 9.)

Hitachi replies that “[t]he office action response cited by Defendants does not distinguish the Reitmeier reference on the basis that it does not convert signals into ‘analog’ signals,” and

Hitachi notes that “[t]he term ‘analog’ appears nowhere in the response [to the PTO’s office action].” (Dkt. No. 148, at 3.)

(2) Analysis

Claim 1 of the ‘243 Patent is representative and recites (emphasis added):

1. A digital broadcast receiver unit for receiving a digital multiplexed signal stream having multiplexed signals commonly encoded using a same encoding/decoding standard, said multiplexed signals including video signals corresponding to a plurality of different video signal formats, and isolating and reproducing at least one video signal, said unit comprising:
 - an isolator to isolate one video signal from a received said digital multiplexed signal;
 - a decoder to decode the video signal from said isolator according to said encoding/decoding standard;
 - a plurality of video processor sections, with respective video processor sections providing video *processing* according to a different video signal format of said plurality of different video signal formats; and
 - a controller using information from the received said digital multiplexed signal to determine a video signal format of said video signal from said decoder, and selecting one video processor section of said video processor sections to perform video *processing* of said video signal according to a determined video signal format thereof.

The parties’ dispute focuses on whether the patentee limited the scope of the term “processing” during prosecution of the ‘243 Patent by distinguishing the “Reitmeier” reference, United States Patent No. 6,118,486:

Office Action comments assert that the applied Reitmeier reference describes a controller 200 which utilizes information (format, colorimetry and other information) and additional information related to display device 175 (e.g., the native format of the display device), to generate a vertical size control signal VS for vertical resizer 140, horizontal size control signal HS for horizontal resizer 150 (col. 7, lines 11-16), and that the vertical resizer 140 and horizontal resizer 150 provide a format conversion function that is controlled by the controller 200 (col. 8, lines 37-39). Strong traversal is appropriate.

That is to say, Reitmeier’s vertical resizer 140 and horizontal resizer 150 sections do not convert video signal format, but instead, simply resize with the same video signal format. More particularly, a video signal format (e.g., DTV, MPEG-1, etc.)

proceeding to the resizers 140, 150, retains the same video signal format (e.g., DTV, MPEG-1, etc.), but is resized by having a number of picture elements (pixels) per line changed or has a number of scanning lines changed. Therefore, Reitmeier does not disclose Applicant's claimed "plurality of video processor sections . . . providing video processing according to a different video signal format". Further, even assuming arguendo that Reitmeier's resizers 140, 150 are "a plurality . . .", Reitmeier's arrangement still would not disclose Applicant's claimed arrangement of "selecting one video processor section", as Reitmeier's resizers 140, 150 (arranged in series) both have to be selected or else the video signals would not be delivered to Reitmeier's frame buffer 160 (i.e., Reitmeier's arrangement would not work). Accordingly, it is respectfully submitted that Applicant's claimed plurality of video processor sections of the claimed features are not met by horizontal resizer 150 and vertical [resizer] 140 (the reference). Therefore, claim 1 as well as all of Applicant's other claims, are not met by the reference.

(Dkt. No. 147, Ex. D, 9/20/2011 Response, at 4-5.)

At best, this prosecution history includes a statement that the claim language "processing according to a different video signal format" does not refer to merely resizing the video signal. This prosecution history does not limit the term "processing" and contains no statement regarding "conversion into an appropriate analog video signal," as Defendants propose, much less any "definitive statements" to that effect. *Omega Eng.*, 334 F.3d at 1324. Likewise, the specification contains no clear disclaimer either. The Court therefore expressly rejects Defendants' proposed construction.

Having resolved the parties' dispute, the Court finds no further construction necessary. *O2 Micro*, 521 F.3d at 1362 ("[D]istrict courts are not (and should not be) required to construe every limitation present in a patent's asserted claims").

The Court accordingly hereby construes the term "**processing**" to have its plain and ordinary meaning.

E. “video processor sections” (‘243 Patent, Claim 1; ‘281 Patent, Claim 14)

Hitachi’s Proposed Construction	Defendants’ Proposed Construction
Plain meaning, no construction necessary. Alternatively, “a portion of hardware or a portion of a program used to process video”	“separate video encoders (141, 142 and 143)”

(Dkt. No. 150-1, 10/3/2012 Hitachi Patents JCCC, at 34.)

Shortly before the October 23, 2012 hearing, the parties agreed that this term should be construed to have its plain and ordinary meaning.

The Court accordingly hereby construes the term **“video processor subsections”** to have its plain and ordinary meaning.

F. “video processing sub-programs” (‘281 Patent, Claim 6)

Hitachi’s Proposed Construction	Defendants’ Proposed Construction
Plain and ordinary meaning. Alternatively, “subroutines used to process video”	“subroutines used by a video encoder”

(Dkt. No. 150-1, 10/3/2012 Hitachi Patents JCCC, at 40.)

The parties incorporated their arguments as to the term “video processor sections” discussed in subsection IV.E., above. (*See* Dkt. No. 137, at 9; Dkt. No. 145, at 11.)

The parties confirmed at the October 23, 2012 hearing that like “video processor sections,” the term “video processing sub-programs” should also be construed to have its plain and ordinary meaning.

The Court accordingly hereby construes the term **“video processing sub-programs”** to have its plain and ordinary meaning.

G. “video signal scanning methods” (‘243 Patent, Claim 24) and “video signal formats” (‘243 Patent, Claim 1; ‘281 Patent, Claims 6 & 14)

Hitachi’s Proposed Construction	Defendants’ Proposed Construction
“the number of scan lines and whether the lines are progressive or interlaced”	“scanning methods associated with different broadcast system standards such as NTSC, PAL(525), ³ and HDTV”

(Dkt. No. 150-1, 10/3/2012 Hitachi Patents JCCC, at 41-42.)

The parties agree that the terms “video signal scanning methods” and “video signal formats” are used interchangeably in the claims. (Dkt. No. 137, at 9; Dkt. No. 145, at 13.)

(1) The Parties’ Positions

Hitachi argues that “Defendants are not attempting to construe the meaning of these limitations but are instead trying to graft on additional limitations from the preferred embodiments.” (Dkt. No. 137, at 9.) Hitachi submits that the ‘243 Patent and the prior art refer to scanning methods in terms of the number of horizontal lines and “whether these lines are scanned progressively (i.e., one after the other) or interlaced (i.e., the odd lines are scanned and then the even lines are scanned).” (*Id.* at 10 (citing ‘243 Patent at 3:7-17; U.S. Patent No. 5,019,908 at 1:19-32; U.S. Patent No. 5,155,767 at 8:14-20; U.S. Patent No. 5,719,633 at 1:5-48; U.S. Patent No. 5,208,669 at 1:12-21).) Hitachi argues that “Defendants’ construction attempts to preclude a given broadcast system standard from using multiple scanning methods.” (*Id.*) Hitachi also cites disclosure in the prior art that “a given broadcast system standard can employ multiple scanning methods.” (*Id.*, at 11 (citing U.S. Patent No. 5,719,633 at 1:21-36 (describing ATV (Advanced Television) “broadcast system” as supporting a “plurality of video formats”)).)

³ The parties noted at the October 23, 2012 hearing that the PAL standard actually has 625 lines, not 525 lines as indicated here in Defendants’ proposed construction.

Defendants respond that the specification repeatedly cites “NTSC,” “PAL,” and “HDTV” and refers to “scanning methods” or the “scanning approach.” (Dkt. No. 145, at 11-12 (citing ‘243 Patent at 1:17-20, 3:56-65, 6:61-64, Fig. 2B & Fig. 2C).) Defendants also argue that the four unrelated patents cited by Hitachi should be given no weight because “how another patentee chose to define his invention is of little consequence to how the term ‘video signal scanning methods’ and ‘video signal scanning formats’ should be construed under the teachings of the ’243 and ’281 patents.” (*Id.*, at 12.) Finally, Defendants argue that the portion of the specification cited by Hitachi actually supports Defendants’ proposed construction because of the disclosure that “each video encoder is designed to handle a scanning method associated with a particular broadcast system, *i.e.*, NTSC, 525, HDTV.” (*Id.* (citing ‘243 Patent at 3:7-17).)

Hitachi’s reply brief does not address these terms. (*See* Dkt. No. 148.)

(2) Analysis

Claim 24 of the ‘243 Patent is representative and recites (emphasis added):

24. A digital broadcast receiver unit for receiving a digital multiplexed signal stream having multiplexed signals commonly encoded using a same encoding/decoding standard, said multiplexed signals including digitally converted audio signals, different kinds of information and video signals corresponding to at least two *video signal scanning methods*, and for isolating and reproducing at least one signal from among said audio signals, said video signals and said different kinds of information, said unit comprising:

 a demodulation means for tuning in a channel of a received signal and performing demodulation thereof;

 a multiplex isolation means to isolate an audio signal, a video signal and other types of data coded from said multiplexed signals output from said demodulation means;

 a decoding means to decode said audio signal and said video signal from said multiplex isolation means;

 a plurality of video processing means for performing processing of said video signal from said decoding means, according to said at least two *video signal scanning methods*;

a control means for determining a scanning method of said video signal of said channel, and for operating said plurality of video processing means based on a determined said scanning method for said video signal.

By way of background, digital signals can be “multiplexed,” that is, multiple signals can be carried on a single carrier wave, and “video signals for different scanning methods” can be multiplexed. (‘243 Patent at 1:13-20.) The specification discloses the use of multiple encoders (emphasis added):

In FIG. 1, the *numeral 141 is a video encoder*, for instance, to convert 525 interlaced scanning lines of an NTSC system signal into an analog signal and add synchronizing information, etc. The *numeral 142 is a video encoder*, for instance, to convert 525 scanning lines of a sequential scanning 525 progressive signal (hereafter abbreviated to 525P signal) into an analog signal and add synchronizing information, etc. The *numeral 143 is a video encoder*, for instance, to convert the 1080 interlaced scanning lines of an HDTV system signal into an analog signal and add synchronizing information, etc.

(‘243 Patent at 3:7-17.) The specification also discloses that transport packet headers can include information for identifying the “scanning approach” (emphasis added):

The operation when processing video signals for different broadcast systems was explained above. FIG. 2A shows the structure of one unit of the multiplexed signal referred to as a transport stream packet (hereafter TS packet). The TS packet is comprised of a payload for storing data (e.g., video, audio and other info.), a header for indicating data such as identification (e.g., packet number) and/or *scanning approach* (e.g., *NTSC, PAL, etc.*) data, and an error correction check bit for performing error correction. As shown in FIG. 2B, in a digital broadcast, multiplexing of video signals in one stream for a plurality of differing scanning methods can be performed. FIG. 2C shows (without headers and error correction check bits) a state of a TS packet in the case where an NTSC signal and an HDTV signal are multiplexed as one example. As is apparent from such Fig., *video signals of different scanning systems* do not have to be alternately or periodically provided, but instead, can be provided in any order.

(‘243 Patent at 3:53-4:3.) All of these passages, as well as the following, identify certain standards, such as NTSC, merely as examples of scanning methods:

[T]he above explanation described an example of digital broadcast receiver compatible with the three scanning methods consisting of an NTSC signal, a 525P signal and an HDTV signal. However the same effect of the invention can be obtained with a configuration in which other video signal scanning methods are handled by a compatible MPEG encoder or video encoder.

(‘243 Patent at 6:61-67.)

Although the specification thus discloses that various exemplary broadcast standards have certain numbers of scan lines and can be progressively scanned or interlaced, the scanning “method” or “format” is not limited to being a “standard” as Defendants have proposed. Defendants’ proposed construction is therefore rejected.

As a final note, the Court’s conclusion is unaffected by the additional patents cited by Hitachi (cited in subsection IV.G.(1), above), which Defendants have argued should be of no weight in the claim construction analysis.

The Court therefore hereby construes the terms “**video signal scanning methods**” and “**video signal formats**” to mean “**number of scan lines and whether the lines are progressive or interlaced.**”

H. “video processing means . . .” (‘243 Patent, Claim 24)

The disputed term is “video processing means for performing processing of said video signal from said decoding means, according to said at least two video signal scanning methods.”

Hitachi's Proposed Construction	Defendants' Proposed Construction
<p>Governed by § 112 ¶ 6</p> <p>Function: “performing processing of said video signal from said decoding means, according to said at least two video signal scanning methods” [agreed]</p> <p>Corresponding Structure: “Alternatively, 1. Video processors 2. Video processor sections 3. Video encoders 141, 142, 143 4. A subprocessor or singular application specific integrated circuit (ASIC) chip 14, having segregated processing programs”</p>	<p>Governed by § 112 ¶ 6</p> <p>Function: “performing processing of said video signal from said decoding means, according to said at least two video signal scanning methods” [agreed]</p> <p>Corresponding Structure: “separate video encoders (141, 142 and 143)”</p>

(Dkt. No. 150-1, 10/3/2012 Hitachi Patents JCCC, at 46.)

The parties agree that this is a means-plus-function limitation governed by 35 U.S.C. § 112, ¶ 6, and the parties agree upon the claimed function. Thus, the parties only dispute the corresponding structure.

(1) The Parties' Positions

Hitachi submits four corresponding structures in the alternative.

First, the '243 Patent (Ex. 5) Abstract discloses “video processors” for “performing respectively different corresponding scanning methods and connected to an output of the decoder.”

Second, the Summary of the Invention describes “video processor sections providing video processing according to a different video signal format of the plurality of different video signal formats.” [‘243 Patent] at 1:58-61.

Third, the parties agree that video encoders 141, 142 and 143 are a corresponding structure, but Defendants add the word “separate” even though the description of these encoders fails to describe them as “separate.” *Id.* at 3:7-17.

Fourth, the specification describes a subprocessor or ASIC having segregated processing programs or processing areas as performing video processing on different scanning methods. *Id.* at 4:56-5:1. FIG. 3 shows that the subprocessor or ASIC 14 processes video signals from MPEG decoder 11 for output at terminal 15.

(Dkt. No. 137, at 11-12.)

Defendants respond that “[t]he generic claim language repeated in the Abstract and Summary of the Invention sections (*i.e.*, ‘video processor’ and ‘video processor sections’), however, fails to disclose any structure for performing the claimed function.” (Dkt. No. 145, at 13.) Defendants urge that the only embodiment that is disclosed as performing the claimed function is the embodiment shown in Figure 1, which includes a plurality of separate video encoders 141, 142, 143. (*Id.*, at 14.) Finally, Defendants argue that in the “segregated processing programs” embodiment cited by Hitachi, “a particular subroutine is activated, and the video signal is only processed in accordance with one selected video signal scanning method.” (*Id.*) Defendants conclude that the “segregated processing programs” embodiment disclosed in the specification does not satisfy the claimed function of processing according to at least two video signal scanning methods. (*Id.*)

In reply, Hitachi argues that “video processors” and “video processor sections” are structures known to a person of ordinary skill in the art. (Dkt. No. 148, at 4 (citing United States Patent No. 5,319,707 at Fig. 14 & 23:58-61 (depicting “video processor” that is comprised of “standard” devices); United States Patent No. 4,916,640 at FIG. 3B (depicting “video processor section”)).) As to the “segregated processing programs” embodiment, Hitachi replies that “Defendants assume that the video processing means must process two or more

scanning methods simultaneously, but this is not required by the plain language of the claim.”

(*Id.*)

(2) Analysis

As a threshold matter, a patent may disclose multiple alternative corresponding structures for a means-plus-function limitation. *See Ishida Co., Ltd. v. Taylor*, 221 F.3d 1310, 1316 (Fed. Cir. 2000).

First, the Abstract can, in some instances, provide corresponding structure. *Playtex Prods., Inc. v. Procter & Gamble Co.*, 400 F.3d 901, 909 (Fed. Cir. 2005). Here, however, the disclosure of “a plurality of video processors performing respectively different corresponding scanning methods and connected to an output of the decoder” in the Abstract of the ‘243 Patent is insufficient. *See Ergo Licensing, LLC v. Carefusion 303, Inc.*, 673 F.3d 1361, 1363-64 (Fed. Cir. 2012) (“None of these disclosures, however, are structures for the function of ‘controlling the adjusting means.’ The recitation of ‘control device’ provides no more structure than the term ‘control means’ itself, rather it merely replaces the word ‘means’ with the generic term ‘device.’”).

Second, the disclosure of “video processor sections” in the Summary of the Invention merely repeats the language of the claim and therefore is not corresponding structure for purposes of 35 U.S.C. § 112 ¶ 6. *See Ergo Licensing*, 673 F.3d at 1363-64.

Third, the parties are in agreement that video encoders 141, 142 and 143 are a corresponding structure. Although Defendants propose that the structure is “separate” video encoders, that requirement of “separateness” does not appear in the specification, at least not in connection with performing the recited function. *See Chiuminatta Concrete Concepts, Inc. v.*

Cardinal Indus., Inc., 145 F.3d 1303, 1308 (Fed. Cir. 1998) (“The specification . . . elaborates on the details of the preferred skid plate, more particularly defining the structure in ways unrelated to the recited function. These additional structural aspects are not what the statute contemplates as structure corresponding to the recited function.”).

Fourth, then, is the parties’ primary dispute, which is whether the corresponding structure can be “a subprocessor or singular application specific integrated circuit (ASIC) chip 14, having segregated processing programs,” as Hitachi has proposed. The specification adequately discloses such an alternative corresponding structure:

The embodiment of FIG. 3[] differs from the embodiment of FIG. 1 in that the configuration of *the video encoder 14 is a singular circuit, e.g., a sub-processor, etc.*, which versatilely permits processing of any of the NTSC signals, 525 signals or HDTV signals. More particularly, *the video encoder 14 can be provided as a sub-processor or singular application specific-integrated circuit (ASIC) chip, having segregated processing sub-programs or processing areas which can be selectively enabled/disabled to permit processing according to an appropriate scanning method.* While the FIG. 1 approach of separately provided encoders has the power saving advantage that unneeded encoders can be powered down, a FIG. 3 software implemented approach has the advantage that the encoder 14 can be easily changed/customized via simple software reprogramming. The control CPU 6 operates the video encoder 14 so as to match the scanning method detected by the MPEG decoder 11 with any of the three previously related processing means based on information conveyed from the MPEG decoder 11.

(‘243 Patent at 4:58-5:10.) Defendants have argued that this is not corresponding structure because it does not perform the claimed function of processing “at least two video signal scanning methods,” as recited in Claim 24. Hitachi responds, however, that Claim 24 does not require processing multiple video signals simultaneously but rather requires processing one video signal out of multiple video signals. The Court agrees. The sub-processor or ASIC embodiment is therefore a corresponding structure.

Defendants properly note, however, that Hitachi’s proposed construction has reworded the corresponding structure so as to omit the phrase “video encoder.” The Court therefore modifies Hitachi’s proposal so as to align the construction with the above-quoted disclosure that “the video encoder 14 can be provided as a sub-processor or singular application specific-integrated circuit (ASIC) chip.”

The Court accordingly hereby finds that the term **“video processing means for performing processing of said video signal from said decoding means, according to said at least two video signal scanning methods”** is a means-plus-function term, that the claimed function is **“performing processing of said video signal from said decoding means, according to said at least two video signal scanning methods,”** and that the corresponding structure is: **“(1) video encoders 141, 142, 143, and equivalents thereof; or (2) a video encoder 14 provided as a subprocessor or singular application specific integrated circuit (ASIC) chip having segregated processing programs, and equivalents thereof.”**

I. “control means for determining a scanning method of said video signal of said channel” (‘243 Patent, Claim 24)

Hitachi’s Proposed Construction	Defendants’ Proposed Construction
<p>Governed by § 112 ¶ 6</p> <p>Function: “determining a scanning method of said video signal of said channel” [agreed]</p> <p>Corresponding Structure: “Alternatively: 1. An MPEG decoder 2. A controller 3. A control CPU”</p>	<p>Governed by § 112 ¶ 6</p> <p>Function: “determining a scanning method of said video signal of said channel” [agreed]</p> <p>Corresponding Structure: “An MPEG decoder (11)”</p>

(Dkt. No. 150-1, 10/3/2012 Hitachi Patents JCCC, at 47-48.)

The parties agree that this is a means-plus-function limitation, and the parties agree on the claimed function. The parties agree that one corresponding structure that performs the claimed method is “an MPEG decoder (11).” The parties dispute whether the two additional alternative corresponding structures proposed by Hitachi, namely “a controller” and “a control CPU,” are appropriate.

(1) The Parties’ Positions

Hitachi cites the disclosure in the Abstract of the ‘243 Patent of “a controller to . . . determine the scanning method of the video signal of the selected program.” (Dkt. No. 137, at 12 (citing ‘243 Patent at 1:61-67).) Hitachi also cites disclosure in the specification that “control CPU 6 detects the video signal scanning method that was selected.” (*Id.*, at 12-13 (citing ‘243 Patent at 6:30-36).)

Defendants respond that “the mere mention of the word ‘controller’ in the Abstract does not constitute a corresponding structure” and that “‘control CPU 6’ is not used to ‘determine a scanning method from the video signal’” as required by the claimed function. (Dkt. No. 145, at 15.) Specifically, Defendants argue that “[w]hile the specification provides that the control CPU (6) ‘detects the video signal scanning method,’ it detects it from the signal provided by the MPEG decoder 11 -- not from the video signal, as required by the claimed function.” (*Id.*, at 16.)

Hitachi replies that “Defendants cite no evidence that ‘controller’ is not a known structure to those of ordinary skill.” (Dkt. No. 148, at 5.) As to Hitachi’s proposal of the “control CPU,” Hitachi replies that “the specification explicitly states, ‘CPU 6 detects the video signal scanning method’ for the embodiment in FIG. 7 as MPEG decoder 11 does for the embodiment in FIG. 1.” (*Id.* (citing ‘243 Patent at 4:11-13, 6:31-32 & Fig. 7).)

(2) Analysis

First, the parties agree that the “MPEG decoder 11” disclosed in the specification is a corresponding structure (emphasis added):

When the viewer selects the desired program from such signals, e.g., through any know[n] remote or switch arrangement (not shown), the multiplex isolation means 5 responds thereto, and only the coded audio data and the coded video data that comprises the selected program is isolated and output from the multiplex isolation means 5. The coded video data and coded audio data which is output is applied to the MPEG decoder 11. The coded video data includes data detailing the scanning method. *The MPEG decoder 11 detects the data detailing the scanning method from the input coded data and conveys this data to the control CPU 6.*

(‘243 Patent at 4:4-14.)

Second, the Abstract can, in some instances, provide corresponding structure. *Playtex Prods.*, 400 F.3d at 909. Here, the Abstract discloses “a controller to control the upper selector and determine the scanning method of the video signal of the selected program and also perform the appropriate processing based on the scanning method for the selected video signal.” On balance, this disclosure in the Abstract of a “controller” as corresponding structure for a “means” is insufficient. *See Ergo Licensing*, 673 F.3d at 1363-64 (finding that “recitation of ‘control device’ provides no more structure than the term ‘control means’ itself, rather it merely replaces the word ‘means’ with the generic term ‘device.’”).

Third, the specification discloses that in one embodiment, a “control CPU” can “detect[] the video signal scanning method” (emphasis added):

A fifth embodiment of the invention is shown in FIG. 7. The embodiment of FIG. 7 differs from the embodiment of FIG. 1 in that the digital broadcast receiver of this invention is housed in a same cabinet 700 with a display unit, or in other words, this embodiment comprises a television with an internal digital broadcast receiver unit. In FIG. 7, the reference numeral 28 denotes a display signal processing means, 29 denotes an audio signal processing means, 30 denotes a

display means such as a CRT or liquid crystal display panel or a plasma display panel, and 31 denotes an audio signal output means such as a speaker. In FIG. 7, the display processing means 28 and the display means 30 are configured, for example, so that an NTSC signal, a 525P signal or a HDTV signal can be displayed. Also in FIG. 7, *the control CPU 6 detects the video signal scanning method that was selected, operates the video encoders 141, 142 and 143 and along with switching the selection means 27, controls the display processing means 28 and functions to allow processing of video signal scanning method that was detected.* This arrangement permits correct processing of the video signal for the program selected by the equipment comprising a television with an internal digital broadcast receiver unit and display of the program by means of the display means 30.

(‘243 Patent at 6:17-40.) At first blush, this passage appears to disclose that the “control CPU 6” is an alternative to the “MPEG decoder 11” for carrying out the claimed function of determining a scanning method of the video signal. Reading the passage more closely, however, and referring to Figure 7 cited therein, Figure 7 discloses the same MPEG decoder 11 that is disclosed in, for example, Figure 1. The above-quoted passage merely notes that the control CPU 6 detects the scanning method that “was selected” by the MPEG decoder 11. Because the control CPU 6 is not disclosed as performing the claimed function of “determining a scanning method,” the control CPU 6 is *not* an alternative corresponding structure for the “control means” term here at issue. *See Telcordia Techs., Inc. v. Cisco Sys., Inc.*, 612 F.3d 1365, 1376 (Fed. Cir. 2010) (noting that “the written description must clearly link or associate structure to the claimed function”).

The Court accordingly hereby finds that the term “**control means for determining a scanning method of said video signal of said channel**” is a means-plus-function term, that the claimed function is “**determining a scanning method of said video signal of said channel,**” and that the corresponding structure is “**MPEG decoder 11, and equivalents thereof.**”

J. “control means . . . for operating said plurality of video processing means based on a determined said scanning method for said video signal” (‘243 Patent, Claim 24)

Hitachi’s Proposed Construction	Defendants’ Proposed Construction
<p>Governed by § 112 ¶ 6</p> <p>Function: “operating said plurality of video processing means based on a determined said scanning method for said video signal” [agreed]</p> <p>Corresponding Structure: “Alternatively: 1. A control CPU 2. A controller”</p>	<p>Governed by § 112 ¶ 6</p> <p>Function: “operating said plurality of video processing means based on a determined said scanning method for said video signal” [agreed]</p> <p>Corresponding Structure: “A control CPU (6)”</p>

(Dkt. No. 150-1, 10/3/2012 Hitachi Patents JCCC, at 49.)

The parties agree that this is a means-plus-function limitation, and the parties agree on the claimed function. The parties also agreed that one corresponding structure is “a control CPU.” The parties dispute whether Hitachi’s proposal of “a controller” as an additional alternative corresponding structure is appropriate.

(1) The Parties’ Positions

Hitachi relies upon disclosure in the specification that the “controller . . . select[s] one video processor section of the video processor sections to perform video processing of the video signal according to a determined video signal format thereof.” (Dkt. No. 137, at 13 (citing ‘243 Patent at 1:62-67).)

Defendants respond that “such an abbreviated disclosure is insufficient to constitute a corresponding structure.” (Dkt. No. 145, at 17 (citing *Ergo Licensing, LLC*, 673 F.3d at 1363-64).)

Hitachi replies that “Defendants contend that one of ordinary skill would not understand a ‘CPU’ to be a structure, but Defendants fail to cite any evidence for this remarkable contention.” (Dkt. No. 148, at 5.)

(2) Analysis

The Summary of the Invention discloses (emphasis added):

. . . a controller using information from the received the [sic] digital multiplexed signal to determine a video signal format of the video signal from the decoder, and selecting one video processor section of the video processor sections to perform video processing of the video signal according to a determined video signal format thereof.

(‘243 Patent at 1:61-67.) This disclosure of a “controller” as corresponding structure for a “control means” is insufficient. *See Ergo Licensing*, 673 F.3d at 1363-64 (finding that “recitation of ‘control device’ provides no more structure than the term ‘control means’ itself, rather it merely replaces the word ‘means’ with the generic term ‘device.’”).

The Court accordingly hereby finds that the term **“control means . . . for operating said plurality of video processing means based on a determined said scanning method for said video signal”** is a means-plus-function term, that the claimed function is **“operating said plurality of video processing means based on a determined said scanning method for said video signal,”** and that the corresponding structure is **“control CPU 6, and equivalents thereof.”**

K. “means for combining” (‘934 Patent, Claim 1)

The disputed term is “means for combining the output signal from said vertical enlargement controller, the output signal from said horizontal enlargement controller and the read clock from said clock generator and for supplying said memory with a combined signal.”

Hitachi's Proposed Construction	Defendants' Proposed Construction
<p>Governed by § 112 ¶ 6 [agreed]</p> <p>Claimed Functions:</p> <ol style="list-style-type: none"> 1. combining the output signal from said vertical enlargement controller, the output signal from said horizontal enlargement controller and the read clock from said clock generator 2. supplying said memory with a combined signal <p>Corresponding Structure:</p> <ol style="list-style-type: none"> 1. combining circuit 2. circuit, or circuitry, wiring, or traces 	<p>Governed by § 112 ¶ 6 [agreed]</p> <p>The term “means for combining’ fails to meet the requirements of 35 U.S.C. § 112, Paragraphs 1, 2 and/or 6.”</p>

(Dkt. No. 150-1, 10/3/2012 Hitachi Patents JCCC, at 51.)

(1) The Parties' Positions

Hitachi argues that “Defendants have identified the incorrect function” because the language in the claim starting with “to thereby provide” “summarizes the end result of the entire claim, instead of the function of the means for combining.” (Dkt. No. 137, at 14.) Hitachi also submits that “‘supplying said memory with a combined signal’ is performed by a circuit, circuitry, wiring or traces” as illustrated in Figures 2, 5, and 6. (*Id.*, at 16.)

Defendants submit that the legal standard for indefiniteness as to a means-plus-function term is not whether the term is amenable to construction but rather is that “if no structure is disclosed, the claim is indefinite.” (Dkt. No. 145, at 17 (quoting *Halliburton Energy Servs., Inc. v. M-I LLC*, 514 F.3d 1244, 1256 n.7 (Fed. Cir. 2008)).) Defendants urge that although “[t]he claimed function requires three separate items to be combined: (1) the output signal from the vertical enlargement controller; (2) the output signal from the horizontal enlargement controller; and (3) the read clock,” “[t]he specification fails to disclose any structure that combines these

three.” (*Id.*) Defendants argue that although “Figures 2, 5, and 6 of the ’934 patent show these three inputs to a box labeled simply ‘combining,’” there is no disclosure of corresponding structure because “[c]learly, ‘combining’ is not a structure” and there are “no details as to the components of the circuit or the construction of the circuit.” (*Id.*, at 17 (citing ‘934 Patent at 4:6-12, 4:14-21 & 5:11-28).)

Defendants submit that Hitachi’s argument that “‘combining circuits’ were well-known in the art” is “an admission that the specification lacks sufficient disclosure.” (*Id.*, at 17.) Defendants emphasize that “consideration of the understanding of one skilled in the art in no way relieves the patentee of adequately disclosing sufficient structure in the specification.” (*Id.*, at 17-18 (quoting *Atmel Corp. v. Information Storage Devices, Inc.*, 198 F.3d 1374, 1380 (Fed. Cir. 1999); citing *Blackboard, Inc. v. Desire2Learn Inc.*, 574 F.3d 1371, 1385 (Fed. Cir. 2009)).)

Hitachi’s reply brief does not address this term. (*See* Dkt. No. 148.)

(2) Analysis

“If there is no structure in the specification corresponding to the means-plus-function limitation in the claims, the claim will be found invalid as indefinite.” *Biomedino, LLC v. Waters Techs. Corp.*, 490 F.3d 946, 950 (Fed. Cir. 2007). Further, “the written description must clearly link or associate structure to the claimed function.” *Telcordia Techs.*, 612 F.3d at 1376.

Claim 1 of the ‘934 Patent recites (emphasis added):

1. A television receiver capable of enlarging and compressing an image comprising:
 - a memory having a storage capacity not less than a given value which is controlled with at least a line period;
 - a clock generator generating a clock having a frequency not less than that of a write clock signal from a writing clock for writing a video signal in said memory and for outputting a read clock for reading said written video signal from said memory;

a vertical enlargement controller generating and outputting a signal for controlling said memory to repeatedly read the same line with a line period depending upon a first preset value when said video signal is read from said memory;

a horizontal enlargement controller generating and outputting a signal for controlling said memory to repeatedly read the same pixel from said memory with a predetermined pixel period depending upon a second preset value when said video signal is read from said memory;

means for combining the output signal from said vertical enlargement controller, the output signal from said horizontal enlargement controller and the read clock from said clock generator and for supplying said memory with a combined signal; to thereby provide a video signal representing an image which is compressed and enlarged in horizontal and vertical directions to a desired size as a video signal read from said memory.

Defendants argue that there is no corresponding structure for the claimed “means for combining” because the specification provides “no details as to the components of the circuit or the construction of the circuit.” (Dkt. No. 145, at 17.) Yet, the specification discloses that outputs from the clock generator, vertical enlargement controller, and horizontal enlargement controller are provided “via” the combining circuit 122:

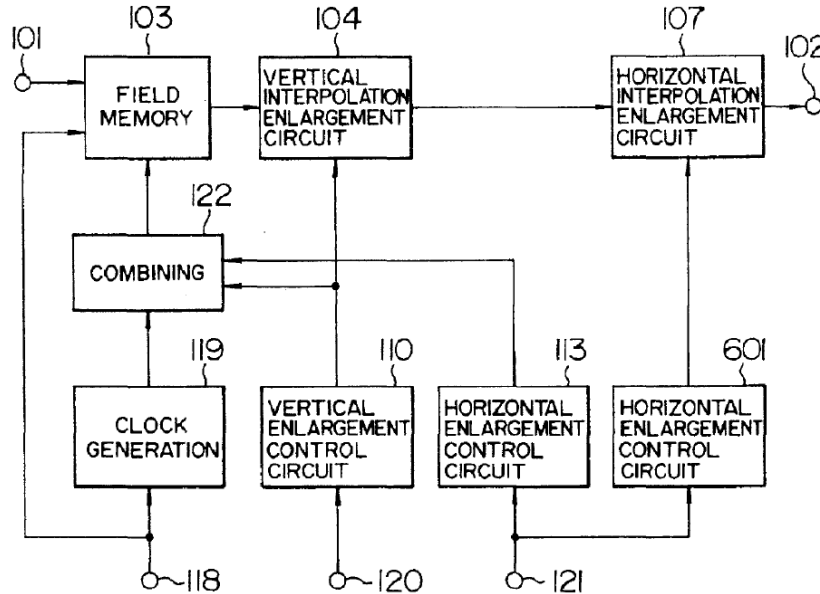
The clock generating circuit 119 generates a read clock having a frequency which is about 4/3 times as high as that of the input write clock and supplies it to the field memory 103 via the combining circuit 122. Accordingly, the video signal in which an image is compressed in a horizontal direction will be read from the field memory 103. The vertical enlarging control circuit 110 controls the field memory 103 via the combining circuit 122 for reading the video signal from the field memory 103 with a line period corresponding to a magnification factor.

* * *

Enlargement in a horizontal direction can be achieved in the same manner as the enlargement in a vertical direction. A delay control signal which is generated by the horizontal enlargement control circuit 113 is fed to the field memory 103 *via the combining circuit 122.*

(‘934 Patent at 4:9-18 & 5:11-15.) Figure 6 is illustrative and is reproduced here:

FIG. 6



Defendants emphasized at the October 23, 2012 hearing that although Figure 6, for example, shows multiple lines going into the combining circuit 122 and one line going from the combining circuit 122 to the field memory 103, the specification contains no disclosure of how the signals are combined.

On balance, the description and illustration of combining circuit 122 is sufficient. In particular, circuit diagrams or software coding details are not required for disclosure of corresponding structure for purposes of 35 U.S.C. § 112, ¶ 6. *See Intel Corp. v. VIA Techs., Inc.*, 319 F.3d 1357, 1365-67 (Fed. Cir. 2003) (finding that “core logic” was sufficient corresponding structure despite absence of disclosure of circuitry); *see also Tech Licensing Corp. v. Videotek, Inc.*, 545 F.3d 1316, 1338-39 (Fed. Cir. 2008); *S3 Inc. v. nVidia Corp.*, 259 F.3d 1364, 1370-71 (Fed. Cir. 2001). The Court therefore adopts Hitachi’s proposed construction.

The Court accordingly hereby finds that the term **“means for combining the output signal from said vertical enlargement controller, the output signal from said horizontal enlargement controller and the read clock from said clock generator and for supplying said memory with a combined signal”** is not indefinite, that the term is a means-plus-function term, that the claimed functions are **“(1) combining the output signal from said vertical enlargement controller, the output signal from said horizontal enlargement controller and the read clock from said clock generator; and (2) supplying said memory with a combined signal,”** and that the corresponding structure is **“combining circuit 112; and wiring or traces; and equivalents thereof.”**

L. “the output of said second register . . .” (‘934 Patent, Claim 6)

The disputed term is “the output of said second register is output as a signal controlling said memory and the pixel delay means to partially change the magnification rate of said image in a horizontal direction.”

The parties now agree that “[t]he phrase ‘to partially change the magnification rate of said image in a horizontal direction’ means ‘changing the magnification factor for part of the horizontal extent of the image.’” (Dkt. No. 150-1, 10/3/2012 Hitachi Patents JCCC, at 97.)

The Court therefore hereby adopts the parties’ agreed construction.

M. “line period” (‘934 Patent, Claim 1)

The parties now agree that this term means “a period of time for reading a line.” (Dkt. No. 150-1, 10/3/2012 Hitachi Patents JCCC, at 52.) The Court therefore hereby adopts the parties’ agreed construction.

N. “pixel period” (‘934 Patent, Claim 1)

The parties now agree that this term means “a period of time for reading a pixel.” (Dkt. No. 150-1, 10/3/2012 Hitachi Patents JCCC, at 87.) The Court therefore hereby adopts the parties’ agreed construction.

O. “preset value” (‘934 Patent, Claims 1-4)

The parties now agree that this term means “a number previously set to obtain a magnification factor.” (Dkt. No. 150-1, 10/3/2012 Hitachi Patents JCCC, at 81.) The Court therefore hereby adopts the parties’ agreed construction.

P. “display means for displaying the decoded program-associated information on a display screen” (‘995 Patent, Claim 1)

Hitachi’s Proposed Construction	Defendants’ Proposed Construction
Governed by § 112 ¶ 6 Function: “displaying the decoded program-associated information on a display screen” [agreed] Corresponding Structure: “a television screen or television display”	Governed by § 112 ¶ 6 Function: “displaying the decoded program-associated information on a display screen” [agreed] Corresponding Structure: “a television display (105) and an image multiplexer (104)”

(Dkt. No. 150-1, 10/3/2012 Hitachi Patents JCCC, at 98.)

The parties agree that this is a means-plus-function limitation, and the parties agree on the claimed function. The parties also agree that a “television display” is a corresponding structure.” The parties dispute whether a “television screen” can be an alternative corresponding structure and whether an “image multiplexer (104)” is also required as part of the corresponding structure.

(1) The Parties' Positions

Hitachi argues that “the terms ‘display screen,’ ‘television display,’ and ‘television display screen’ are used interchangeably, and are linked to the ‘displaying’ function in claim 1 of the ‘995 Patent.” (Dkt. No. 137, at 19-20 (citing ‘995 Patent at 1:10-17 & 2:4-6).) Hitachi argues that the “image multiplexer,” proposed as additional corresponding structure by Defendants, does not perform the recited function and therefore should not be identified as corresponding structure. (*Id.*, at 20.) Hitachi argues that a “multiplexer” is simply a device that combines two or more signal into a single signal and that “[t]here is no support in the specification to link the ‘image multiplexer’ to the function of ‘displaying.’” (*Id.*, at 20.)

Defendants respond that

the specification provides that “the image multiplexer 104 multiplexes the display data received from the display data setter 114 and the video signal received from the A/V decoder 103 and displays it on the television display 105.” [‘995 Patent] at 3:51-56. Thus, an image multiplexer (104) must be used together with the television display (105) to display “the decoded program-associated information on a display screen.”

* * *

Without the multiplexer, the program-associated information cannot be combined with the information that is being displayed on the display screen.

(Dkt. No. 145, at 19.)

Hitachi’s reply brief does not address this term. (*See* Dkt. No. 148.)

(2) Analysis

Claim 1 of the ‘995 Patent recites (emphasis added):

1. A broadcasting and communication receiver apparatus comprising:
receiver means for receiving program-associated information including a title, a start time, and an end time of a broadcast program together with a video signal and an audio signal;

decoder means for decoding the program-associated information from the received signal;

display means for displaying the decoded program-associated information on a display screen;

command receiver means for receiving an input signal from a remote controller or from a key or keys provided to a main body of the receiver apparatus; and

display controller means for controlling the display screen based on the input signal;

wherein a first display zone in which a plurality of character strings are displayed is provided in the display screen of the program-associated information; and

wherein the display controller means includes data quantity comparator means for comparing a magnitude of the first display zone with a quantity of display data and, when the display data quantity is judged to be larger than the first display zone, a displayable part of the character string of the display data as well as a symbol indicative of omission and attached to a last tail part of the character string are displayed.

The Description of the Preferred Embodiments discloses that the “image multiplexer 104” can be used to display video data and program-associated information on the television display at the same time (emphasis added):

FIG. 3 is a block diagram of a broadcasting and communication receiver apparatus in accordance with an embodiment of the present invention, which includes . . . a separator or demultiplexer 102 for extracting any one of video and audio signals and program-associated information signal from the received signal, a A/V decoder 103 for decoding the video and audio signals to reproduce original image and original audio, *an image multiplexer 104 for multiplexing the video signal and such graphics as characters*, a television display 105, a command receiver 106 for receiving a user input, an information decoder 107 for *decoding the transmitted program-associated information*, a program-associated information buffer 108 for holding therein the decoded program-associated information, a control micro-computer 110 containing the above elements 106 to 109, an input data amount calculator 111 for calculating the amount of display data received from the information buffer, displayable-data amount calculator 113 for calculating the number of character rows capable of being displayed on the display screen, a comparator 112 for comparing the amount of input data with the amount of displayable data, *a display data setter 114 for setting character rows to be displayed*, and a *display controller 109 containing the above elements 111 to 114 for controlling the image multiplexer*.

* * *

The display controller 109 controls the image multiplexer 104 in such a manner that the *image multiplexer 104 multiplexes the display data received from the display data setter 114 and the video signal received from the A/V decoder 103 and displays it on the television display 105.*

(’995 Patent at 3:1-26 & 3:51-56.)

“The corresponding structure to a function set forth in a mean-plus-function limitation must actually perform the recited function, not merely enable the pertinent structure to operate as intended.” *Asyst Tech., Inc. v. Empak, Inc.*, 268 F.3d 1364, 1371 (Fed. Cir. 2001). Here, the parties agree that the claimed function is “displaying the decoded program-associated information on a display screen.” Although the claim recites receiving a video signal in addition to receiving program-associated information, the agreed-upon function does not include multiplexing. Thus, although the image multiplexer 104 would be necessary for displaying the video signal and the program-associated information on the display screen at the same time, the image multiplexer 104 is not necessary for merely “displaying the decoded program-associated information on a display screen.”

Finally, as to Hitachi’s proposal that the phrases “television screen” and “television display” are used interchangeably in the ’995 Patent, on one hand Defendants’ response brief does not appear to object. (*See* Dkt. No. 145, at 18-19.) On the other hand, the phrase “television screen” appears nowhere in the ’995 Patent, which instead discloses a “television display screen” in two instances in the Background of the Invention. (’995 Patent at 1:14 & 2:6.) The corresponding structure should therefore be limited to the “television display 105” that is disclosed in the specification in connection with displaying the decoded program-associated information. (*See id.* at 3:1-26 & 3:51-56.)

The Court accordingly hereby finds that the term **“display means for displaying the decoded program-associated information on a display screen”** is a means-plus-function term, that the function is **“displaying the decoded program-associated information on a display screen,”** and that the corresponding structure is **“television display 105, and equivalents thereof.”**

Q. “a plurality of character strings” (‘995 Patent, Claim 1) and “the character string” (‘995 Patent, Claim 1)

Hitachi’s Proposed Construction	Defendants’ Proposed Construction
“two or more sets of characters,” alternatively, “two or more sets of letters, numbers, spaces, and/or punctuation marks”	“plurality of programs,” alternatively, “a plurality of any set of letters, numbers, spaces, and punctuation marks” “one of the plurality of character strings”

(Dkt. No. 150-1, 10/3/2012 Hitachi Patents JCCC, at 102.)

(1) The Parties’ Positions

Hitachi cites a dictionary definition as evidence of the “generally accepted meaning of ‘character string.’” (Dkt. No. 137, at 21 (citing Ex. 35, *Dictionary of Computing* 66 (3d ed. 1990) (TPV-10-260-0114123) (defining “character set” and “character string”).) Hitachi argues that Defendants’ proposed construction should be rejected because “character strings can also represent times and not just programs.” (*Id.*, at 21.) Hitachi also urges that the two disputed terms at issue, “a plurality of character strings” and “the character string,” should be given the same construction because, contrary to Defendants’ arguments, “the character string” has antecedent basis in “a plurality of character strings.” (*Id.*, at 20-21 n.3.)

Defendants respond that “[f]or example, in reference to Figure 6 [of the ‘995 Patent], a first program (*e.g.*, “pro-baseball relay broadcast”) is displayed in cell 401₂, a second program

(e.g., “movie”) is displayed in cell 401₃, etc.” (Dkt. No. 145, at 20.) Defendants also argue that the term “the character string” lacks antecedent basis and therefore should be construed to mean “one of the plurality of character strings.” (*Id.*) Defendants propose that “the first time the phrase ‘the character string’ is recited, it is referring to ‘one of the plurality of programs,’ and the second time it is recited, it is referring to ‘the one of the plurality of programs.’” (*Id.*)

Hitachi replies that “[c]onstruing ‘character string’ as a ‘program’ will confuse the jury” because “[a] ‘program’ is what you watch on the television, not the program-associated information at issue here.” (Dkt. No. 148, at 5.) Hitachi reiterates that “a character string is simply a ‘set of characters’ and is not a ‘program,’” and “[w]ith the definite article, ‘the character string’ becomes simply the particular ‘set of characters’ referred to in the final element of claim 1, *i.e.*, the character string which is partially displayed.” (*Id.*, at 6.)

As to Defendants’ proposal in its response brief that “character string” could be construed to mean “any set of letters, numbers, spaces, and punctuation marks,” “Hitachi would agree to this construction, except that a character string need not include a letter **and** a number **and** a space **and** a punctuation mark. Hitachi would agree to construing “character string” as “any set of letters, numbers, spaces, **and/or** punctuation marks.” (*Id.*)

At the October 23, 2012 hearing, Defendants agreed that using “and/or” in the construction would be acceptable.

(2) Analysis

Claim 1 of the ‘995 Patent recites, in relevant part (emphasis added):

1. A broadcasting and communication receiver apparatus comprising:
receiver means for receiving program-associated information including a title, a start time, and an end time of a broadcast program together with a video signal and an audio signal;

decoder means for decoding the program-associated information from the received signal;

display means for displaying the decoded program-associated information on a display screen;

command receiver means for receiving an input signal from a remote controller or from a key or keys provided to a main body of the receiver apparatus; and

display controller means for controlling the display screen based on the input signal;

wherein a first display zone in which a *plurality of character strings* are displayed is provided in the display screen of the program-associated information; and

wherein the display controller means includes data quantity comparator means for comparing a magnitude of the first display zone with a quantity of display data and, when the display data quantity is judged to be larger than the first display zone, a displayable part of *the character string* of the display data as well as a symbol indicative of omission and attached to a last tail part of *the character string* are displayed.

First, Hitachi properly argues that using the word “program” in the construction, as Defendants have proposed, would be confusing and potentially too narrow because the word “program” is commonly understood to refer to audio/video content that is viewed by a user. Defendants urged at the October 23, 2012 hearing that the relevant character string is a program title and not, for example, a program start time or end time. The claim, however, as quoted above, only recites “character string” and provides no basis for limiting the term to a program title. Defendants also urged that Hitachi’s proposed construction could be read to mean that individual words within a single program title could constitute a “plurality of character strings,” but here again, the claim does not require the character string to be a program title, let alone an entire program title. Defendants further cited prosecution history of a related patent application in which the patentee referred to a program title as a “character string.” (Dkt. No. 147, Ex. G, 9/29/2004 Amendment, at 13.) On balance, however, the patentee made no “definitive statements” in this regard, and Defendants have thus failed to establish a “clear and

unmistakable” waiver of any claim scope during prosecution. *Omega Eng’g*, 334 F.3d at 1325-26.

Second, the definite article “the” gives rise to a presumption that the term that follows has antecedent basis in an earlier recitation of the term. *NTP, Inc. v. Research In Motion, Ltd.*, 418 F.3d 1282, 1306 (Fed. Cir. 2005) (“[I]t is a rule of law well established that the definite article ‘the’ particularizes the subject which it precedes. It is a word of limitation as opposed to the indefinite or generalizing force of ‘a’ or ‘an.’”) (quoting *Warner-Lambert Co. v. Apotex Corp.*, 316 F.3d 1348, 1356 (Fed. Cir. 2003)). Nonetheless, the recitation of “the character string” in the singular, together with the context of the limitation in which it appears, quoted above, demonstrates that “the character string” refers to one or more of the “plurality of character strings.” In other words, the term “the character string” need not be read to refer to two or more character strings.

The Court therefore hereby construes the term **“plurality of character strings”** to mean **“two or more sets of letters, numbers, spaces, and/or punctuation marks.”** The Court also hereby construes the term **“the character string”** to mean **“one or more of the plurality of character strings.”**

R. “enabler/disabler means for selectively preventing said user adjustment control means from adjusting at least said portions of said displayed image containing said information image based on said control signal” (‘713 Patent, Claim 8)

Hitachi’s Proposed Construction	Defendants’ Proposed Construction
<p>Governed by § 112 ¶ 6</p> <p>Function: “selectively preventing said user adjustment control means from adjusting at least said portions of said displayed image containing said information image based on said control signal” [agreed]</p> <p>Corresponding Structure: “a changeover switch, a short-circuiting switch, or a bypass circuit”</p>	<p>Governed by § 112 ¶ 6</p> <p>Function: “selectively preventing said user adjustment control means from adjusting at least said portions of said displayed image containing said information image based on said control signal” [agreed]</p> <p>Corresponding Structure: “a changeover switch (13), or a changeover switch (13a) together with a bypass circuit (15)”</p>

(Dkt. No. 150-1, 10/3/2012 Hitachi Patents JCCC, at 112.)

The parties agree that this is a means-plus-function limitation, and the parties agree on the claimed function. The parties also agree that a “changeover switch” is part of the corresponding structure.” The parties dispute whether a “short-circuiting switch” and a “bypass circuit” (by itself) can be alternative corresponding structures.

(1) The Parties’ Positions

Hitachi cites the use of a “short-circuiting switch” in Figure 4 and the use of a “bypass circuit” in Figure 2. (Dkt. No. 137, at 21-22 (citing ‘713 Patent at 7:4-58, 8:28-63, Fig. 2 & Fig. 4).)

Defendants respond that Figure 2 of the ‘713 Patent illustrates that a bypass circuit must be used in conjunction with a changeover switch because bypassing of the adjustment circuit only occurs when the changeover switch has connected the bypass circuit to the output. (Dkt.

No. 145, at 22 (citing ‘713 Patent at 7:16-30 & Fig. 2).) As to the “short-circuiting switch,” Defendants respond that the function of the “short-circuiting switch” does not prevent adjustment from occurring but rather merely limits the adjustment range. Defendants conclude that the “short-circuiting switch” does not perform the claimed function of “selectively preventing” user adjustment. (*Id.*, at 23.)

Hitachi replies that “[a]lthough the Defendants’ changeover circuit is a means for selecting whether or not to prevent user control, it is the bypass circuit that does the preventing when selected.” (Dkt. No. 148, at 6.) Hitachi reiterates that “[a] structure merely enabling the recited function, not actually performing it, is not corresponding structure.” (*Id.* (citing *Asyst Tech.*, 268 F.3d at 1371).) Hitachi also replies that a “short-circuiting switch” is an alternative corresponding structure for performing the claimed function of “selectively preventing” because “[w]hen a user is ‘limited’ by the short-circuiting switch to making adjustments within a certain range . . . , that user can be said to have been ‘prevented’ from making adjustments outside of that range.” (*Id.*, at 7 (citing ‘713 Patent at 8:44-51).)

(2) Analysis

Claim 8 of the ‘713 Patent recites:

8. An image display apparatus comprising:
 - a display means for selectably displaying at least two of: a picture image without an information image; said information image without said picture image; and said picture image simultaneously with said information image;
 - a detection means for detecting a portion of said displayed image containing said information image and outputting a control signal according to said detected portion;
 - a user adjustment control means for allowing user adjustment of an image quality of a displayed image; and
 - an *enabler/disabler means for selectively preventing said user adjustment control means from adjusting at least said portions of said displayed image containing said information image based on said control signal.*

The parties only dispute the corresponding structure for this means-plus-function term, and their dispute is centered on Figures 1-5 of the '713 Patent. Figure 1 is reproduced here:

FIG. 1

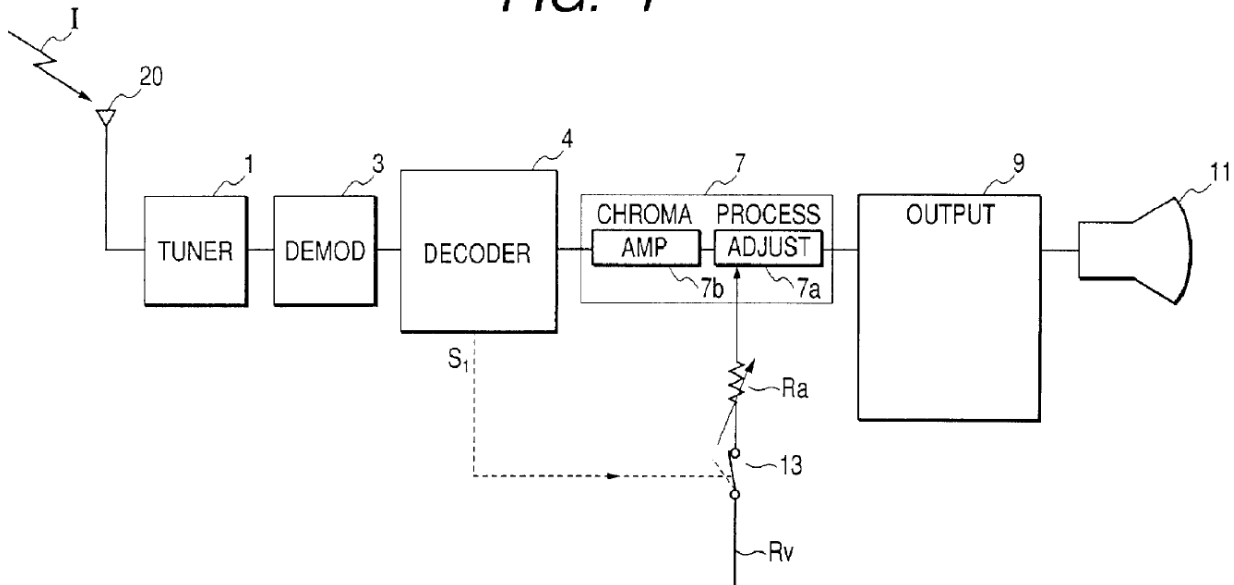


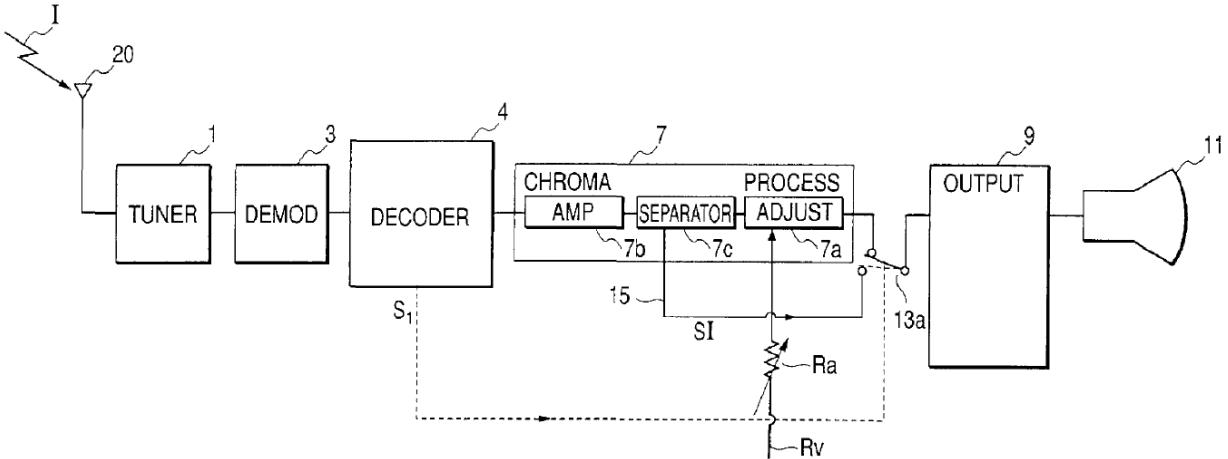
Figure 1 thus illustrates an embodiment in which a “changeover switch 13” enables or disables user control of color density and luminance (by way of “Rv” and “Ra” in Figure 1). (See ‘713 Patent at 6:15-57.) The “changeover switch 13” is therefore one alternative corresponding structure.

As to Figure 2, the specification discloses:

In the above construction, when an on-off signal S_1 is on (e.g., at a high-level) indicating a superposed period detected in the digital decoder 4 under timing control . . . , the changeover switch 13a is switched to the lower side shown by a dashed line in FIG. 2, such that the bypass circuit 15 is connected to the output device 9, and only an SI [(service information)] signal is input to the output device 9 via the bypass circuit 15 and switch 13a. Therefore, the SI signal bypasses the adjustment circuit 7a so as not to be adjusted thereby, and a display of an SI signal thus is not disadvantageously affected by the adjustment circuit 7a, e.g., a menu, EPG [(electronic program guide)] or PPV [(pay-per-view)] information is never rendered unreadable and/or never disappears.

(‘713 Patent at 7:16-30.) Figure 2 is reproduced here:

FIG. 2



Because the agreed-upon function requires “*selectively preventing,*” bypass circuit 15 together with the changeover switch 13a—which *selects* the circuit path through the bypass circuit 15—is another alternative corresponding structure.

Figures 3 and 5 are similar to Figure 1 in terms of the changeover switch. (*See* ‘713 Patent at 7:66-8:27, 8:64-9:25, Fig. 3 & Fig. 5.) Thus, the changeover switch 13b and changeover switch 13d illustrated in those Figures are also alternative corresponding structures. (*See id.*)

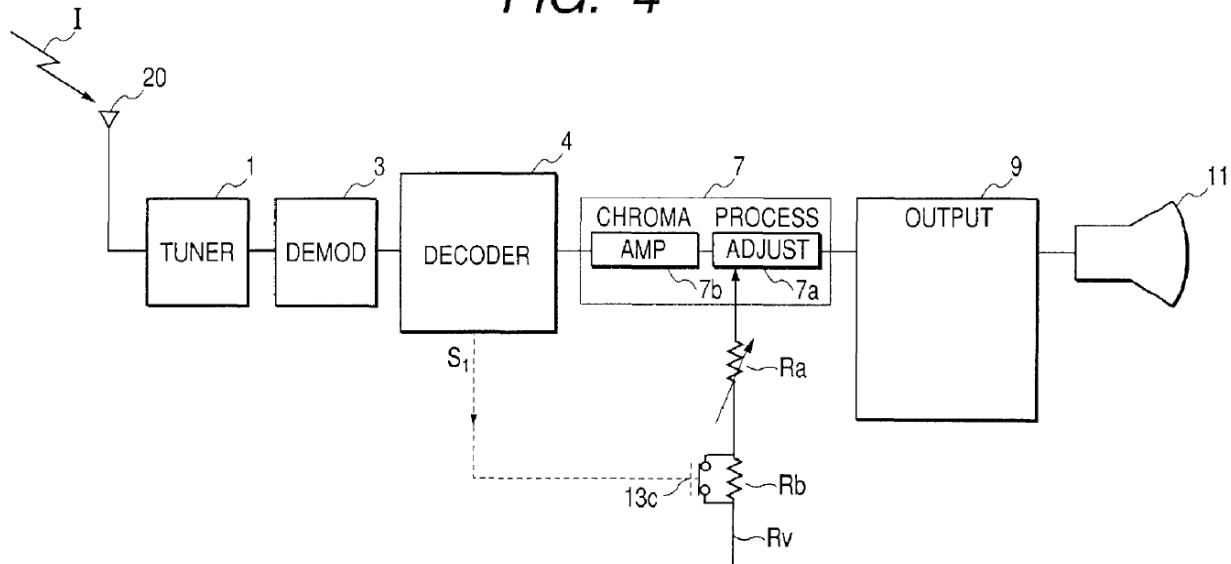
As to Figure 4, the specification discloses:

More particularly, if the above on-off signal S_1 , is on (e.g., at a high level, and indicative of superposition), the short-circuiting switch 13c is switched to the left side shown by a dashed line in FIG. 4. That is, is switched to an unconnected (or non-shunting) position, and the adjustment part R_a and the fixed part R_b operate in a series combination. Therefore, the adjustment range of the image quality adjusting circuit 7a is limited by the series combination of the adjustment part R_a and the fixed part R_b . With such arrangement, the series combination is chosen

such that degradation of superposed information images on a screen by the adjustment of image quality is never caused.

(‘713 Patent at 8:44-51.) Figure 4 is reproduced here:

FIG. 4



Thus, the short-circuiting switch 13c is another alternative corresponding structure for “selectively preventing” user adjustment.

The Court hereby finds that the term “**enabler/disabler means for selectively preventing said user adjustment control means from adjusting at least said portions of said displayed image containing said information image based on said control signal**” is a means-plus-function term, that the claimed function is “**selectively preventing said user adjustment control means from adjusting at least said portions of said displayed image containing said information image based on said control signal,**” and that the corresponding structure is “**(1) changeover switch 13, changeover switch 13b, short-circuiting switch 13c,**

or changeover switch 13d, and equivalents thereof; or (2) bypass circuit 15 together with changeover switch 13a, and equivalents thereof.”

S. “enabler/disabler” (‘713 Patent, Claim 1)

Hitachi’s Proposed Construction	Defendants’ Proposed Construction
“a circuit or switch that enables or disables an operation”	“a switching circuit that enables and disables an operation”

(Dkt. No. 150-1, 10/3/2012 Hitachi Patents JCCC, at 111.)

(1) The Parties’ Positions

Hitachi’s opening arguments are responsive to Defendants’ original proposal that the disputed term be construed to mean a “changeover switch (13).” (Dkt. No. 137, at 22; *see* Dkt. No. 127, Ex. B, 8/17/2012 Parties’ Proposed Constructions of Disputed Terms, at 12.) Hitachi argued that Defendants’ proposed construction should be rejected as an attempt to limit the term to a preferred embodiment. (Dkt. No. 137, at 22.)

In their response brief, Defendants’ propose that the disputed term be construed to mean “a switching circuit that enables and disables operation.” (Dkt. No. 145, at 23.) Defendants note that unlike the similar term in Claim 8 of the ‘713 Patent, discussed in subsection IV.R., above, “enabler/disabler” in Claim 1 is not recited in means-plus-function format. (*Id.*) Defendants nonetheless argue that “[a]lthough the ‘enabler/disabler’ is not necessarily limited to the corresponding structures in the specification and their equivalents, the enabler/disabler cannot encompass any ‘circuit’ that performs the recited function, as Hitachi argues.” (*Id.* (citing *Halliburton Oil Well Cementing Co. v. Walker*, 329 U.S. 1 (1946); *LizardTech, Inc. v. Earth Resource Mapping, Inc.*, 424 F.3d 1336 (Fed. Cir. 2005)).)

Defendants further urge that Hitachi’s proposed construction should be rejected because it would encompass a device that can enable *or* disable. (*Id.*, at 24.) Defendants submit that “[t]he recited function necessarily requires that the ‘enabler/disabler’ both enable *and* disable,” which “is consistent with the specification, wherein each embodiment that prevents user adjustment includes a changeover switch that switches between two states—an ‘on’ state and an ‘off’ state.” (*Id.* (citing ’713 Patent at 6:32-57).) Defendants conclude that “the enabler/disabler must be adapted to ‘select’ between a prevention state and a non-prevention state.” (*Id.*)

Hitachi replies that Defendants’ proposal of “switching circuit” is too narrow because “[t]he specification describes both circuits and switches.” (Dkt. No. 148, at 7.) Finally, Hitachi argues that Defendants’ proposal of “enables *and* disables” is improper because “in at least one embodiment of the invention, the user adjustment is normally enabled,” and “[i]n that case, the enabler/disabler only serves to disable user adjustment control, not to enable it.” (*Id.* (citing ’713 Patent at 7:48-58).)

(2) Analysis

Claim 1 of the ’713 Patent recites (emphasis added):

1. An image display apparatus comprising:
 - a display circuit adapted to selectably display at least two of: a picture image without an information image; said information image without said picture image; and said picture image simultaneously with said information image;
 - a detector which detects a portion of said displayed image containing said information image and outputs a control signal according to said detected portion;
 - a user adjustment control circuit allowing user adjustment of an image quality of a displayed image; and
 - an *enabler/disabler* adapted to selectively prevent said user adjustment control circuit from adjusting at least said portions of said displayed image containing said information image based on said control signal.

Hitachi relies upon the following disclosure as evidence that the “enabler/disabler” need only be able to disable (emphasis added):

FIG. 9 is exemplary of a situation wherein user adjustment is enabled for a major portion of a displayed image, while being disabled for sub-portion of a displayed image, such sub-portion corresponding to an image information portion of the displayed image. More particularly, a display 900 illustrates a picture image 902 being superposed by an information image 906 window. In this embodiment, the *user adjustment circuit is normally enabled*, unless a predetermined situation is encountered. More particularly, vertical periods 920 and horizontal periods 930 are detected using any well know window period detection method. Such vertical periods 920 and horizontal periods 930 are then used, e.g., via combination with an AND gate, to determine periods when the user adjustment circuit should be disabled. Thus, *while the user adjustment circuit is normally enabled during a majority of image display, the user adjustment circuit would be disabled during the information image 906 window.*

(‘713 Patent at 7:48-58.) Hitachi’s argument fails because even the above-quoted disclosure relied upon by Hitachi necessarily involves a circuit that can both enable and disable.

Defendants’ proposal of a circuit that can “enable and disable” is consistent with the above-quoted passage as well as the disclosure cited by Defendants:

The function of the high definition display unit constituted as described above will be described below. More particularly, in the high definition display unit, an on-off signal S_1 indicative of superposed/non-superposed periods of a PI [(picture information)] signal and an SI [(service information)] signal is detected under timing control in the digital decoder 4. As described above, the *changeover switch 13* is provided within the user control circuit connected to the image quality adjusting circuit 7a in the video chroma processing circuit 7 via an adjustment part Ra. *If the above on-off signal S_1 is on* (e.g., at a high level) indicating both signals are presently superposed, the above *switch 13 is operated on the left side in FIG. 1 (i.e., is opened) such that the user control circuit is disabled* to prevent the density of a color, hue and luminance of superposed signals from being controlled by user control. Since user control (i.e., adjustment) of image quality is thus temporarily disabled, image quality is performed at a predetermined level (e.g., preset within the adjustment circuit 7a) rather than at a user-adjusted level, so as to guarantee a viewability of the image information (i.e., menu, EPG or PPV). If the above on-off signal S_1 is off (e.g., at a low-level) indicating both signals are not presently superposed, the above *switch 13 is operated on the right side in FIG. 1 (i.e., is closed) and the user control*

arrangement is enabled to allow the density of a color and luminance to be controlled by normal user control.

(’713 Patent at 6:32-57.) The specification thus discloses that an enabler/disabler is something that switches between enabled and disabled. Including the term “switching” as Defendants have proposed, however, would imply a requirement of a switch, which is not a limitation of the claim and which should not be imported from the disclosed embodiments.

The Court therefore hereby construes “**enabler/disabler**” to mean “**a circuit that enables and disables an operation.**”

T. “said displayed image” (’713 Patent, Claims 1 & 8)

Hitachi’s Proposed Construction	Defendants’ Proposed Construction
“an image for display by the display circuit” (claim 1) or “an image for display by the display means” (claim 8)	“an image displayed on a display” (claim 1) or “an image displayed on the display means” (claim 8)

(Dkt. No. 150-1, 10/3/2012 Hitachi Patents JCCC, at 116.)

(1) The Parties’ Positions

Hitachi argues that because “Claims 1 and 8 each contain an ‘enabler/disabler’ that prevents a user adjustment control circuit from adjusting certain portions of ‘said displayed image’” *before* it is displayed, “Defendants’ construction would necessarily exclude the preferred embodiments and is improper.” (Dkt. No. 137, at 23 (citation omitted).)

Defendants respond that the constituent term “displayed” in the disputed term appears in the past tense. (Dkt. No. 145, at 24 (citing *Modavox, Inc. v. Tacoda, Inc.*, 607 F. Supp. 2d 530, 535 (S.D.N.Y. Mar. 24, 2009) (“While ‘embedded’ functions as an adjective in the patents . . . that adjective derives from a verb that is in the past tense, thereby suggesting that the act of

embedding the code module has already occurred.”)). Defendants also cite disclosure that “FIG. 9 is exemplary of a situation wherein user adjustment is enabled for a major portion of a *displayed image*, while being disabled for sub-portion of a *displayed image*, such sub-portion corresponding to an image information portion of *the displayed image*,” wherein adjustments are made to the “displayed image,” past tense. (*Id.*, at 25 (quoting ‘713 Patent at 7:41-45).)

Defendants also note that the first limitation of Claim 1 of the ‘713 recites “display[ing]” in the present tense whereas the remaining three limitations recite “said displayed image” in the past tense.” (*Id.*) Defendants conclude that “[r]egardless of whether the proper interpretation of claim language renders the claim nonsensical or inoperable, the Court may not disregard the claim language.” (*Id.* (citing *Haemonetics Corp. v. Baxter Healthcare Corp.*, 607 F.3d 776, 780 (Fed. Cir. 2010); *Chef Am., Inc. v. Lamb-Weston, Inc.*, 358 F.3d 1371, 1374 (Fed. Cir. 2004)).)

Hitachi replies that “Defendants cannot credibly argue that an image can be adjusted after it has already been displayed, and any fair reading of the specification reveals that the embodiments describe processing of the picture image and information image prior to their being output for display.” (Dkt. No. 148, at 8 (citing ‘713 Patent at 6:30-31 (“an image is *thus* formed with the display 11”) & 7:25-28 (“Therefore, the SI signal bypasses the adjustment circuit 7a so as not to be adjusted thereby, and a display of an SI signal *thus* is not disadvantageously affected by the adjustment circuit”))). Finally, Hitachi submits that “the only images described previously in claim 1 that provide antecedent basis for ‘said displayed image’ are the picture/information image combination described in the first element that the display circuit is ‘to . . . display.’” (*Id.*)

(2) Analysis

Claims 1 and 8 of the '713 Patent recite (emphasis added):

1. An image display apparatus comprising:
a display circuit adapted to selectably display at least two of: a picture image without an information image; said information image without said picture image; and said picture image simultaneously with said information image;
a detector which detects a portion of *said displayed image* containing said information image and outputs a control signal according to said detected portion;
a user adjustment control circuit allowing user adjustment of an image quality of *a displayed image*; and
an enabler/disabler adapted to selectively prevent said user adjustment control circuit from adjusting at least said portions of *said displayed image* containing said information image based on said control signal.

* * *

8. An image display apparatus comprising:
a display means for selectably displaying at least two of: a picture image without an information image; said information image without said picture image; and said picture image simultaneously with said information image;
a detection means for detecting a portion of *said displayed image* containing said information image and outputting a control signal according to said detected portion;
a user adjustment control means for allowing user adjustment of an image quality of *a displayed image*; and
an enabler/disabler means for selectively preventing said user adjustment control means from adjusting at least said portions of *said displayed image* containing said information image based on said control signal.

On one hand, the past tense of “displayed” suggests an image that has already been displayed. *Modavox*, 607 F. Supp. 2d at 535. On the other hand, the specification discloses that a “displayed image” can be adjusted or varied by the user:

More particularly, the object is to provide a high definition display unit which can prevent or limit a video chroma adjustment circuit from significantly adjusting an image quality of information image portions of a displayed image, such that an information image is never significantly degraded and/or rendered unviewable. ('713 Patent at 2:29-35.)

* * *

As mentioned above, the invention is directed toward avoiding a situation where user adjustment of an image quality (e.g., color density, hue, and/or brightness) of a displayed image renders image (e.g., menu selection) information unviewable. (*Id.* at 3:49-53.)

* * *

As shown in FIG. 1 . . . a reference number Ra denotes an adjusting section circuit adjusted by a user (i.e., so as to vary an image quality of a displayed image) (*Id.* at 4:38-46.)

* * *

However, in order to avoid a situation where user adjustment can disadvantageously degrade a viewing quality of displayed image information (e.g., a menu, an EPG and/or PPV information), a changeover switch 13 is provided relative to the user control (i.e., adjustment) circuit, and is automatically operated according to the on-off signal S₁ which is indicative of whether or not the PI and SI signals are superposed or not. (*Id.* at 6:18-26.)

* * *

FIG. 9 is exemplary of a situation wherein user adjustment is enabled for a major portion of a displayed image, while being disabled for sub-portion of a displayed image, such sub-portion corresponding to an image information portion of the displayed image. (*Id.* at 7:41-45.)

On balance, because an image that has already been displayed cannot then be adjusted, construing “said displayed image” as “an image to be displayed” is appropriate in light of both the claim language and the specification.

The Court accordingly hereby construes “said displayed image” in both Claim 1 and Claim 8 of the ‘713 Patent to mean **“an image to be displayed.”**

U. “said selection menu” (‘713 Patent, Claims 6, 13 & 20)

The parties now agree that “said selection menu” means “said EPG or PPV selection menu.” (Dkt. No. 150-1, 10/3/2012 Hitachi Patents JCCC, at 118.) The Court therefore hereby adopts the parties’ agreed construction.

V. “display means for selectably displaying . . .” (‘713 Patent, Claim 8)

The disputed term is “display means for selectably displaying at least two of: a picture image without an information image; said information image without said picture image; and said picture image simultaneously with said information image.”

The parties now agree that this term should be construed as follows:

Governed by [35 U.S.C.] § 112 ¶ 6

Function:

“selectably displaying at least two of: a picture image without an information image; said information image without said picture image; and said picture image simultaneously with said information image”

Corresponding Structure:

a cathode ray tube (or CRT), a display, or a screen

(Dkt. No. 150-1, 10/3/2012 Hitachi Patents JCCC, at 120.) The Court therefore hereby adopts the parties’ agreed construction.

W. “user adjustment control means for allowing user adjustment of an image quality of a displayed image” (‘713 Patent, Claims 8, 9, 10 & 13)

The parties now agree that the term “user adjustment control means for allowing user adjustment of an image quality of a displayed image” should be construed as follows:

Governed by § 112 ¶ 6

Function:

“allowing user adjustment of an image quality of a displayed image”

Corresponding Structure:

an adjusting section circuit (Ra) and an image quality adjusting circuit (7a)

(Dkt. No. 150-1, 10/3/2012 Hitachi Patents JCCC, at 121.) The Court therefore hereby adopts the parties’ agreed construction.

X. “first selector” (‘412 Patent, Claim 1)

The parties now agree that the term “first selector” should be construed to have its “[p]lain and ordinary meaning.” (Dkt. No. 150-1, 10/3/2012 Hitachi Patents JCCC, at 124.) The Court therefore hereby adopts the parties’ agreed proposal that the term “first selector” be construed to have its plain and ordinary meaning.

Y. “to thereof” (‘412 Patent, Claim 1)

The disputed term is “to thereof” in the phrase “a vertical scaling unit performing third local signal processing of compression and expansion in a vertical direction to thereof.”

Hitachi’s Proposed Construction	Defendants’ Proposed Construction
“to the signal selected by the first selector”	“to the signal scaled by the horizontal scaling unit”

(Dkt. No. 150-1, 10/3/2012 Hitachi Patents JCCC, at 125.)

(1) The Parties’ Positions

Hitachi submits that “[t]he parties’ dispute determines whether the claim requires horizontal scaling to be performed before vertical scaling.” (Dkt. No. 137, at 27.) In other words, the issue is whether “to thereof” refers to the selected signal—which may or may not have already been horizontally scaled—or to the signal that has already been horizontally scaled.

Hitachi argues that ““a signal selected by a first selector’ provides the antecedent basis for the latter appearing ‘to thereof.’” (*Id.*)

Defendants respond that “[t]he claim language sets forth a specific order of operation.” (Dkt. No. 145, at 26.) Defendants emphasize that “the horizontal scaling unit performs ‘second’ local signal processing to the signal selected by the first selector. Next, the vertical scaling unit performs ‘third’ local signal processing (i.e., after the ‘second’ local signal processing occurs) to the signal just processed by the horizontal scaling unit.” (*Id.*, at 26-27.)

Hitachi replies that the terms “second” and “third” in the claim “are merely used to distinguish between the different processing functions and do not prescribe an order.” (Dkt. No. 148, at 8.)

(2) Analysis

Claim 1 of the ‘412 Patent recites (emphasis added):

1. A circuit for signal processing of format conversion of picture signal which performs signal processing of converting a format of an input picture signal into a predetermined display format of a picture output device, said circuit comprising:
 - a scanning convertor for performing first local signal processing of converting the input picture signal into a picture signal of progressive scanning when the input picture signal is of interlace scanning;
 - a first selector for selecting either one of the input picture signal and the picture signal of progressive scanning outputted from the scanning convertor;
 - a scaling unit comprising a horizontal scaling unit for performing second local signal processing of compression and expansion in a horizontal direction to a signal selected by the first selector and a vertical scaling unit performing third local signal processing of compression and expansion in a vertical direction *to thereof*; and
 - a control unit for selecting parameters of the signal processing in accordance with the format of the input picture signal and the display format of the picture output device and controlling at least the scanning convertor, the first selector and the scaling unit in accordance with the parameters of the signal processing.

Claim 1 thus does not specify the signal to which “thereof” refers. The specification discloses “a scaling unit for performing signal processing of scaling in horizontal and vertical directions in

respect of an output signal from the selector.” (‘412 Patent at 2:30-32.) In the disclosed embodiments, scaling can be performed in either order:

[T]he horizontal scaling is performed preferably prior to the vertical scaling and in the converse case, the vertical scaling is preferably performed prior to the horizontal scaling.

* * *

Further, it is preferable in view of simplifying signal processing to provide the horizontal scaling unit 5 on the input side of the vertical scaling unit 6 when horizontal compression ($K > L$) is performed and provide the horizontal scaling unit 5 on the output side of the vertical scaling unit 6 when horizontal expansion ($K < L$) is performed.

(*Id.* at 2:58-64 & 7:4-9.) The specification thus explains that horizontal and vertical scaling can be performed in any order, depending on the particular implementation and circumstances.

Finally, the use of “second” and “third” in the claim does not refer to an order of steps but rather merely distinguishes between multiple instances of signal processing. *See 3M Innovative Properties Co. v. Avery Dennison Corp.*, 350 F.3d 1365, 1371 (Fed. Cir. 2004) (“The use of the terms ‘first’ and ‘second’ is a common patent-law convention to distinguish between repeated instances of an element or limitation.”). Defendants’ proposed construction, which would require that horizontal scaling occur before vertical scaling, should therefore be rejected.

The Court accordingly hereby construes “**to thereof**” to mean “**to the signal selected by the first selector.**”

Z. “parameters of the signal processing” (‘412 Patent, Claim 1) and “signal processing parameters” (‘412 Patent, Claim 15)

Hitachi’s Proposed Construction	Defendants’ Proposed Construction
Plain and ordinary meaning. Alternatively, “controls for signal processing.”	“switch settings for the first, second, and third local signal processing” (claim 1) “switch settings” (claim 15)

(Dkt. No. 150-1, 10/3/2012 Hitachi Patents JCCC, at 126.)

Shortly before the October 23, 2012 hearing, the parties agreed that these terms should be construed to have their plain and ordinary meaning.

The Court accordingly hereby construes the terms “**parameters of the signal processing**” and “**signal processing parameters**” to have their plain and ordinary meaning.

AA. “motion coefficient of picture” (‘412 Patent, Claim 3)

Hitachi’s Proposed Construction	Defendants’ Proposed Construction
“a coefficient of motion of the picture to be displayed”	“coefficient of the motion of the entire picture to be displayed”

(Dkt. No. 150-1, 10/3/2012 Hitachi Patents JCCC, at 130.)

(1) The Parties’ Positions

Hitachi submits that when generating a progressive video signal from an interlaced video signal, “[t]he ‘412 invention detects the amount of motion, generates one or more motion coefficients K for the picture, and uses those coefficients to optimally vary the ratio of interfield and intrafield interpolation.” (Dkt. No. 137, at 29.) Intrafield interpolation, which is also known as “spatial” interpolation, uses neighboring lines from the same field (that is, from the same image). Intrafield interpolation is better for reproducing video of relatively fast-moving objects. Interfield interpolation, which is also known as “temporal” interpolation, uses the same line from

one or more neighboring fields, such as the previous field or the next field. Interfield interpolation is better for reproducing video of relatively slow-moving objects.

Hitachi argues that whereas Defendants' proposal would improperly limit the disputed term to a single coefficient for "the entire picture," Hitachi's proposal would properly allow for multiple coefficients for a single picture. (*Id.*, at 30.) Hitachi submits that the claim uses the indefinite article, "a," which is well-established to mean "one or more." (*Id.*)

Defendants respond that "[d]espite Hitachi's assertions, neither the specification nor the claims describe more than one motion coefficient." (Dkt. No. 145, at 29.) Defendants argue that because "the specification describes it as an absolute value," "the inventors clearly intended to limit the motion coefficient to a single coefficient – 'an absolute value' – that represents the entire picture." (*Id.*)

Hitachi replies that there may be "separate calculations for different areas within the picture." (Dkt. No. 148, at 10). Hitachi also argues that the use of "an absolute value" is irrelevant because "'absolute value' is a mathematical term that simply means that the sign of the value is ignored." (*Id.*) "For example, regardless of whether a ball is moving in the picture from left to right ('+' direction) at a speed of +3 or from right to left ('-' direction) with a speed of -3, the absolute value is '3.'" (*Id.*) Hitachi submits that this "has nothing to do with whether there is a single motion coefficient for the entire picture." (*Id.*)

(2) Analysis

Claim 3 of the '412 Patent recites (emphasis added):

3. A circuit for signal processing of format conversion of picture signal according to claim 2, wherein the first convertor comprises:
 - a motion detector for detecting *a motion coefficient of picture* of the input picture signal;

a circuit for constituting a first interpolation signal and a second interpolation signal by performing an intrafield calculation and an interfield calculation respectively to the input picture signal; and

a circuit for providing the interpolation scanning line signal by varying a mixture ratio of the first interpolation signal and the second interpolation signal by the motion coefficient.

The indefinite article “a,” when it appears in a claim, generally means “one or more.”

Baldwin Graphic Sys., Inc. v. Siebert, Inc., 512 F.3d 1338, 1342-43 (Fed. Cir. 2008).

The specification, however, discloses a “motion coefficient K” that is used to combine interfield and intrafield interpolation to varying respective degrees depending on the amount of motion in a picture:

A motion coefficient setting unit 18 sets a motion information coefficient having a value from 0 to 1 in accordance with an absolute value of the differential signal, that is, a magnitude of motion of picture. A MAX selecting unit 19 sets a final motion coefficient K by also using motion information of previous 1 field to avoid motion detection miss. That is, a maximum value is detected between a signal of motion of previous 1 field formed by delaying a signal at a field memory FD3 that are multiplied by a coefficient α ($0 < \alpha < 1$) at a coefficient product unit 20 and the motion information coefficient, and the maximum value is outputted as the final motion coefficient K ($0 \leq K \leq 1$, stationary: $K=0$). Thus the MAX selecting unit 19 constitutes a motion detector. Coefficient product units 15 multiply the interpolation signal suitable for moving picture and the interpolation signal suitable for stationary picture by coefficients K and $1 - K$ respectively, and an adder 16 forms a luminance signal SI(Y) of the interpolation scanning line signal SI by adding the both multiplied signals.

(‘412 Patent at 7:59-8:16.) Thus, the above-quoted passage discloses a single motion coefficient,

“K,” for the entire picture.

Nonetheless, the general rule that “a” means “one or more” should be applied in light of the primacy of the claims and the related principles set forth in *Phillips*:

[A]lthough the specification often describes very specific embodiments of the invention, we have repeatedly warned against confining the claims to those embodiments. . . . In particular, we have expressly rejected the contention that if a patent describes only a single embodiment, the claims of the patent must be

construed as being limited to that embodiment. . . . That is not just because section 112 of the Patent Act requires that the claims themselves set forth the limits of the patent grant, but also because persons of ordinary skill in the art rarely would confine their definitions of terms to the exact representations depicted in the embodiments.

Phillips, 415 F.3d at 1323 (citations omitted); *Renishaw*, 158 F.3d at 1248 (“[T]he claims define the scope of the right to exclude; the claim construction inquiry, therefore, begins and ends in all cases with the actual words of the claim.”).

The Court therefore hereby construes **“motion coefficient of picture”** to mean **“one or more coefficients of motion of the picture to be displayed.”**

V. CONSTRUCTION OF AGREED TERMS IN THE “VIZIO” PATENTS

The parties have submitted the following agreed-upon constructions for terms in the VIZIO Patents, which the Court hereby adopts:

Term	Agreed Construction
U.S. Patent No. 5,511,096	
“means for receiving and demodulating convolutionally encoded output symbols from a communication path”	<p><u>Function</u>: receiving and demodulating convolutionally encoded output symbols from a communication path.</p> <p><u>Corresponding Structure</u>: receiver 28 and demodulator 31.</p>
U.S. Patent No. 5,621,761	
“AND gate”	No construction necessary – this should be given its plain and ordinary meaning.
“exclusive OR gate”	No construction necessary – this should be given its plain and ordinary meaning.

U.S. Patent No. 5,703,887	
“means for replacing the parity code in each packet with an MPEG synchronization pattern”	<p><u>Function</u>: replacing the parity code in each packet with an MPEG synchronization pattern</p> <p><u>Corresponding Structure</u>: sync byte and error flag insertion circuit 94</p>
U.S. Patent No. 5,745,522	
“means for multiplying an N-bit pseudorandom output from said LFSR by an N-bit value f_k that is an element of said finite field”	<p><u>Function</u>: multiplying an N-bit pseudorandom output from said LFSR by an N-bit value f_k that is an element of said finite field</p> <p><u>Corresponding Structure</u>: constant term α^3 designated by box 60 in Figure 4 as implemented by exclusive OR-gates 100, 102 and 104 and connections 106, 108, and 110 in Figure 5.</p>
“exclusive OR gate”	No construction necessary – this should be given its plain and ordinary meaning.
U.S. Patent No. 5,396,518	
“means for digitizing received QAM symbols to provide digital data representative of orthogonal in-phase (I) and quadrature-phase (Q) components of said symbols”	<p><u>Function</u>: digitizing received QAM symbols to provide digital data representative of orthogonal in-phase (I) and quadrature-phase (Q) components of said symbols</p> <p><u>Corresponding Structure</u>: A/D (analog-to-digital converter) 30</p>
“means for convolutionally reencoding said recovered information stream at a punctured rate n/k of a binary convolutional code when n/k is less than one to provide a stream of successive two bit symbol group identifiers, each identifier representing a best estimate of a symbol group of said QAM constellation that partially identifies received QAM symbol”	<p><u>Function</u>: convolutionally reencoding said recovered information stream at a punctured rate n/k of a binary convolutional code when n/k is less than one to provide a stream of successive two bit symbol group identifiers, each identifier representing a best estimate of a symbol group of said QAM constellation that partially identifies a received QAM symbol</p> <p><u>Corresponding Structure</u>: punctured rate n/k reencoder 44</p>

<p>“means for multiplexing the sliced (N-2) uncoded bit portions with the information stream recovered in said second receiver path to reconstruct a desired data stream”</p>	<p><u>Function</u>: multiplexing the sliced (N - 2) uncoded bit portions with the information stream recovered in said second receiver path to reconstruct a desired data stream</p> <p><u>Corresponding Structure</u>: multiplexer 52</p>
<p>“means for delaying said digital data by $D/(2n/k)$ symbols, where D is substantially the delay inherent in said second receiver path”</p>	<p><u>Function</u>: delaying said digital data by $D/(2n/k)$ symbols, where D is substantially the delay inherent in said second receiver path</p> <p><u>Corresponding Structure</u>: delay buffer 34</p>
<p>“means for further quantizing said digital data”</p>	<p><u>Function</u>: further quantizing said digital data</p> <p><u>Corresponding Structure</u>: I/Q quantizer 32</p>
<p>U.S. Patent No. 5,233,629</p>	
<p>“means for demodulating a received carrier to recover an N-bit QAM modulation function in which a two-bit codeword identifies one of a plurality of QAM constellation subsets and the remaining (N-2) bit portion represents a signal point within said one subset”</p>	<p><u>Function</u>: demodulating a received carrier to recover an N-bit QAM modulation function in which a two-bit codeword identifies one of a plurality of QAM constellation subsets and the remaining (N- 2) bit portion represents a signal point within said one subset</p> <p><u>Corresponding Structure</u>: receiver 28</p>
<p>“decoder means for using said metrics in an algorithm for decoding a rate $\frac{1}{2}$ binary conventional code to recover a first bit”</p>	<p>No construction necessary – this should be given its plain and ordinary meaning.</p>
<p>“means for combining the selected subgroup with the recovered first bit to provide a decoded output”</p>	<p><u>Function</u>: combining the selected subgroup with the recovered first bit to provide a decoded output</p> <p><u>Corresponding Structure</u>: serializer 76</p>

(Dkt. No. 126, 8/17/2012 Joint Claim Construction and Pre-Hearing Statement Regarding VIZIO Patents, at 2-4.)

VI. CONSTRUCTION OF DISPUTED TERMS IN THE “VIZIO” PATENTS

The VIZIO Patents all relate to “Quadrature Amplitude Modulation” (“QAM”) and are therefore sometimes referred to as the “QAM Patents.” Background regarding QAM is discussed in subsection I.B., above. The parties note that the VIZIO Patents have been construed during the course of proceedings at the International Trade Commission (“ITC”), Investigation No. 337-TA-789, entitled “Certain Digital Televisions and Components Thereof” (the “ITC Investigation”), presided over by Chief Administrative Law Judge Charles E. Bullock. Judge Bullock entered a claim construction order on March 1, 2012. (Dkt. No. 143, Ex. A (“ITC Order”).)

VIZIO argues that the constructions reached in the ITC Order “were contrary to Federal Circuit law and relied in-part on contradictory extrinsic evidence.” (Dkt. No. 142, at 1.) Hitachi responds that the claim constructions in the ITC Order were the culmination of two rounds of briefing and oral argument on the VIZIO Patents and should be highly persuasive. (Dkt. No. 143, at 2.) In general, prior claim construction proceedings involving the same patents-in-suit are “entitled to reasoned deference under the broad principals of *stare decisis* and the goals articulated by the Supreme Court in *Markman*, even though *stare decisis* may not be applicable *per se*.” *Maurice Mitchell Innovations, LP v. Intel Corp.*, No. 2:04-CV-450, 2006 WL 1751779, at *4 (E.D. Tex. June 21, 2006). The Court therefore considers the analysis by the ITC but has ultimately conducted an independent review of the disputed terms.

Hitachi has also submitted the Expert Declaration of Dr. Todd Moon in Support of Hitachi’s Claim Construction, in order to “further explain the pertinent technology and

supplement the Technology Tutorial.” (Dkt. No. 143, at 1 (citing 9/19/2012 Moon Decl., Dkt. No. 144-6).)

A. “means for deinterleaving the recovered blocks” (‘096 Patent, Claim 22)

VIZIO’s Proposed Construction	Hitachi’s Proposed Construction
Function: “deinterleaving the recovered blocks” [agreed] Corresponding structure: “deinterleaver”	Function: “deinterleaving the recovered blocks” [agreed] Corresponding structure: “deinterleaver / stripper 34”

(Dkt. No. 150-2, 10/3/2012 Joint Claim Construction Chart for VIZIO Patents (“VIZIO Patents JCCC”), at 3.)

The parties agree that this is a means-plus-function limitation, and the parties agree upon the claimed function. The parties dispute the corresponding structure.

(1) The Parties’ Positions

Hitachi submits that “[t]he dispute between the parties is whether the corresponding structure for the ‘means for deinterleaving’ in claim 22 is the specific structure disclosed in the specification and in Figure 1 as ‘DEINTERLEAVER AND STRIPPER’ 34, as Hitachi contends, or whether it is a generic ‘deinterleaver’ as Vizio contends.” (Dkt. No. 143, at 6.)

VIZIO argues that “Hitachi’s construction incorrectly requires an additional structure (‘stripper’) that does not actually perform the claimed function.” (Dkt. No. 142, at 21.) In particular, VIZIO submits that deinterleaving occurs after the optional step of stripping the control bits, if any, out of the blocks. (*Id.*, at 22 (citing ’096 Patent at 4:32-34, 5:55-57, 8:15-23, 8:56-58 & 10:6-10).)

Hitachi responds that it has proposed the same construction adopted by the ITC Order, which relied upon “the specification repeatedly stat[ing] that the deinterleaver and stripper are combined in a single structure: deinterleaver/stripper 34.” (Dkt. No. 143, at 6 (quoting ITC Order, at 35).) Hitachi quotes from the specification that “[t]he decoded output from decoder 32 is input to a *deinterleaver and control symbol stripper 34* that strips out the control symbols (if provided) and reverses the effects of interleaver 18 discussed above.” (*Id.*, at 6-7 (quoting ‘096 Patent at 8:55-58; citing ‘096 Patent at Fig. 1).)

Hitachi concludes that “[t]he fact that the ‘deinterleaver and stripper 34’ may also perform additional unclaimed functions (*e.g.*, stripping) does not change the fact that it is the only structure clearly linked to performing the claimed function.” (*Id.*, at 7.) Hitachi further points to the ITC Order’s reliance on Claim 24, which recites “said deinterleaving means deinterleaver [*sic*] the recovered blocks after stripping said control symbols therefrom.” (*Id.* (quoting ITC Order, at 36).) Thus, Hitachi argues that “[t]he fact that it may also perform a stripping function is irrelevant, and indeed fully consistent with dependent claim 24.” (*Id.*, at 8.)

As to VIZIO’s proposed construction, Hitachi urges that the disclosure in the specification of “deinterleaver 34” is actually a reference to the “deinterleaver and stripper 34” of Figure 1, as denoted by the reference numeral “34.” (*Id.*)

VIZIO replies that the ‘096 Patent “includes another preferred embodiment in which the decoded output does not include control symbols” and in which “further processing of the decoded output” is done “by deinterleaver 34 . . .” (Dkt. No. 149, at 1 (citing ‘096 Patent at 9:15-10:15).) VIZIO submits that “in this embodiment, block 34 from Figure 1 describes only a ‘deinterleaver 34.’” (*Id.*) VIZIO concludes that because only the deinterleaver is required to

perform the claimed function, the corresponding structure is only the deinterleaver. (*Id.* (citing *Wenger Mfg., Inc. v. Coating Mach. Sys., Inc.*, 239 F.3d 1225, 1233 (Fed. Cir. 2001) (noting that the court may not import “structural limitations from the written description that are unnecessary to perform the claimed function”)).)

(2) Analysis

“[S]tructure disclosed in the specification is “corresponding” structure only if the specification or prosecution history clearly links or associates that structure to the function recited in the claim.” *B. Braun Med., Inc. v. Abbott Labs.*, 124 F.3d 1419, 1424 (Fed. Cir. 1997).

The ITC relied upon disclosure in the specification of a combined “deinterleaver and stripper 34” as well as on the doctrine of claim differentiation as applied to Claim 24:

Claim 24, which depends from claim 22, sheds light on the meaning of claim 22, reciting that “said deinterleaving means deinterleaver the recovered blocks after stripping said control symbols therefrom.” (‘096 patent at 18:31-33.) Here, the claim states that the stripping function is an additional limitation that is not found in independent claim 22, but it refers to the “deinterleaving means” as the structure that performs that function. *See Unidynamics Corp. v. Automatic Products Intern., Ltd.*, 157 F.3d 1311, 1320 (Fed. Cir. 1998). That is, the deinterleaver recovers the blocks, but *said deinterleaver* first strips the control[] symbols, requiring that the deinterleaving means is a deinterleaver/stripper. (‘096 patent at 18:31-33.)

(ITC Order, at 36.)

On balance, the ITC Order is persuasive. Further, the portion of the specification on which VIZIO relies discloses that “further processing of the decoded output, by *deinterleaver 34* and a Reed-Solomon outer decoder 36 (*FIG. 1*) is used to recover the original information bits.” (‘096 Patent at 10:8-10 (emphasis added)). Although VIZIO argued at the October 23, 2012 hearing that “FIG. 1” in this passage is cited only for the Reed-Solomon outer decoder 36, a more natural reading is that Figure 1 is cited for both reference numerals 34 and 36. Figure 1, in

turn, discloses a “deinterleaver and stripper” block labeled with reference numeral 34, as reproduced here:

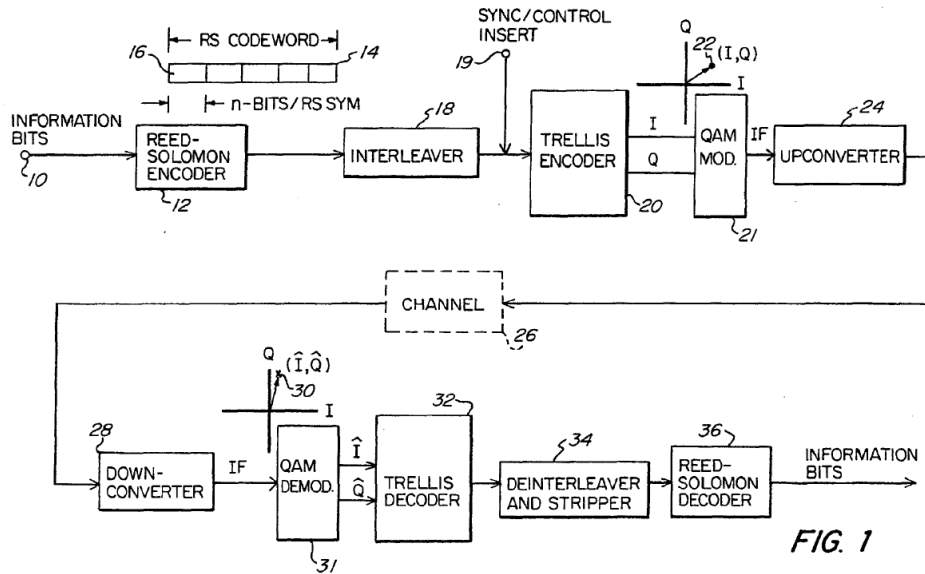


FIG. 1

The patentee, having elected to use a means-plus-function claim format, provided a single corresponding structure, namely the “deinterleaver and stripper 34” illustrated in Figure 1 and described in the specification. The disputed term should be construed accordingly.

The Court therefore hereby finds that “**means for deinterleaving the recovered blocks**” is a means-plus-function term, that the function is “**deinterleaving the recovered blocks,**” and that the corresponding structure is “**deinterleaver and stripper 34, and equivalents thereof.**”

B. “the recovered blocks” (’096 Patent, Claim 22)

VIZIO’s Proposed Construction	Hitachi’s Proposed Construction
<p>No construction necessary – this should be given its plain and ordinary meaning.</p> <p>If the Court finds construction is necessary, the term should be construed to mean: “blocks of coded symbols recovered by the inner decoder.”</p>	<p>“blocks comprising coded symbols as recovered by the inner decoder”</p>

(Dkt. No. 150-2, 10/3/2012 VIZIO Patents JCCC, at 2-3.)

(1) The Parties' Positions

VIZIO argues that this “is a self-contained term for which the claim language provides a clear meaning.” (Dkt. No. 142, at 4.) VIZIO also submits that if the Court finds that construction is necessary, then VIZIO’s alternative proposed construction is consistent with the specification. (*Id.* (citing ‘096 Patent at 18:3-12).)

In response, “[t]o narrow the issues for the Court, Hitachi seeks to have the Court simply adopt Judge Bullock’s construction [in the ITC Order], which was included within Hitachi’s original proposed construction.” (Dkt. No. 143, at 8.) Hitachi submits that because the term “the recovered blocks” refers back to an earlier limitation for antecedent basis, Hitachi “seeks construction of ‘the recovered blocks’ to clarify that the ‘blocks’ that are deinterleaved by the ‘means for deinterleaving’ are the same ‘blocks’ that are recovered by the ‘inner decoder.’” (*Id.*, at 9.) Hitachi argues that VIZIO’s proposed construction, by contrast, “fails to clarify the disputed term.” (*Id.*)

VIZIO replies that Hitachi’s insertion of the word “as” is “an attempt to preclude any intermediary steps between the inner decoder and the deinterleaver. Such a construction adds a limitation to the claim that is not present in the claim language,” VIZIO argues, and is improper because “this claim uses the transitional phrase ‘comprising’ which provides for an open-ended claim.” (Dkt. No. 149, at 1-2 (citing *Mars, Inc. v. R.J. Heinz Co.*, 377 F.3d 1369, 1376 (Fed. Cir. 2004)).)

(2) Analysis

Although VIZIO proposes that the disputed term need not be construed, the parties have presented a “fundamental dispute regarding the scope of a claim term,” and the Court has a duty to resolve that dispute. *O2 Micro*, 521 F.3d at 1362-63.

Claim 22 recites (emphasis added):

22. A decoder for multilevel modulated digital data communicated in a standard bandwidth television channel comprising:
 means for receiving and demodulating convolutionally encoded output symbols from a communication path;
 an inner decoder for decoding the demodulated output symbols using a rate 4/5 code to *recover interleaved blocks of data*, each block comprising N seven-bit coded symbols of which M coded symbols represent information to be recovered and the remaining N-M coded symbols comprise error correcting overhead, wherein an outer symbol error correcting rate M/N is one of rates 120/126, 121/127, and 122/128;
 means for deinterleaving the recovered blocks; and
 an outer symbol error decoder concatenated with said inner decoder for decoding the blocks from said inner decoder to recover a transmitted information signal.

The parties agree in principle that the term “the recovered blocks” has an antecedent basis recited earlier in the claim.

The ITC Order construed “the recovered blocks” to mean “blocks comprising coded symbols as recovered by the inner decoder,” which was the proposal by the respondents in the ITC Investigation. (*See* ITC Order, at 36-38.) Hitachi proposes the same construction here, but the ITC Order did not specifically address the use of the word “as” in the respondents’ proposal. (*See id.*)

On balance, VIZIO properly notes that the word “as” in Hitachi’s proposed construction might be read to preclude any intermediate processing. Hitachi has shown no persuasive support for such a limitation, and the Court finds none. The antecedent basis required by the word “the”

in the term “the recovered blocks” is satisfied so long as “the recovered blocks” are the same blocks recovered by the inner decoder, even if the blocks are modified by some intermediate processing.

The Court therefore adopts the construction reached in the ITC Order except for the word “as.” The Court accordingly hereby construes “**the recovered blocks**” to mean “**blocks comprising coded symbols recovered by the inner decoder.**”

C. “puncture map of {1 0 0 0 / 1 1 1 1}” (‘082 Patent, Claims 1 and 2)

VIZIO’s Proposed Construction	Hitachi’s Proposed Construction
“representation of bits to be punctured wherein three out of every four bits in a first path are repetitively deleted while no bits in a second path are deleted”	“puncturing pattern of {1000/1111}, progressing from the top left-most bit in the puncture pattern to the bottom right most bit in the puncture map and aligning the top-leftmost bit with the first output bit, where the output bits are aligned with the zeros in the pattern are deleted and the bits aligned with the ones are not deleted”

(Dkt. No. 150-2, 10/3/2012 VIZIO Patents JCCC, at 1.)

The disputed term is “puncture map of

$$\left\{ \begin{array}{c} 1000 \\ 1111 \end{array} \right\},$$

but for convenience the disputed term is referred to herein and by the parties as “puncture map of {1 0 0 0 / 1 1 1 1}.”

(1) The Parties’ Positions

VIZIO argues that Hitachi’s proposed construction improperly limits the disputed term to “one example within the specification for demonstrating the operation of the puncture logic.”

(Dkt. No. 142, at 17 (citing '082 Patent at 3:66-4:15).) VIZIO urges that the context preceding the disclosure cited by Hitachi demonstrates that “the puncture map is applied to the bit streams on a bit-by-bit basis” such that “[c]ontrary to the suggestion made in Hitachi’s construction, the puncture logic does not wait for a group of 8 bits to be output before puncturing that block of bits.” (*Id.*, at 18 (citing '082 Patent at 3:45-65).) VIZIO concludes that “[w]hich bits are removed is irrelevant and merely a function of time, as shown above.” (*Id.*, at 19.)

Hitachi responds that “the specific pattern claimed is represented by the ‘puncture map of {1 0 0 0 / 1 1 1 1}” and that “[e]very repeating set of eight input bits (four from each path) is punctured and output as a single stream in this manner.” (Dkt. No. 143, at 10.) Hitachi argues that VIZIO’s attempt to encompass puncture maps of {0 1 0 0 / 1 1 1 1}, {0 0 1 0 / 1 1 1 1}, and {0 0 0 1 / 1 1 1 1} should be rejected because “[t]he starting point and ending point of the puncture map are critical because, at the receive end, a corresponding decoder will then rely on the same puncture pattern to account for the deleted bits.” (*Id.*, at 11.) Hitachi submits that the ITC Order reached this conclusion, as well, and found that

one of ordinary skill would understand that claim 1 covers a single puncture map that must be applied as disclosed in the specification, *i.e.*, from the top left-most bit to the bottom right-most bit and aligning the top left most bit with the first output bit. Vizio’s construction is improper because it conflicts with the intrinsic evidence and encompasses additional puncture maps that were not claimed or disclosed in the '082 patent.

(*Id.*, at 12 (quoting ITC Order, at 48).)

Hitachi also emphasizes disclosure that “[a] block diagram of a rate 4/5 convolutional encoder *in accordance with the present invention* is shown in FIG. 1.” (*Id.*, at 13 (quoting '082 Patent at 3:35-4:2 (emphasis added); citing *C.R. Bard, Inc. v. U.S. Surgical Corp.*, 388 F.3d 858, 864 (Fed. Cir. 2004) (“Statements made that describe the invention as a whole, rather than

statements that describe only preferred embodiments, are more like to support a limited definition of a claim term.”)).) Hitachi argues that “Vizio’s contention that ‘the puncture map is applied to the bits streams on a bit-by-bit basis’ is both unsupported and irrelevant.” (*Id.*, at 14.) Hitachi submits that VIZIO’s proposed construction is “incomplete because it completely omits the order in which the puncture map is to be read, as explicitly stated in the ’082 patent.” (*Id.*, at 14-15.)

VIZIO replies that the order proposed by Hitachi “is simply a preferred embodiment and nothing in the specification indicates that it is the only order for applying the claimed puncture map.” (Dkt. No. 149, at 2.) In other words, VIZIO argues, “Hitachi attempts to limit the term ‘puncture map’ further by introducing an aspect of timing that does not exist anywhere in the specification.” (*Id.*, at 3.) As to Hitachi’s argument regarding decoding, VIZIO replies that:

It is true that on the receive end, the decoder will rely on the same puncture pattern, i.e., it will rely on the fact that 3 out of every 4 bits from the top row were deleted and all the bits of the bottom row were kept. This is the puncture pattern. Beyond that, the decoder does not care about the starting or ending points (i.e., timing) of the bit stream.

(*Id.*, at 3.) VIZIO explains that because “[t]he receiver does not know which bits came from the top row or which bits came from the bottom,” the receiver “must discern this information by aligning itself with the data,” such that the puncture map could be any of {1 0 0 0 / 1 1 1 1}, {0 1 0 0 / 1 1 1 1}, {0 0 1 0 / 1 1 1 1}, or {0 0 0 1 / 1 1 1 1}, depending on where in the stream the receiver picks up the signal. (*Id.*, at 4.) VIZIO reiterates that all that is necessary to decode the punctured stream is to know that “3 out of every 4 bits from the top row are deleted and all of the bottom bits are kept.” (*Id.*)

(2) Analysis

Claim 1 of the '082 Patent is representative and recites:

1. A method for convolutionally encoding digital data with a rate 4/5 convolutional code, comprising the steps of:
 - puncturing a rate 1/2, sixteen state convolutional code based on octal generators 25,37 to rate 4/5 using a puncture map of { 1 0 0 0 / 1 1 1 1 } wherein $v=4$;⁴ and
 - processing an incoming data stream using said rate 4/5 code.

Claim 1 does not recite puncturing in which three out of every four bits in a first path are repetitively deleted while no bits in a second path are deleted, as VIZIO here proposes. Instead, Claims 1 and 2 of the '082 Patent recite a specific puncture map, and as found by the ITC Order, the specification explains the operational significance of that specific puncture map. (ITC Order, at 48.) The Court therefore adopts the analysis and conclusion of the ITC Order.

The Court accordingly hereby construes **“puncture map of {1 0 0 0 / 1 1 1 1}”** to mean **“puncturing pattern of {1 0 0 0 / 1 1 1 1}, progressing from the top left-most bit in the puncture pattern to the bottom right most bit in the puncture pattern and aligning the top-leftmost bit with the first output bit, where the output bits aligned with the zeros in the pattern are deleted and the output bits aligned with the ones are not deleted.”**

D. “means for puncturing” (‘082 Patent, Claim 2)

The full disputed term is “means for puncturing the code from said rate 1/2 encoder to rate 4/5 using the puncture map of {1 0 0 0 / 1 1 1 1}, wherein $v=4$.”

⁴ In the phrase “wherein $v=4$,” “ v ” is the Greek letter “Nu,” which refers to the number of “state bits” associated with the convolutional coder. (See '082 Patent at 1:20-22 (“The memory of the encoder is characterized by its state, which is represented as a v -bit binary number.”).)

VIZIO’s Proposed Construction	Hitachi’s Proposed Construction
Function: “puncturing the code from said rate 1/2 encoder to rate 4/5 using a puncture map of { 1000/1111 } wherein v=4” [agreed] Corresponding structure: “puncture logic”	Function: “puncturing the code from said rate 1/2 encoder to rate 4/5 using a puncture map of { 1000/1111 } wherein v=4” [agreed] Corresponding structure: “indefinite”

(Dkt. No. 150-2, 10/3/2012 VIZIO Patents JCCC, at 2.)

The parties agree that this is a means-plus-function limitation, and the parties agree upon the claimed function. The parties dispute whether the specification of the ‘082 Patent discloses sufficient corresponding structure to satisfy the requirements of 35 U.S.C. § 112.

(1) The Parties’ Positions

VIZIO argues that the disclosure of “puncture logic 28” in the specification is sufficient corresponding structure. (Dkt. No. 142, at 23-24 (citing ‘082 Patent at 3:57-65 & Fig. 1).)

Hitachi responds that the disclosure of “puncture logic” cited by VIZIO is “merely a paraphrase of ‘puncture means’ and does not connote any specific structure.” (Dkt. No. 143, at 16 (citing *Ergo Licensing, LLC v. Carefusion 303, Inc.*, 673 F.3d 1361, 1364 (Fed. Cir. 2012)).) That is, Hitachi argues that “‘puncture logic’ is depicted as a functional block and is described in purely functional terms.” (*Id.* (citing ‘082 Patent at 3:57-4:21, 5:29-41 & Fig. 1).) Hitachi also relies upon the opinion of its expert, Dr. Todd Moon, that a person of ordinary skill in the art would understand that the claimed function could be carried out using various different types of structures, none of which are disclosed in the specification. (*Id.*, at 17 (citing Dkt. No. 144-6, 9/19/2012 Moon Decl., at ¶¶ 42-45).)

VIZIO replies that “the Federal Circuit has held that logic modified to perform a specific function is adequate structure.” (Dkt. No. 149, at 4 (citing *Intel*, 319 F.3d at 1365-66).) VIZIO argues that “[t]he specification describes logic modified to puncture a code by applying a puncture map” and “identifies a specific way of applying the puncture map to a code.” (*Id.* (citing ‘082 Patent at 3:57-4:21 & Fig. 1).) VIZIO further argues that the *Ergo Licensing* case cited by Hitachi is distinguishable because here “the specification describes exactly how the puncture map is applied.” (*Id.*, at 5 (citing 673 F.3d 1361).) Finally, VIZIO urges that Dr. Moon’s opinions “should be ignored” because “[a]s the Federal Circuit has stated, ‘when the intrinsic evidence is unambiguous, it is improper for a court to rely on extrinsic evidence such as expert testimony when construing disputed claim terms.’” (*Id.* (quoting *CAE Screenplates v. Heinrich Fiedler GmbH & Co. Kg*, 224 F.3d 1308, 1318 (Fed. Cir. 2000)).)

(2) Analysis

Indefiniteness is a “legal conclusion that is drawn from the court’s performance of its duty as the construer of patent claims.” *Exxon Research & Eng’g Co. v. U.S.*, 265 F.3d 1371, 1376 (Fed. Cir. 2001) (citation omitted). A finding of indefiniteness must overcome the statutory presumption of validity. *See* 35 U.S.C. § 282. That is, the “standard [for finding indefiniteness] is met where an accused infringer shows by clear and convincing evidence that a skilled artisan could not discern the boundaries of the claim based on the claim language, the specification, and the prosecution history, as well as her knowledge of the relevant art area.” *Halliburton Energy Servs., Inc. v. M-I LLC*, 514 F.3d 1244, 1249-50 (Fed. Cir. 2008).

In determining whether that standard is met, i.e., whether the claims at issue are sufficiently precise to permit a potential competitor to determine whether or not he is infringing, we have not held that a claim is indefinite merely because it poses a difficult issue of claim construction. We engage in claim construction

every day, and cases frequently present close questions of claim construction on which expert witnesses, trial courts, and even the judges of this court may disagree. Under a broad concept of indefiniteness, all but the clearest claim construction issues could be regarded as giving rise to invalidating indefiniteness in the claims at issue. But we have not adopted that approach to the law of indefiniteness. We have not insisted that claims be plain on their face in order to avoid condemnation for indefiniteness; rather, what we have asked is that the claims be amenable to construction, however difficult that task may be. If a claim is insolubly ambiguous, and no narrowing construction can properly be adopted, we have held the claim indefinite. If the meaning of the claim is discernible, even though the task may be formidable and the conclusion may be one over which reasonable persons will disagree, we have held the claim sufficiently clear to avoid invalidity on indefiniteness grounds. . . . By finding claims indefinite only if reasonable efforts at claim construction prove futile, we accord respect to the statutory presumption of patent validity . . . and we protect the inventive contribution of patentees, even when the drafting of their patents has been less than ideal.

Exxon, 265 F.3d at 1375 (citations and internal quotation marks omitted).

The ITC Order did not address the “means for puncturing” term. On one hand, Hitachi’s expert, Dr. Moon, opines that “[t]here are several ways that a person of ordinary skill could accomplish [puncturing], including:

- Using a microprocessor configured so that the outputs of a convolutional encoder $b_{n,1}$, $b_{n,2}$ are input to the process, and output data is provided to shift register 30, with program code written in accordance with the description of the function of the puncture logic in the patent.
- Using an application-specific integrated circuit (ASIC) designed to accept the outputs of a convolutional encoder $b_{n,1}$, $b_{n,2}$ and to output data to shift register 30.
- Using a field-programmable gate array (FPGA) to perform the functionality.
- Using a programmable read-only memory (PROM), with additional timing and register logic.

- Using custom designed circuitry for implementation using small-scale integrated circuits, such as TTL⁵ gates and registers.

(Dkt. No. 144-6, 9/19/2012 Moon Decl., at ¶ 45.) “That ordinarily skilled artisans could carry out the recited function in a variety of ways is precisely why claims written in ‘means-plus-function’ form must disclose the particular structure that is used to perform the recited function.” *Blackboard, Inc. v. Desire2Learn Inc.*, 574 F.3d 1371, 1385 (Fed. Cir. 2009); *see Ergo Licensing*, 673 F.3d at 1363-64 (finding that “recitation of ‘control device’ provides no more structure than the term ‘control means’ itself, rather it merely replaces the word ‘means’ with the generic term ‘device’”).

On the other hand, “puncture logic” is disclosed in the specification in the following two passages (emphasis added):

In order to convert the rate 1/2 code of the convolutional encoder 12 to a rate 4/5 code, *puncture logic 28* is provided. The *puncture logic* uses a puncture map { 1 0 0 0 / 1 1 1 1 } such that the bits output from convolutional encoder 12 which align with the zeros in the puncture map are deleted. *Puncture logic 28* applies the puncture map to the bits $b_{n,1}$; $b_{n,2}$ in a pattern progressing from the top left-most bit in the puncture map to the bottom right-most bit in the puncture map, progressing from left to right and from top to bottom. Thus, for bits a_1 , a_2 , a_3 and a_4 input to terminal 10 of the convolutional encoder 12, bits { $b_{1,1}$ $b_{2,1}$ $b_{3,1}$ $b_{4,1}$ / $b_{1,2}$ $b_{2,2}$ $b_{3,2}$ $b_{4,2}$ } will be output and puncture pattern { 1 0 0 0 / 1 1 1 1 } will result in the output from puncture logic 28 of bits $b_{1,1}$; $b_{1,2}$; $b_{2,2}$; $b_{3,2}$; and $b_{4,2}$.

Puncture logic 28 will load the five output bits $b_{1,1}$; $b_{1,2}$; $b_{2,2}$; $b_{3,2}$; and $b_{4,2}$ into a shift register 30 for output in a sequential order. Thus, for each four bits input to terminal 10, five bits will be output from shift register 30 as a result of the rate 4/5 code punctured from the rate 1/2 convolutional encoder 12.

* * *

The *puncture logic* for the new rate 3/4 and rate 6/7 codes is illustrated in FIGS. 3 and 4, respectively. In FIG. 3, *puncture logic 28a* outputs selected bits to shift register 30a in accordance with puncture map { 1 0 0 / 1 1 1 }. In FIG. 4,

⁵ “TTL” presumably refers to transistor-transistor logic, the details of which are not relevant here.

puncture logic 28b outputs selected bits to shift register 30b in accordance with puncture map { 1 0 0 0 1 0 / 1 1 1 1 0 1}.

(‘082 Patent at 3:57-4:21 & 5:29-40.) The specification thus discloses that the puncture logic 28 receives inputs, applies the puncture map from left to right and top to bottom, and produces outputs. This disclosure is sufficient, as has been found by the Court of Appeals for the Federal Circuit in analogous circumstances involving “core logic”:

The core logic, as described in the specification and adapted both to write directly and to react to WBF# [(write buffer full)], is the structure corresponding to the two functions recited in claim 1.

...

We hold that the [patent-in-suit] is not indefinite merely because no specific circuitry is disclosed to show the modification.

* * *

A generic description of the core logic, as adapted to practice Fast Write pursuant to the specification, is not inadequate solely because no circuitry is disclosed on how to modify the core logic.

* * *

[The challenger] also argues that claim 1 is indefinite because there may be unlimited numbers of implementations that can modify the core logic to perform the recited functions and the patent does not disclose circuitry or other structure on any of the implementations so the universe of such implementations is undefined. We disagree.

* * *

By analogy, if a chair is disclosed in the specification that corresponds to the “means for seating” limitation in a claim, asserting that there are infinite numbers of structures that could make a chair or there are unlimited types of chairs in the world would not necessarily make the claim indefinite.

Intel, 319 F.3d at 1365-67. Thus, by analogy, the disclosure of the “puncture logic” as the “means for puncturing” is like the disclosure of a chair as a “means for seating.” *Id.* Though

there may be various ways to implement the “puncture logic,” the above-quoted disclosure of “puncture logic” in the specification is sufficient corresponding structure to satisfy 35 U.S.C. § 112, ¶ 6.

The Court accordingly hereby finds that **“means for puncturing”** is a means-plus-function term, that the term is not indefinite, that the function is **“puncturing the code from said rate 1/2 encoder to rate 4/5 using a puncture map of { 1 0 0 0 / 1 1 1 1 } wherein v=4,”** and that the corresponding structure is **“puncture logic 28, and equivalents thereof.”**

E. “a(x)” & “b(x)” (‘887 Patent, Claim 22)

VIZIO’s Proposed Construction	Hitachi’s Proposed Construction
<p>No construction necessary – this should be given its plain and ordinary meaning.</p> <p>If the Court finds construction is necessary, the term should be construed to mean:</p> <p>a(x): “a polynomial that can equal 1 as long as b(x) is not equal to 1 at the same time”</p> <p>b(x): “a polynomial that can equal 1 as long as a(x) is not equal to 1 at the same time”</p>	<p>“a polynomial having a value other than 1 and representing a function for a filter that provides a finite impulse response”</p>

(Dkt. No. 150-2, 10/3/2012 VIZIO Patents JCCC, at 5-6.)

(1) The Parties’ Positions

VIZIO emphasizes disclosure in the specification that a(x) can equal 1, which VIZIO notes is still a polynomial because a(x)=1 can be represented as a(x)=x⁰. (Dkt. No. 142, at 7 & n.4.) VIZIO argues that “the Court should reject Hitachi’s proposed construction because such a construction reads the preferred embodiment out of the asserted claims and flies in the face of the overwhelming intrinsic evidence.” (Dkt. No. 142, at 7.) VIZIO also argues that the ITC Order

erred by finding “a disclaimer in the prosecution history where no such disclaimer exists” and by “ignor[ing] the mountain of intrinsic evidence shown above and instead chos[ing] to rely upon extrinsic evidence in the form of expert testimony.” (*Id.*, at 9.)

During prosecution, the examiner rejected Claim 22 as anticipated by the “Bruekheimer” reference, United States Patent No. 5,367,544, and the examiner stated that Bruekheimer disclosed an embodiment where $a(x) = 1$ and $b(x) = x^{n-k-1}$. VIZIO submits that the patentee argued that Bruekheimer was distinguishable on three grounds, none of which were that $a(x)$ could not equal 1. (*Id.*, at 9-10.)

Hitachi responds that “a person of ordinary skill would have also understood that when ‘ $a(x)$ ’ or ‘ $b(x)$ ’ is set equal to 1 they do not perform any filtering function. Instead, when ‘ $a(x)$ ’ or ‘ $b(x)$ ’ is set equal to 1 they simply pass a signal without acting upon it and thus do not act as filters to provide a finite impulse response.” (Dkt. No. 143, at 18.) Hitachi also cites the ITC Order’s analysis of these disputed terms. (ITC Order, at 11-12.)

Hitachi emphasizes that “the applicants’ amendment to claim 22 that ‘ $a(x)$ and $b(x)$ are polynomials chosen . . . to provide finite impulse responses’ ([Dkt. No. 143, Ex. G, 5/2/1997 Amendment] at VIZIO-HITACHI-13243-44 (emphasis added)) has a clear meaning to a POSITA—that ‘ $a(x)$ ’ and ‘ $b(x)$ ’ are filters that perform a filtering function.” (Dkt. No. 143, at 20 (citing Dkt. No. 144-6, 9/19/2012 Moon Decl., at ¶¶ 47-54).) Hitachi submits that this was a disclaimer of $a(x)=1$ or $b(x)=1$ because “it is well known to a POSITA that when ‘ $a(x)$ ’=1 or ‘ $b(x)$ ’=1 they do not act as a filter but simply pass information unchanged and they do not otherwise perform any filtering function.” (*Id.* (citing Dkt. No. 144-6, 9/12/2012 Moon Decl., at ¶ 47; citing Dkt. No. 143, Ex. G, 5/7/2010 King dep., at VIZIO-HITACHI-0023864).) Hitachi

urges that “Vizio’s argument that the applicants’ other distinctions somehow influenced the examiner is erroneous because the other distinctions had no bearing on the amendment to claim 22 and the examiner expressly noted that the ’887 patent was allowed in response to “the amendment filed on May 2, 1997.” (*Id.*, at 22 (citing Dkt. No. 143, Ex. I, Notice of Allowability, at VIZIO-HITACHI-13254).)

Hitachi further submits that “the majority of embodiments in the ’887 patent do not disclose $a(x)=1$ and none of the embodiments teach $b(x)$ being equal to 1.” (*Id.*, at 20.) Hitachi argues that VIZIO’s proposed construction, which would only require that one of $a(x)$ or $b(x)$ be not equal to 1, would be contrary to the plain language of claim 22, which requires that both $a(x)$ and $b(x)$ be “polynomials chosen . . . to provide finite impulse responses,” plural. (*Id.*, at 22.)

VIZIO replies that Hitachi’s arguments depend upon the extrinsic Declaration of Dr. Moon, which VIZIO argues should be given less weight than the intrinsic evidence. (Dkt. No. 149, at 5.) VIZIO also argues that Hitachi’s proposed construction imports a “filter” limitation that is not supported by the language of Claim 22. (*Id.*, at 5-6.) “Rather,” VIZIO argues, “the claim language simply requires that $a(x)$ and $b(x)$ be polynomials having finite impulse responses.” (*Id.*, at 6.) As to the prosecution history, VIZIO replies that between the statements relied upon by Hitachi, the patentee cited Figure 6 as illustrating the differences between Bruekheimer and the invention claimed in Claim 22. (*Id.*, at 6-7.) Figure 6 is an embodiment where $a(x)$ can equal 1. (*Id.*, at 7 (citing ‘887 Patent at 14:28-46).) VIZIO further submits that in responding to an earlier office action, the patentee “repeatedly relied upon examples from the specification where $a(x)=1$.” (*Id.*, at 8 (citing Dkt. No. 149, Ex. B, 5/10/1996 Amendment, at 8, 12 & 13).)

(2) Analysis

Although VIZIO proposes that the disputed term need not be construed, the parties have presented a “fundamental dispute regarding the scope of a claim term,” and the Court has a duty to resolve that dispute. *O2 Micro*, 521 F.3d at 1362-63.

“The purpose of consulting the prosecution history in construing a claim is to exclude any interpretation that was disclaimed during prosecution.” *Chimie v. PPG Indus.*, 402 F.3d 1371, 1384 (Fed. Cir. 2005). “[I]n order to disavow claim scope during prosecution ‘a patent applicant must clearly and unambiguously express surrender of subject matter.’” *Voda v. Cordis Corp.*, 536 F.3d 1311, 1321 (Fed. Cir. 2008) (citing *Sorensen v. Int’l Trade Comm’n*, 427 F.3d 1375, 1378-79 (Fed. Cir. 2005)).

During prosecution, the patentee amended Claim 22 of the ‘887 Patent as follows (additions underlined):

22. (Twice Amended) Apparatus for calculating syndromes for linear block coded codewords, comprising:

a finite impulse response filter having an input for receiving a serial bit stream of codeword data, each codeword containing k information bits and r parity bits, said filter having an output for providing a serial bit stream of syndromes, said syndromes comprising a fixed linear combination of a current bit of said codeword data input to said filter and the k previous bits of said codeword data;

wherein said filter has an impulse response $h^{k+1}(x)$, where:

$$h^{k+1}(x) = \frac{a(x) - x^{k+1}b(x)}{g(x)},$$

g(x) is a generator polynomial of degree r describing a recursion to provide an infinite impulse response, and

a(x) and b(x) are polynomials chosen such that the polynomial $h^{k+1}(x)$ will be of degree k, have a non-zero constant term $h_0 = 1$, and have a non-zero final term $h_k = 1$ to provide finite impulse responses.

(Dkt. No. 149, Ex. A, 4/29/1997 Amendment, at 1-2.) Claim 22 issued in this amended form.

The patentee also argued, in connection with the amendment:

Claims 22 and 24 have been rejected under 35 U.S.C. §102(b) as being anticipated by U.S. patent 5,367,544 to Bruekheimer. Applicants respectfully traverse this rejection, in view of the amendments to claim 22 which have been made herein. In particular, the Bruekheimer reference discloses the use of two IIR filters in a modified CRC decoder. Bruekheimer Figure 2, for example, illustrates such a decoder for natural length cyclic codes. A filter for shortened cyclic codes is presented in Figure 3.

With reference to Bruekheimer Figure 2, a first IIR filter 11 and a second IIR filter 12 are provided. Bruekheimer differs from Applicants' claimed apparatus in that he does not disclose or suggest the use of an IIR filter together with two FIR filters for calculating syndromes for linear block coded codewords. In particular, as illustrated in Applicants' Figure 6, an IIR filter 82 is provided together with a first FIR filter 86 and a second FIR filter 92. Claim 22 has been amended to more clearly set forth that the $g(x)$ function provides an infinite impulse response while the $a(x)$ and $b(x)$ polynomials provide finite impulse responses. Applicants have found no comparable FIR structure disclosed in the Bruekheimer reference.

(*Id.*, at 6-7.)

The ITC Order found a prosecution disclaimer as follows:

During the prosecution of the '887 patent, the examiner rejected claim 22 as being anticipated by Bruekheimer. The examiner concluded that Bruekheimer disclosed an embodiment where $a(x)=1$ and $b(x)=x^{n-k-1}$. In response to the rejection, the applicants amended claim 22, in part, to recite that "a(x) and b(x) are polynomials chosen such that the polynomial $h^{k+1}(x)$ will be of degree k, have a non-zero constant term $h_0=1$, and have a non-zero final term $h_k=1$ to provide finite impulse responses" (amendment shown in underline). In their remarks, the applicants stated that "Bruekheimer differs from Applicants' claimed apparatus in that he does not disclose or suggest the use of an IIR [(infinite impulse response)] filter together with two FIR [(finite impulse response)] filters for calculating syndromes for linear block coded codewords." The applicants further stated that "[c]laim 22 has been amended to more clearly set forth that the $g(x)$ function provides an infinite impulse response while the $a(x)$ and $b(x)$ polynomials provide finite impulse responses." After this response, the examiner allowed the application.

* * *

Here, the undersigned finds that the applicants overcame the examiner's rejection based on Bruekheimer by making clear that their invention included two FIR filters — $a(x)$ and $b(x)$. Additionally, one of ordinary skill in the art would understand that $a(x)=1$ or $b(x)=1$ would correspond to a wire where you would have no filtering. Thus, in order for claim 22 to have two FIR filters, as required by the applicants, neither $a(x)$ nor $b(x)$ can be equal to 1. As a result, the undersigned finds, based on the prosecution history outlined above, that the applicants of the '887 patent disclaimed any embodiments where either $a(x)$ or $b(x)$ is equal to 1.

(ITC Order, at 11-12 (citations omitted).)

VIZIO urges that the prosecution history relied upon by Hitachi and the ITC Order includes a reference to Figure 6 of the '887 Patent: "as illustrated in Applicants' Figure 6, an IIR filter 82 is provided together with a first FIR filter 86 and a second FIR filter 92." (Dkt. No. 149, Ex. A, 4/29/1997 Amendment, at 1-2.) In Figure 6, reference numbers 86 and 92 refer to " $b(x)$ " and " $g(x)$," respectively. For the embodiment illustrated in Figure 6, $a(x)=1$, as described in the following passage cited by VIZIO:

In an MPEG implementation as illustrated in FIGS. 3-6, the packets are 188 bytes ($n=1504$ bits) long with 187 bytes ($k=1496$ bits) of data and 1 byte ($r=8$ bits) of sync word. . . . The illustrated embodiment uses the space for the 1 byte sync word to accomplish both synchronization and additional error detection, above that provided by other error detection layers in the transmission system, such as Reed Solomon encoding. This is accomplished via an FIR-parity-check based linear block code, as described above. The parameters of one possible code are ($n=1504$, $k=1496$) where:

$$g(x) = 1 + x + x^5 + x^6 + x^8;$$

$$a(x) = 1;$$

$$b(x) = 1 + x + x^3 + x^7,$$

which is based on a primitive polynomial $g(x)$ of degree 8 (i.e., it produces a PN-sequence of length 255), a constant $a(x)$ and a $b(x)$ with 4 terms.

(‘887 Patent at 14:28-46.) Further, “generator polynomial $g(x)$ as indicated at box 92” “is the inverse of the IIR filter function $1/g(x)$.” In other words, the specification and the prosecution history discloses that in the embodiment illustrated in Figure 6, the infinite impulse response filter is “ $1/g(x)$ ” and the two finite impulse response filters are $b(x)$ and $g(x)$. Hitachi’s proposed construction would seemingly exclude this embodiment. *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1583 (Fed. Cir. 1996) (noting that a construction that excludes the preferred embodiment “is rarely, if ever, correct and would require highly persuasive evidentiary support”).

Nonetheless, “the claims define the scope of the right to exclude; the claim construction inquiry, therefore, begins and ends in all cases with the actual words of the claim.” *Renishaw*, 158 F.3d at 1248. Further, “[i]t is not necessary that each claim read on every embodiment.” *Baran v. Med. Device Techs., Inc.*, 616 F.3d 1309, 1316 (Fed. Cir. 2010), *cert. denied*, 131 S. Ct. 1607 (2011). Here, Claim 22 explicitly recites that $a(x)$ and $b(x)$, which are illustrated in Figure 8, “provide finite impulse responses,” plural, and regardless of the embodiment disclosed in Figure 6, the patentee relied upon the finite impulse response feature of both $a(x)$ and $b(x)$ during prosecution, as quoted above. That prosecution history should be given effect. *Typhoon Touch Techs., Inc. v. Dell, Inc.*, 659 F.3d 1376, 1381 (Fed. Cir. 2011) (“The patentee is bound by representations made and actions that were taken in order to obtain the patent.”). The Court therefore adopts the analysis of the ITC Order, as quoted above, which reached the same conclusion.

The Court accordingly hereby construes both “**a(x)**” and “**b(x)**” to mean “**a polynomial having a value other than 1 and representing a function for a filter that provides a finite impulse response.**”

F. “finite impulse response filter having an input for receiving a serial bit stream of codeword data, . . . said filter having an output for providing a serial bit stream of syndromes” (‘887 Patent, Claim 22)

VIZIO’s Proposed Construction	Hitachi’s Proposed Construction
No construction necessary – this should be given its plain and ordinary meaning.	“a one bit in, one bit out, finite impulse response (FIR) filter which receive[s] as its input a serial bit stream of codeword data, and which outputs a serial bit stream of syndromes”

(Dkt. No. 150-2, 10/3/2012 VIZIO Patents JCCC, at 6.)

(1) The Parties’ Positions

VIZIO submits that “[t]he heart of the argument between the parties revolves around whether the language of claim 22 is limited to a ‘one bit in, one bit out’ finite impulse response filter.” (Dkt. No. 142, at 11.) VIZIO argues that based on the claim language and the written description, “neither the input nor the output are limited to single bit in, single bit out situations.” (*Id.*, at 11-12.) VIZIO argues that Hitachi’s “one bit in, one bit out” limitation is an improper attempt to limit the claim to a particular embodiment despite the absence of any “expressions of manifest exclusion or restriction” in the specification. (*Id.*, at 13 (citing *Teleflex, Inc. v. Ficosa N. Am. Corp.*, 299 F.3d 1313, 1325 (Fed. Cir. 2002)).)

Hitachi responds that including “one bit in, one bit out” in the construction is necessary to give effect to the constituent term “serial.” (Dkt. No. 143, at 23.) In Hitachi’s view, “it would be improper for Vizio to potentially argue during the infringement stage of these proceedings

that this limitation is met by periodically receiving or outputting groups of bits at the same time. Such facts would demonstrate receiving or outputting data in parallel rather than serially.” (*Id.*) Hitachi also cites analysis by the ITC Order as well as disclosure in the specification that it was “important” to “the invention” “for the finite impulse response filter to function as a one bit in, one bit out filter.” (*Id.* (citing ITC Order, at 14; citing ‘887 Patent at 11:39-43).) Hitachi further cites a dictionary definition of a “serial bit” as “[d]ata in which the bits of each byte or word are sent or received one at a time.” (*Id.*, at 24 (Dkt. No. 143, Ex. J, *The Illustrated Dictionary of Electronics* 499 (4th ed. 1988)).) Finally, Hitachi responds that “Hitachi does not argue that the input or the output has only a single bit. What Hitachi’s construction clarifies, and what the claim language and the specification mandates, is that only one bit is inputted into or outputted from the filter at a given time.” (*Id.*, at 24.)

VIZIO replies that the ‘887 Patent “discloses syndromes ‘outputs’ that are larger than one bit,” and VIZIO argues that “nothing in the specification requires that for every bit input a single bit must be output.” (Dkt. No. 149, at 9.) VIZIO further argues that “the plain and ordinary meaning of ‘serial’ does not require either [single bit] relationship.” (*Id.*)

(2) Analysis

Claim 22 of the ‘887 Patent is reproduced in subsection VI.E., above. The specification discloses, for example (emphasis added):

It should now be appreciated that the present invention provides a method and apparatus for achieving synchronization and detecting errors in a packetized data stream. Although the invention has particular applicability to the synchronization and error detection in an MPEG transport packet scheme, it is not limited to use with the MPEG format. *The invention* also provides a unique and economical decoder, in which syndrome calculation is accomplished using *a one bit input, one bit output FIR filter*.

(‘887 Patent at 14:53-61.)

The ITC Order found:

The specification describes the FIR filter of the claimed syndrome calculator numerous times as having a one bit in, one bit out characteristic. (‘887 patent at Abstract (“A syndrome calculator in the decoder can be implemented using a unique one bit in, one bit out FIR filter.”); 4:59-62 (“FIG. 8 is a block diagram illustrating a one bit in, one bit out finite impulse response (FIR) filter used as a syndrome calculator”); 5:8-10 (“The data stream is transmitted in serial fashion, most significant bit (MSB) first.”) [footnote: This implies that “in serial fashion” means one bit at a time.]; 11:39-43 (“This is very important in implementing the single bit in, single bit out decoder FIR filter (syndrome calculator) of the present invention”).)

Moreover, the specification refers to “the present invention” and “[t]he invention” when stating that “syndrome calculation is accomplished using a one bit input, one bit output FIR filter.” (*Id.* at 14:53-61.) This language leads to the conclusion that a FIR filter with a one bit input and one bit output is the only FIR filter that the claims cover, and is not merely a preferred embodiment.

(ITC Order, at 14-15 (citing, *e.g.*, *Honeywell Int’l Inc. v. ITT Indus., Inc.*, 452 F.3d 1312, 1318 (Fed. Cir. 2006) (finding that use of phrases such as “the invention” and “the present invention” in the written description weighs in favor of limiting the claim scope to the described embodiment)).) On balance, this Court adopts the analysis and conclusion reached in the ITC Order.

The Court accordingly hereby construes **“finite impulse response filter having an input for receiving a serial bit stream of codeword data, . . . said filter having an output for providing a serial bit stream of syndromes”** to mean **“a one bit in, one bit out, finite impulse response (FIR) filter which receives as its input a serial bit stream of codeword data, and which outputs a serial bit stream of syndromes.”**

G. “scrambling” (‘522 Patent, Claims 1 and 6)

VIZIO’s Proposed Construction	Hitachi’s Proposed Construction
<p>This is a preamble term that is not a claim limitation.</p> <p>Alternatively, should the Court construe this element to be a claim limitation, VIZIO proposes the following:</p> <p>“randomizing / derandomizing”</p>	<p>“performing a logical operation on data bits to be transmitted in order to flip the bits in a random or pseudorandom manner”</p>

(Dkt. No. 150-2, 10/3/2012 VIZIO Patents JCCC, at 6-7.)

(1) The Parties’ Positions

VIZIO argues that because the term “scrambling” only appears in the preambles, and not the bodies, of Claims 1 and 6 of the ‘522 Patent, “scrambling” is not a limitation. (Dkt. No. 142, at 14.) Alternatively, VIZIO proposes that “scrambling” means “randomizing/derandomizing,” based on disclosure in the specification that “the randomizer can also be used to derandomize” and that “the term randomizer as used herein and in the claims is intended to also encompass a derandomizer.” (*Id.* (citing ‘522 Patent at 1:63-67).) VIZIO submits that “[l]ogically, this makes sense” because “[t]o derandomize a randomized bit stream, the same exact scrambling sequence would be applied at the transmitter and the receiver.” (*Id.*, at 15 (citing ‘522 Patent at Figs. 1 & 2).) VIZIO acknowledges that the ITC Order found that “scrambling” is different than “descrambling,” but VIZIO argues that the ITC Order misread the disclosure in the specification that “[d]escrambling is carried out using a circuit that performs the inverse operation using the same polynomial [used for scrambling].” (*Id.*, at 15-16.) VIZIO argues that the “inverse operation” relied upon by the ITC Order is the same “scrambling” because “[t]o ‘reverse’ this

scrambling process, the same scrambling sequence is applied to the randomized bit stream, which causes the bit stream to return to its original state.” (*Id.*, at 16.)

Hitachi responds that “scrambling” is a limitation of the claims because the patentee relied upon “scrambling” to distinguish prior art during prosecution. (Dkt. No. 143, at 25.) Hitachi cites the patentee’s amendment in response to the examiner’s rejection of claims based on obviousness over the “Arazi” prior art reference, United States Patent No. 5,206,824. (*Id.*, at 26 (citing Dkt. No. 143, Ex. K, 10/10/1996 Amendment, at 1-3 (VIZIO-HITACHI-0013443-45)).) In particular, Hitachi notes that the patentee amended the preamble of application claim 1 so as to “replace the word ‘scramble’ with the phrase ‘provide byte-wise scrambling.’” (*Id.*)

As to the proper construction, Hitachi responds that “Vizio seeks to transform a transmitter/encoder claim into a receiver/decoder claim by changing the term ‘scrambling’ to ‘randomizing’ and then argu[ing] that randomizing and derandomizing are the same.” (*Id.*)

Hitachi explains:

[T]he patentee specifically chose to claim “scrambling” rather than “randomizing,” and scrambling and descrambling are opposite processes rather than the same process. Scrambling occurs at the transmitter/encoder and descrambling happens at the receiver/decoder. ’522 patent at 1:27-30; 1:55-56. Hitachi’s construction, the same as that adopted by Judge Bullock [in the ITC Order], attempts to give “scrambling” its ordinary meaning known to those of ordinary skill in the art and declines to equate it to randomizing, let alone equate it to derandomizing as Vizio ultimately seeks to do.

(*Id.*) Hitachi also submits that “[t]he term ‘scrambling’ is well-understood in the art to refer to an operation at the transmitter” and that a person of ordinary skill in the art would use the term “descrambling” to describe the operation that occurs at the receiver. (*Id.*, at 27 (citing Dkt. No. 144-6, 9/19/2012 Moon Decl., at ¶¶ 64-68).) Hitachi also cites other HDTV-related patents that discuss scrambling and descrambling as different operations. (*Id.* (citing Dkt. No. 144, Ex. L,

United States Patent No. 5,007,088 at 1:14-22 & Ex. M, United States Patent No. 5,682,195 at 2:24-30).) Further, Hitachi cites a dictionary that defines “scrambled signal” to mean “[a]ny signal—audio, video, or other—in which (for secrecy or exclusivity) the elements are disarranged according to some agreed-upon scheme so that intelligent reception is possible only if the signal is unscrambled by means of [a] suitable decoder at the receiving point.” (*Id.* (citing Dkt. No. 143, Ex. J, *The Illustrated Dictionary of Electronics* 499 (4th ed. 1988) (emphasis omitted)).)

Finally, Hitachi cites disclosure in the specification that “scrambling” occurs prior to transmission and that “descrambling” is the inverse operation that takes place at the receiver. (*Id.*, at 28 (citing ‘522 Patent at 1:27-32).) Hitachi analogizes that “Vizio is essentially saying that locking and unlocking a lock is the same process because the same key is used.” (*Id.*) Hitachi concludes that VIZIO’s proposed construction should be rejected because there is no lexicography in the patent that defines “scrambling” to refer to a “randomizer.” (*Id.*, at 28-29 (citing Dkt. No. 144-6, 9/19/2012 Moon Decl., at ¶¶ 69-70).)

VIZIO replies by noting that Hitachi relies heavily on extrinsic evidence. (Dkt. No. 149, at 10.) Such evidence is irrelevant here, VIZIO argues, because extrinsic evidence cannot be relied upon where the intrinsic evidence is unambiguous. (*Id.* (citing *CAE Screenplates*, 224 F.3d at 1318).) VIZIO emphasizes disclosure in the specification that:

The present invention provides a *data randomizer* for processing bytes of data *to scramble data* bits contained therein. It should be appreciated that the randomizer can also be used to *derandomize (i.e., descramble)* data that has already been randomized by a counterpart randomizer. Thus, the term randomizer as used herein and in the claims is intended to also encompass a derandomizer.

(*Id.* (citing ‘522 Patent at 1:60-67 (emphasis VIZIO’s)).)

(2) Analysis

In general, a preamble limits the invention if it recites essential structure or steps, or if it is necessary to give life, meaning, and vitality to the claim. . . . [A] preamble is not limiting where a patentee defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention.

Catalina Mktg. Int'l, Inc. v. Coolsavings.com, Inc., 289 F.3d 801, 808 (Fed. Cir. 2002) (citation and internal quotation marks omitted); see *Altiris, Inc. v. Symantec Corp.*, 318 F.3d 1363, 1372 (Fed. Cir. 2003) (preamble not limiting where it “merely recites a purpose of the invention and does not add anything to the body of the claims.”); see also *Bristol-Myers Squibb Co. v. Ben Venue Laboratories, Inc.*, 246 F.3d 1368, 1376-77 (Fed. Cir. 2001) (holding that a preamble term that merely states a use is not limiting).

During prosecution, the patentee responded to an obviousness rejection by amending the preamble of Claim 1 as follows (additions underlined, deletions in square brackets):

1. (Amended) A data randomizer for processing bytes of data to provide byte-wise scrambling of [scramble] data bits contained therein, each byte having an integer number N of bits, said randomizer comprising:

The patentee then argued:

Claims 1-5 have been rejected under 35 U.S.C. § 103 as being unpatentable over U.S. patent 5,206,824 to Arazi. Applicant traverses this and the subsequent rejections in view of the foregoing amendment and the following comments. In particular, claim 1 has been amended to clarify that a data randomizer is set forth for processing bytes of data to provide byte-wise scrambling of bits contained therein. Thus, data is input to the randomizer a byte at a time, and the bits within the byte are scrambled concurrently.

. . .

[T]he Arazi structure cannot provide byte-wise scrambling, but instead provides a square vector β^2 which includes a sequence of individual bits including alternating 0's (Arazi, column 6, lines 11-13).

(Dkt. No. 143, Ex. K, 10/10/1996 Amendment, at 3-4 (VIZIO-HITACHI-0013445-46).) Claim 1 issued in this amended form. Although this argument focuses on the “byte-wise” nature of the scrambling, the fact remains that the patentee relied upon the “scrambling” in the preamble of Claim 1 to distinguish Arazi.

Because the patentee relied upon the term “scrambling” in the preamble of Claim 1 to overcome a prior art rejection during prosecution, the term “scrambling” in the preamble is a limitation of Claim 1 of the ‘522 Patent. *Invitrogen Corp. v. Biocrest Mfg., L.P.*, 327 F.3d 1364, 1370 (Fed. Cir. 2003) (“[C]lear reliance on the preamble during prosecution to distinguish the claimed invention from the prior art transforms the preamble into a claim limitation because such reliance indicates use of the preamble to define, in part, the claimed invention.”) (quoting *Catalina Mktg.*, 289 F.3d at 808). The ITC Order reached the same conclusion. (*See* ITC Order, at 23-25.)

Hitachi also argues that “scrambling” is a limitation in the preamble of Claim 6 of the ‘522 Patent, which recites (emphasis added):

6. A data randomizer for scrambling seven-bit data bytes, said randomizer comprising:
 - a bank of seven linear feedback shift registers SR₀-SR₆ for providing as output seven binary pseudorandom (PN) sequences Y₀-Y₆, respectively;
 - each of said linear feedback shift registers (“LFSRs”) comprising three register stages in series and having feedback taps after said first and third register stages;
 - the PN sequences Y₀-Y₆ from the third stages of the LFSRs being fed back to the tap that follows the first stage of the respective LFSR;
 - the first stage of LFSRs SR₆, SR₀, SR₁, and SR₂ receiving as inputs the PN sequences Y₃, Y₄, Y₅, and Y₆ respectively; and
 - the first stage of LFSRs SR₃, SR₄, and SR₅ receiving as inputs the exclusive-OR’s Y₀⊕Y₄, Y₁⊕Y₅, and Y₂⊕Y₆, respectively.⁶

⁶ The published patent uses a circled bar symbol to represent exclusive-OR (“XOR”), but XOR is commonly represented as a circled plus, as in the Figures of the ‘522 Patent.

Hitachi presents no separate argument as to Claim 6. (*See* Dkt. No. 143, at 24-29.) Hitachi has not shown that the prosecution history cited above with respect to Claim 1 has any applicability to Claim 6. Although Hitachi relies generally on the ITC Order, the ITC Order did not address Claim 6. (*See* ITC Order, at 20-25.) Further, Claim 6 on its face does not appear to rely upon the recitation of “scrambling” in the preamble “to give life, meaning, and vitality to the claim.” *Catalina Mktg.*, 289 F.3d at 808. Thus, although the term “scrambling” in the preamble of Claim 1 is a limitation of that claim, the same term in the preamble of Claim 6 is *not* a limitation of that claim.

As to the proper construction for “scrambling” in Claim 1 of the ‘522 Patent, “[i]t is well-settled that an inventor may act as his own lexicographer to define a patent term.” *Ecolab, Inc. v. FMC Corp.*, 569 F.3d 1335, 1344 (Fed. Cir. 2009) (citation omitted). However, “[t]he patentee’s lexicography must . . . appear with reasonable clarity, deliberateness, and precision before it can affect the claim.” *Renishaw*, 158 F.3d at 1249. VIZIO relies upon the following disclosure in the written description as a lexicography that “define[s] randomizer as being both a randomizer and a derandomizer for scrambling and descrambling data” (Dkt. No. 142, at 15):

It should be appreciated that the randomizer can also be used to derandomize (i.e. descramble) data that has already been randomized by a counterpart randomizer. Thus, the term randomizer as used herein and in the claims is intended to also encompass a derandomizer.

(‘522 Patent at 1:63-67.) The Background of the Invention also discloses:

The present invention provides a scrambler/descrambler having the aforementioned and other advantages. More particularly, the present invention provides a data randomizer/derandomizer for scrambling/unscrambling data bytes on a “byte-wise” level, wherein data is input to the randomizer or derandomizer a byte at a time, and the bits within the byte are scrambled concurrently.

(*Id.*, at 1:52-58.) This usage of “scrambling/unscrambling,” together with the statements that the “randomizer or derandomizer” “scramble[s]” the bits within the byte and that “the term randomizer . . . encompass[es] a derandomizer,” could be read to mean that “scrambling” and “descrambling” are synonymous.

The ITC Order nonetheless concluded that “[u]nlike the case of ‘data randomizer’ above, the patentee did not indicate a clear intent to define ‘scrambling’ as meaning both ‘scrambling’ and ‘descrambling.’” (ITC Order, at 25.) The ITC Order highlighted that “the specification clearly states”:

Scrambling, or randomization of the data stream input to a modem is intended to prevent long sequences of logical “1”s or “0”s. ***The scrambler*** performs a logical operation on the data bits to be transmitted using a polynomial with binary coefficients implemented via the LFSR. ***Descrambling*** is carried out using a circuit that ***performs the inverse operation*** using the same polynomial.

(*Id.* (quoting ‘522 Patent at 1:24-32).) Thus, although scrambling and descrambling may apply the same polynomial in order to scramble and descramble, respectively, descrambling is the inverse of scrambling. (*See* ‘522 patent at 3:8-9.) The ITC Order’s finding in this regard is also consistent with disclosure of a “scrambler” and a “descrambler” as separate structures in Figures 1 and 2. (‘522 Patent at 2:47-51, 2:61-63, 3:5-7, Fig. 1 & Fig. 2.)

Finally, turning to the extrinsic evidence, Hitachi’s expert, Dr. Moon, opines that “[a] ‘[r]andomizer’ and a ‘derandomizer’ are devices or apparatuses, while scrambling refers [to] an operation that a randomizer performs, and descrambling refers to an operation that a derandomizer performs.” (Dkt. No. 144-6, 9/19/2012 Moon Decl., at ¶ 69.)

On balance, this Court agrees with the ITC Order that the patentee did not set forth a lexicography with “reasonable clarity, deliberateness, and precision” so as to alter the otherwise


apparent use of different terms, “scrambling” and “descrambling,” to refer to different operations. *Renishaw*, 158 F.3d at 1249. As Hitachi appropriately analogizes, equating scrambling and descrambling would be tantamount to “saying that locking and unlocking a lock is the same process because the same key is used.” (Dkt. No. 143, at 28.) This Court therefore applies substantially the same construction of “scrambling” as reached in the ITC Order. The Court omits the phrase “to be transmitted,” however, because Defendants have not demonstrated that Claim 1 is limited to transmission.

In sum, the Court finds that “scrambling” is a limitation of Claim 1 of the ‘522 Patent, finds that “scrambling” is *not* a limitation of Claim 6 of the ‘522 Patent, and hereby construes **“scrambling” to mean “performing a logical operation on data bits in order to flip certain bits in a random or pseudorandom manner.”**

VII. CONCLUSION

The Court adopts the constructions set forth in this opinion for the disputed terms of the patents-in-suit. The parties are ordered that they may not refer, directly or indirectly, to each other’s claim construction positions in the presence of the jury. Likewise, the parties are ordered to refrain from mentioning any portion of this opinion, other than the actual definitions adopted by the Court, in the presence of the jury. Any reference to claim construction proceedings is limited to informing the jury of the definitions adopted by the Court.

So ORDERED and SIGNED this 13th day of November, 2012.



RODNEY GILSTRAP
UNITED STATES DISTRICT JUDGE