UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

PARTHENON UNIFIED MEMORY ARCHITECTURE, LLC	§	
	§	
v.	§	**Case No. 2:14-cv-00690-RSP (Lead)**
	§	
HTC CORPORATION and HTC AMERICA, INC.	§	

PARTHENON UNIFIED MEMORY ARCHITECTURE, LLC	§	
	§	
v.	§	**Case No. 2:14-cv-00691-JRG-RSP (Consolidated)**
	§	
LG ELECTRONICS, INC. and LG ELECTRONICS USA., INC.	§	

MEMORANDUM OPINION AND ORDER

On June 5, 2015, the Court held a hearing to determine the proper construction of disputed terms in the nine Asserted Patents in this case. The Court, having considered the parties' claim construction briefing (Dkt. Nos. 120, 121, 122) and their arguments at the hearing, issues this Memorandum Opinion and Order construing the disputed terms.

BACKGROUND AND THE ASSERTED PATENTS

Parthenon Unified Memory Architecture, LLC ("PUMA") brings two actions: first, against HTC Corp. and HTC America, Inc.; and second, against LG Electronics, Inc. and LG Electronics USA, Inc. (collectively, "Defendants"). These actions allege that Defendants infringed nine of PUMA's patents: U.S. Patent Nos. 5,812,789 ("the '789 Patent"), 6,058,459 ("the '459 Patent"), 6,427,194 ("the '194 Patent"), 7,321,368 ("the '368 Patent"), 7,542,045

("the '045 Patent"), 7,777,753 ("the '753 Patent"), 8,054,315 ("the '315 Patent"), 8,681,164 ("the '164 Patent") and 5,960,464 ("the '464 Patent") (collectively, "the Asserted Patents"). Of the nine patents, two patents, the '789 Patent and the '459 Patent, were both filed on August 26, 1996, rely on similar specifications, and incorporate each other by reference. Six patents are based on continuation applications of the '459 Patent: the '194 Patent, the '368 Patent, the '045 Patent, the '753 Patent, the '315 Patent, and the '164 Patent. One patent, the '464 Patent,[1] relies on a specification that is not shared by any of the other Asserted Patents.

In general, the '789 Patent, the '459 Patent, the '194 Patent, the '368, the '045 Patent, the '753 Patent, the '315 Patent, and the '164 Patent relate to systems in which a first device (for example a processor) and a decoder/encoder share a common memory. For example, the '459 Patent abstract recites:

> An electronic system provides direct access between a first device and a decoder/encoder and a memory. The electronic system can be included in a computer in which case the memory is a main memory. Direct access is accomplished through one or more memory interfaces. Direct access is also accomplished in some embodiments by direct coupling of the memory to a bus, and in other embodiments, by direct coupling of the first device and decoder/encoder to a bus. The electronic system includes an arbiter for determining access for the first device and/or the decoder/encoder to the memory for each access request. The arbiter may be monolithically integrated into a memory interface of the decoder/encoder or the first device. The decoder may be a video decoder configured to decode a bit stream formatted to comply with the MPEG-2 standard. The memory may store predicted images which are obtained from a single preceding image and may also store intra images. Bidirectional images which are directly supplied to a display adapter may be obtained from two preceding intra or predicted images.

'459 Patent Abstract.

[1] The '464 Patent was filed on August 23, 1996.

The remaining patent, the ’464 Patent, relates generally to a system whereby a decoder, which requires contiguous blocks of memory, can utilize noncontiguous blocks of the system’s memory. The ’464 patent abstract recites:

> A method and apparatus employing a memory management system that can be used with applications requiring a large contiguous block of memory, such as video decompression techniques (e.g., MPEG 2 decoding). The system operates with a computer and the computer's operating system to request and employ approximately 500 4-kilobyte pages in two or more noncontiguous blocks of the main memory to construct a contiguous 2-megabyte block of memory. The system can employ, on a single chip, a direct memory access engine, a microcontroller, a small block of optional memory, and a video decoder circuit. The microcontroller retains the blocks of multiple pages of the main memory, and the page descriptors of these blocks, so as to lock down these blocks of memory and prohibit the operating system or other applications from using them. The microcontroller requests the page descriptors for each of the blocks, and programs a lookup table or memory mapping system in the on-chip memory to form a contiguous block of memory. As a result, the video decoder circuit can perform operations on a 2-megabyte contiguous block of memory, where the microcontroller employs the lookup table to translate each 2-megabyte contiguous address requested by the video decoder circuit to its appropriate page in the main memory. As soon as the video decoding operations are complete, the microcontroller releases the blocks of multiple pages of memory back for use by the computer.

’464 Patent Abstract.

APPLICABLE LAW

1. Claim Construction

“It is a ‘bedrock principle’ of patent law that ‘the claims of a patent define the invention to which the patentee is entitled the right to exclude.’” *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (quoting *Innova/Pure Water Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)). To determine the meaning of the claims, courts start by considering the intrinsic evidence. *Id.* at 1313; *C.R. Bard, Inc. v. U.S. Surgical Corp.*, 388 F.3d 858, 861 (Fed. Cir. 2004); *Bell Atl. Network Servs., Inc. v. Covad Commc’ns Group, Inc.*, 262 F.3d 1258, 1267 (Fed. Cir. 2001). The intrinsic evidence includes the claims themselves, the

specification, and the prosecution history. *Phillips*, 415 F.3d at 1314; *C.R. Bard, Inc.*, 388 F.3d at 861. Courts give claim terms their ordinary and accustomed meanings as understood by one of ordinary skill in the art at the time of the invention in the context of the entire patent. *Phillips*, 415 F.3d at 1312–13; *Alloc, Inc. v. Int'l Trade Comm'n*, 342 F.3d 1361, 1368 (Fed. Cir. 2003).

The claims themselves provide substantial guidance in determining the meaning of particular claim terms. *Phillips*, 415 F.3d at 1314. First, a term's context in the asserted claim can be very instructive. *Id*. Other asserted or unasserted claims can also aid in determining the claim's meaning, because claim terms are typically used consistently throughout the patent. *Id*. Differences among the claim terms can also assist in understanding a term's meaning. *Id*. For example, when a dependent claim adds a limitation to an independent claim, it is presumed that the independent claim does not include the limitation. *Id*. at 1314–15.

"[C]laims 'must be read in view of the specification, of which they are a part.'" *Id*. (quoting *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995) (en banc)). "[T]he specification 'is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.'" *Id*. (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)); *Teleflex, Inc. v. Ficosa N. Am. Corp.*, 299 F.3d 1313, 1325 (Fed. Cir. 2002). This is true because a patentee may define his own terms, give a claim term a different meaning than the term would otherwise possess, or disclaim or disavow the claim scope. *Phillips*, 415 F.3d at 1316. In these situations, the inventor's lexicography governs. *Id*. The specification may also resolve ambiguous claim terms "where the ordinary and accustomed meaning of the words used in the claims lack sufficient clarity to permit the scope of the claim to be ascertained from the words alone." *Teleflex, Inc.*, 299 F.3d at 1325. But, "'[a]lthough the specification may aid the court in interpreting the meaning of

disputed claim language, particular embodiments and examples appearing in the specification will not generally be read into the claims.'" *Comark Commc'ns, Inc. v. Harris Corp.*, 156 F.3d 1182, 1187 (Fed. Cir. 1998) (quoting *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1560, 1571 (Fed. Cir. 1988)); *see also Phillips*, 415 F.3d at 1323. The prosecution history is another tool to supply the proper context for claim construction because a patent applicant may also define a term in prosecuting the patent. *Home Diagnostics, Inc., v. Lifescan, Inc.*, 381 F.3d 1352, 1356 (Fed. Cir. 2004) ("As in the case of the specification, a patent applicant may define a term in prosecuting a patent.").

Although extrinsic evidence can be useful, it is "'less significant than the intrinsic record in determining the legally operative meaning of claim language.'" *Phillips*, 415 F.3d at 1317 (quoting *C.R. Bard, Inc.*, 388 F.3d at 862). Technical dictionaries and treatises may help a court understand the underlying technology and the manner in which one skilled in the art might use claim terms, but technical dictionaries and treatises may provide definitions that are too broad or may not be indicative of how the term is used in the patent. *Id*. at 1318. Similarly, expert testimony may aid a court in understanding the underlying technology and determining the particular meaning of a term in the pertinent field, but an expert's conclusory, unsupported assertions as to a term's definition are entirely unhelpful to a court. *Id*. Generally, extrinsic evidence is "less reliable than the patent and its prosecution history in determining how to read claim terms." *Id*.

2. Claim Indefiniteness

Patent claims must particularly point out and distinctly claim the subject matter regarded as the invention. 35 U.S.C. § 112, ¶ 2. "[I]ndefiniteness is a question of law and in effect part of claim construction." *ePlus, Inc. v. Lawson Software, Inc.*, 700 F.3d 509, 517 (Fed. Cir. 2012). A

party challenging the definiteness of a claim must show it is invalid by clear and convincing evidence. *Young v. Lumenis, Inc.*, 492 F.3d 1336, 1345 (Fed. Cir. 2007).

The definiteness standard of 35 U.S.C. § 112, ¶ 2 requires that:

> [A] patent's claims, viewed in light of the specification and prosecution history, inform those skilled in the art about the scope of the invention with reasonable certainty. The definiteness requirement, so understood, mandates clarity, while recognizing that absolute precision is unattainable. The standard we adopt accords with opinions of this Court stating that "the certainty which the law requires in patents is not greater than is reasonable, having regard to their subject-matter.

Nautilus, Inc. v. Biosig Instruments, Inc., 134 S. Ct. 2120, 2129–30 (2014) (internal citations omitted).

3. Construing Claim Terms that Have Previously Been Construed by This Court or Other Courts

This is not the first time a Court in this District has construed some of the disputed terms. In *STMicroelectronics, Inc. v. Motorola, Inc.*, 327 F. Supp. 2d 687 (E.D. Tex. 2004) the Court construed the '789 Patent. This previous construction is not controlling here but it can be instructive and will, at times, provide part of the basis for the Court's analysis. *See Burns, Morris & Stewart Ltd. P'ship v. Masonite Int'l Corp.*, 401 F. Supp. 2d 692, 697 (E.D. Tex. 2005) (while a previous construction may be instructive and provide the basis of the analysis, the previous construction is not binding on the court, particularly when there are new parties and those parties have presented new arguments).

AGREED TERMS

The parties agree that "simultaneously accesses the bus" means "accesses the bus at the same time." (Dkt. No. 123-2 at 4). The parties also agree that the following terms require no construction: "without requiring a second bus," "without also requiring a second bus" and "video

stream input device circuit." (Dkt. No. 120 at 24, 28); (Dkt. No. 121 at 1). At the oral hearing, the parties agreed that "display device" means "screen and its circuitry." (Dkt. No. 137 at 4). At the oral hearing, the parties also agreed that "display adapter" means "an adapter that processes images for a display device." (*Id.*).

DISPUTED TERMS

1. **"bus" ('789 Patent claims 1, 13; '459 Patent claims 1, 2, 7, 11, 13; '194 Patent claims 1, 2, 9, 11, 16-18, 23; '368 Patent claims 1, 5, 7, 13, 19, 20, 23; '045 Patent claims 1, 4, 5, 12, 15; '753 Patent claims 1, 7; '315 Patent claim 1 and '164 Patent claims 1, 6, 7)**

PUMA's Construction	Defendants' Construction
No construction necessary. Alternatively: "a signal line or a set of signal lines to which a number of devices are coupled and over which information may be transferred"	"a signal line or set of parallel signal lines to which a number of devices are attached and over which information may be broadcast among them"

The primary disputes between the parties relate to PUMA's inclusion of the word "coupled" and Defendants' inclusion of the words "parallel" and "broadcast among them." The parties' disputes on these issues turn on whether a "bus" can have intervening components and whether two buses are included in the construction of "bus."

Positions of the Parties

PUMA asserts that the term "bus" is well-known in the art and does not need construction. PUMA's alternative construction comes from *STMicroelectronics*. In *STMicroelectronics*, the parties agreed that "bus" should be construed as "a signal or set of signal lines to which a number of devices are coupled and over which information may be transferred between them." *STMicroelectronics*, 327 F. Supp. 2d at 711. PUMA asserts that its construction is consistent with multiple extrinsic evidence dictionaries. (Dkt. No. 120 at 8).

PUMA objects to Defendants' inclusion of "broadcast" and "parallel" in their proposed construction. PUMA asserts that the word "broadcast" itself requires additional construction, and that, to the extent "broadcast" means "transmitted," PUMA's use of the word "transferred" is less ambiguous and less confusing.

PUMA asserts that if Defendants have proposed "broadcast" because "broadcast" has a specific meaning, limiting "bus" in this manner is not supported by the specification. (*Id*. at 9). Not every bus "broadcasts" a signal to all locations on the line, and PUMA asserts that Defendants' construction would read out types of buses that were known and commonly used in the art at the time. For example, the SPARC memory bus ("Mbus") developed by Sun Microsystems and similar circuit-switch or multiplexed buses. (Dkt. No. 122 at 2).

PUMA objects to Defendants' use of the word "parallel" because it is as ambiguous as "broadcast." PUMA asserts that "parallel" could refer to either a geometrical arrangement (*i.e.*, parallel versus perpendicular lines) or to a method of data transmission (*i.e.*, parallel data versus serial data). (Dkt. No. 120 at 9). PUMA states that the Asserted Patents do not make either of those distinctions and do not use the term "parallel."

Defendants assert that the construction stipulated to in *STMicroelectronics* does not apply in this case because *STMicroelectronics* involved only the '789 Patent. Defendants further assert that the Court's construction in *STMicroelectronics* fails for two reasons. First, the *STMicroelectronics* construction does not distinguish between a single bus and multiple buses. Defendants assert this distinction is critical because some claims explicitly exclude a second bus. For example, claim 1 of the '459 Patent, which states, "without also requiring a second bus." Defendants note that similar language is found in other claims of the '459 Patent and in the '194 Patent claims. (Dkt. No. 121 at 2, n.1).

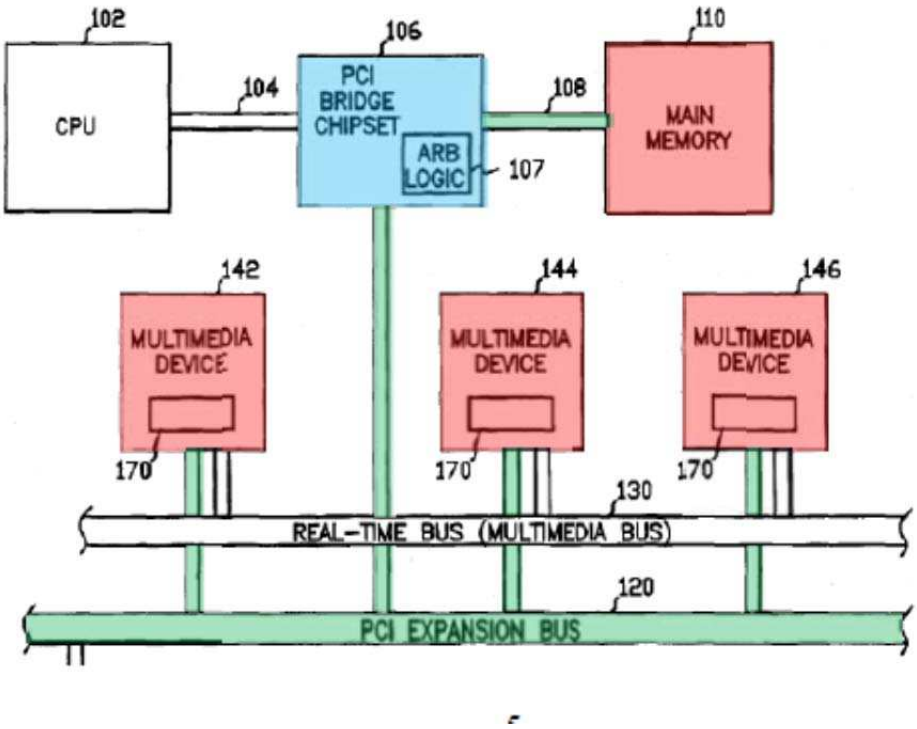
Second, Defendants assert that the *STMicroelectronics* construction fails to consider statements made during the prosecution of the ’368 Patent. Defendants assert that during the prosecution of the ’368 Patent, the Applicants required a “bus” to be more than a local point-to-point connection between two devices. (*Id*. at 2). Defendants assert that their construction accounts for this prosecution history statement because it distinguishes between busses that can provide a point-to-point connection between two devices from busses that must connect more than two devices.

As to the words “broadcast” and “parallel” not appearing in the claims, Defendants assert that these concepts are contained throughout the claims. (*Id*. at 2). Defendants assert that “broadcast” reflects a fundamental property of a “signal line” and distinguishes one bus from multiple buses. Defendants assert that a signal line carries only one signal at a time. Defendants assert that a signal line cannot convey two different signals from two different sources at the same time, or else a “contention” would occur. (*Id*. at 3). Defendants assert that the patents include an arbiter to prevent any contentions.

Defendants point to Figure 1c of the ’789 Patent as being illustrative. Defendants assert that the PCI bus 170 and ISA bus 198 present a signal everywhere on the line and, thus, the signal is available to any device attached to the line. Defendants assert that to “broadcast” information on a signal line of a bus means that the entire signal line carries the same information, regardless of the number of devices receiving the information. Defendants assert that, in contrast, if the signal line is broken into separate parts by an intervening component, then two buses are present. For example, Defendants assert that if a switch is present, so that a device broadcasts to only part of the signal line, or so that different devices may transmit information separately on different parts of the signal line, then more than one bus is present. (*Id*. at 4).

Defendants assert that PUMA's construction is too broad in that the construction potentially covers configurations that include multiple, separate, buses. Defendants again point to '789 Patent Figure 1c as an example. Defendants assert that under PUMA's construction, the PCI bus 170 and ISA bus 198 could constitute a single bus as the two buses are connected through the PCI bridge 192. Defendants assert that such a reading contradicts the specification, prosecution histories, and the understanding of one skilled in the art. (*Id*. at 4-5). Defendants assert that the patents clearly disclose two buses: PCI bus 170 and ISA bus 198. Defendants similarly point to the three buses of '459 Patent Figure 7 (buses 170, 198, and 185). Defendants assert that PUMA's construction would interpret the three buses as a single bus. (*Id*. at 5).

Defendants also assert that the prosecution history of the '459 Patent supports their construction. During prosecution, a rejection was based on U.S. Patent No. 5,682,484 ("Lambrecht"). Defendants point to Lambrecht Figure 1:



(Dkt. No. 121 at 5 (Lambrecht Figure 1, color coding added)). Defendants assert that during prosecution, the Applicants distinguished the PCI bus 120 and memory bus 108 of Lambrecht as being two buses. Defendants assert the Applicants then added to the claims this limitation: that the devices access the memory "without requiring a second bus." (*Id*. at 7 (citing Ex. 8 at 0791)). Defendants assert that the Applicants, thus, distinguished the PCI bus 120 and memory bus 108 as being separate busses due to the intervening PCI bridge chipset 106. (*Id*.). Defendants assert that the prosecution history makes clear that a "bus" cannot include a set of signal lines that are sequential or in series with other signal lines. Defendants assert that the series connection in Lambrecht of the PCI bus 120, PCI bridge chipset 106, and memory bus 108 is not a "bus," but rather two sequential buses. (*Id*.).

Defendants also state that the language "among them" that is used in Defendants' construction is relevant to prosecution history statements. Defendants assert that such language makes clear that connections between only two devices are not a bus. Defendants point to a rejection in the '368 Patent prosecution based on U.S. Patent No. 5,576,765 ("Cheney"). Defendants assert that, with regard to Cheney, the Applicants asserted that a connection between just a memory and a decoder was not a bus. Specifically, Defendants point to the arguments regarding Cheney Figure 4:

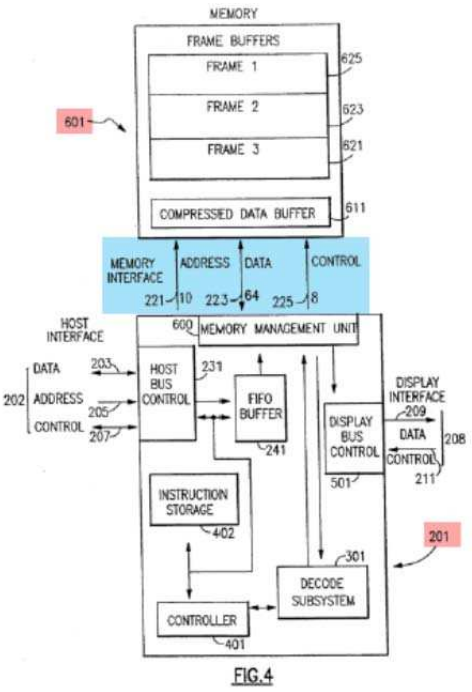


FIG.4

(Dkt. No. 121 at 7 (Cheney Figure 4, color coding added)). Defendants assert that the Applicants argued that the lines 221, 223 and 225 connecting the memory 601 and the decoder 201 were not a bus:

> The connection between memory 601 and decoder 201 is a local connection and connects only the two devices together. **It is not a bus** as was well recognized by Cheney and as is recognized by those with skill in the art.

(Dkt. No. 121 Ex. 11 at 01236) (emphasis added). Defendants assert that in contradiction to this statement, Cheney recognized that the lines in question were buses: "[t]he interface between the memory management unit 600 and the memory 601 includes an address bus, 221, a bidirectional data bus, 223, and a control bus 225." (Dkt. No. 121 Ex. 9 (Cheney) at 7:35-37). Defendants assert that Cheney never describes a "local connection." Defendants assert that the Applicants made a clear and unmistakable statement that a connection between only two devices is "not a bus." (Dkt. No. 121 at 8). At the oral hearing, Defendants stated that the language "among them" required the bus to be capable of connecting at least three devices. (Dkt. No. 137 at 31-32).

At the oral hearing, Defendants agreed that the term "bus" was generally understood in the art. (*Id.* at 9). Defendants emphasized at the hearing that PUMA's construction would allow devices to be indirectly coupled to a bus. Defendants asserted that PUMA's construction would, thus, allow all the devices shown in the various figures to be "coupled" to a bus. (*Id.* at 12-13). Defendants assert that such an interpretation is an improper reading of "bus." Defendants asserted that as shown in the figures and known in the art, various buses such as the PCI bus 170 and ISA bus 198 are separate buses. (*Id.* at 11, 13, 28). Defendants assert that if "coupled" is used, the term must be "directly coupled." (*Id.* at 30).

PUMA offers various responses to Defendants' assertions. As to whether a "bus" within the meaning of the Asserted Patents can contain a "second bus," PUMA asserts that the relevant claims already contain the limitation "without requiring a second bus." PUMA asserts that this limitation speaks for itself. (Dkt. No. 122 at 2). PUMA also asserts that Defendants' proposal would import the "parallel" limitation into eight of the nine Asserted Patents, even though only two of the patents have claims excluding a second bus. (*Id.*).

As to Cheney, PUMA asserts that Defendants have misread the file history. PUMA asserts that the Applicants were observing that the portion of the prior art identified by the Examiner "refers to the connections as interface line," not a bus. (*Id*. (quoting Dkt. No. 121 Ex. 11 at 6)). PUMA notes that in the subsequent Office Action, the Examiner disagreed with Applicants' characterization and maintained that Cheney discloses a bus. (*Id*. at 2-3 (citing Dkt. No. 122 Ex. B at 2)). PUMA asserts that the Applicants did not reargue the "bus" issue during the subsequent prosecution but rather secured allowance of the claims on other grounds. (*Id*. at 3).

Analysis

The parties do not dispute that the term "bus" is well-known in the art. Defendants seek a construction that adds "parallel" and "broadcast among them" to its well-known meaning. The Court rejects Defendants' proposed construction because including "parallel" and "broadcast among them" does not add clarity to the construction and is not supported by the intrinsic evidence. However, the Court also rejects PUMA's proposed construction because the construction is broader than what is disclosed in the specification.

Fundamentally, Defendants argue that a "bus" must be one set of associated signal lines without intervening modules or components. Defendants assert that if there are intervening components on a "bus," the "bus" must be considered a sequence or series of multiple "buses." Defendants' main objection at the hearing with regard to the term "bus" was not directed toward the meaning of "bus." Rather, Defendants focused on the extent to which other devices may be directly or indirectly "coupled" to a "bus."

Defendants' addition of the words "parallel" and "broadcast" do not show that a "bus" must be unbroken by intervening modules or components. The Court agrees with PUMA that the words "parallel" and "broadcast" have multiple meanings in the art. For example, "serial" and "parallel" buses also have well-known meanings that are different than the "parallel" meaning sought by Defendants. Defendants' "broadcast" requirement would exclude buses such as MBus discussed by PUMA. Defendants have not established, in the intrinsic record, that the ordinary meaning of "bus" has been disavowed or disclaimed, such that the terms "parallel" and "broadcast" should be incorporated into the construction of "bus."

Furthermore, Defendants' focus on the term "coupled" does not change the meaning of the term "bus." For example, the '789 Patent Figure 2 provides that the decoder/encoder 45 is "coupled to the memory 50 through devices, typically a bus 70." '789 Patent 6:29-30. Figure 2 shows that the decoder 45 is indirectly coupled to the memory 50 through an intervening memory interface 48 and a bus 70. The meaning of the term "bus" does not change just because the memory interface 48 and bus 70 separate the decoder 45 and the memory 50. Defendants' arguments appear directed toward the meaning of "coupled" not "bus."

To the extent that Defendants assert that a "bus" cannot be a point-to-point connection between two devices (Dkt. No. 121 at 2, 6-8), Defendants' proposed construction of "broadcast among them" does not include such a limitation. An ordinary reading of Defendants' construction would encompass point-to-point connections between two devices.[2]

Moreover, Defendants' argument that a "bus" excludes a point-to-point connection between two devices is unsupported by the intrinsic evidence. Defendants' argument relies on the Applicants' prosecution history statements regarding the Cheney reference. But Cheney describes a point-to-point connection between two devices as buses. It states: "[t]he interface between the memory management unit 600 and the memory 601 includes an address bus, 221, a bidirectional data bus, 223, and a control bus 225." (Dkt. No. 121 Ex. 9 (U.S. Patent No. 5,576,765) at 7:35-37, Figure 4). Moreover, the statements made by the Applicants regarding Cheney were directed toward a portion of the specification that referenced "interface 221, 223, 225." (*Id*. at 10:29-30). It is clear that elsewhere, Cheney referred to such connections as a "bus." (*Id*. 7:35-37).

[2] Defendants assert that "among them" negates a point to point connection. The Court does not find such language so limiting.

In any event, the Examiner did not accept the Applicants' "interface" argument during prosecution, and the Applicants did not subsequently rely on that argument to secure allowance of the claims. In the context of the prosecution history as a whole, "bus" was not redefined from its ordinary meaning to exclude point-to-point connections. The Court's construction adopted below concludes with "between them." Such language does not prohibit a point-to-point connection and does not require the bus to be coupled to at least three devices

PUMA's construction, however, is also problematic because it could be interpreted to encompass more than what the intrinsic record would teach to be a "bus." For example, the patents illustrate an example of two buses: a PCI bus 170 and an ISA bus 198. '789 Patent Figure 1c. PUMA acknowledges that each of these buses would be considered to be a separate bus. At the oral hearing, PUMA also unequivocally stated that a PCI bus 170 and an ISA bus 198 were two separate buses. (Dkt. No. 137 at 22, 24-25). Further, PUMA stated that one skilled in the art would recognize the buses were separate. (*Id.*). Also, in prosecution, the Applicants distinguished the memory bus 108 and the PCI bus 120 of Lambrecht as being two separate buses.

However, PUMA's construction merely defines a "bus" as "a set of signal lines." If one defined the "bus" as a "set of signal lines," contrary to PUMA's statements at the hearing and contrary to the Applicants' statements during prosecution, the PCI bus 170 and the ISA bus 198 could be considered one "set of signal lines" and argued to form one "bus." Similarly, the two busses in Lambrecht, the memory bus 108 lines and the PCI bus 120 lines, could also be considered to be one "bus." In the context of the patent disclosure, the prosecution history arguments made to distinguish Lambrecht, and the acknowledgements made by PUMA during the oral hearing, such an interpretation of "bus" is not correct.

As shown in the patents and the prosecution history, the "set of signal lines" is not just any lines chosen randomly to form "a set." Rather, the "set" is a set of associated lines, for example the PCI bus lines, ISA bus lines, or memory bus lines, each being a separate set. The Court's construction requires the set of signal lines to be "a set of associated signal lines."[3]

The Court construes "bus" to mean "a signal line or a set of associated signal lines to which a number of devices are coupled and over which information may be transferred between them."

2. "real time" ('789 Patent claim 1, 13; '315 Patent claim 1 and '164 Patent claim 1, 6)

PUMA's Construction	Defendants' Construction
"fast enough to keep up with an input data stream"	Indefinite: Alternatively: "fast enough to keep up with an input data stream, wherein obtaining bus mastership does not consume bus cycles"

The fundamental dispute raised relates to the question whether prosecution history statements rendered the term "real time" indefinite.

Positions of the Parties

PUMA notes that, in *STMicroelectronics*, the Court construed "real time" to mean "processing fast enough to keep up with an input data stream." *STMicroelectronics*, 327 F. Supp. 2d at 693, 710-711. PUMA asserts that this construction comports with the intrinsic and extrinsic evidence.

[3] At the oral hearing PUMA agreed to the Court's suggested use of "associated." (Dkt. No. 137 at 5, 22).

PUMA asserts that the patent specifications state that "[i]f the decoder does not operate in real time the decoded movie would stop periodically between images until the decoder can get access to the memory." '789 Patent at 3:21-24. PUMA also cites to the passage:

> A goal is to have the decoder/encoder 45 operate in real time without dropping so many frames that it becomes noticeable to the human viewer of the movie. To operate in real time the decoder/encoder 45 should decode and/or encode images fast enough so that any delay in decoding and/or encoding cannot be detected by a human viewer. This means that the decoder/encoder 45 has a required bandwidth that allows the decoder/encoder 45 to operate fast enough to decode the entire image in the time between screen refreshes, which is typically 1/30 of a second, with the human viewer not being able to detect any delay in the decoding and/or encoding.

Id. at 6:41-52. PUMA also cites to an IEEE dictionary and to the *STMicroelectronics* characterization that "[t]he relevant dictionary definition indicates that real time concerns the processor's ability to 'keep up with' the data input." (Dkt. No. 120 at 11 (quoting *STMicroelectronics*, 327 F. Supp. 2d at 693)).

PUMA asserts that the specification informs a person of skill in the art with "reasonable certainty" of the scope of the invention. PUMA further notes that the Defendants' own expert uses the term "real time" in a variety of his own publications. (Dkt. No. 120 at 12).

Defendants do not dispute that, apart from the patents, "real time" can have meaning. Defendants assert that although "real time" has a well-known meaning in the art, the Applicants adopted a narrower definition of the term by making statements regarding "bus latency" during the prosecution of the '164 Patent in 2013. Defendants assert that this recent, contradictory, and confusing portion of the intrinsic record renders "real time" indefinite under *Nautilus*. (Dkt. No. 121 at 10-11).

Defendants assert that the asserted patents use "real time" to qualify how a bus transfers data between a decoder and a memory. Defendants assert that every disclosed embodiment

includes a "fast bus" to permit real time operation. (*Id*. at 11). Defendants assert that the specification defines a fast bus in the context of having sufficient bandwidth to operate in real time. (*Id*.). Defendants assert that, according to the specification, whether a bus permits data transfers in "real time" is determined from the bus's bandwidth. Defendants note that an example of a "real time bus" disclosed in the specification is the PCI bus and that some patents in the '459 Patent family explicitly claim a PCI bus as satisfying the real time requirement. (*Id*. at 12, n. 10). Defendants note that even PUMA's expert, Dr. Mangione-Smith, admits that the patents describe bandwidth as the key bus performance factor and that the patents do not appear to be concerned with latency. (*Id*. at 12 (citing Dkt. No. 120 Ex. J at ¶29)).

Defendants assert that the Applicants made arguments, during the '164 Patent prosecution, that contradict the specification and Dr. Mangione-Smith's statements. Specifically, Defendants assert that the Applicants argued that (1) a bus's latency, irrespective of bandwidth, determines the "real time" requirement and, as a result, (2) a PCI bus does not satisfy the "real time" requirement. (Dkt. No. 121 at 12). Defendants point to the following statement from the prosecution of the '164 Patent:

> . . . *Gulick's* PCI devices must communicate with the main memory using **PCI bus 120, which is not a real time bus**. *Gulick* at 5:29-38. **Instead, the PCI devices 142, 144, 146 must obtain bus mastership, which consumes PCI cycles**. *Id.* The PCI devices in *Gulick's* FIG. 1 may communicate data between each other in real-time using the multimedia bus 130, but **this is different from claim 1, which calls out a memory bus configured to pass data in real time between a shared main memory and a decoder/encoder.**

(Dkt. No. 121 Ex 13 at 02591) (emphasis added). Defendants assert that the Applicants' reference to consumption of PCI cycles to obtain bus mastership is a reference to bus latency, a concept that is separate from bus bandwidth. Defendants assert that PCI is an industry standard and has the same potential bandwidth regardless of whether it is recited in Gulick or the Asserted

Patents. Defendants assert that the Applicants distinguished Gulick's PCI bus from the Asserted Patents based on latency, regardless of bandwidth, contrary to the specification. (Dkt. No. 121 at 13). Defendants assert that the Applicants' reliance on latency alone to evaluate "real time" created a new, undefined latency requirement.

Defendants assert that the Applicants' prosecution statements force a person skilled in the art to guess as to the meaning of "real time." Defendants assert that it is unclear whether "real time" means bandwidth, latency, or both. Further, Defendants assert that, as to latency, there is no disclosure as to how much latency is allowed. (*Id*.). Defendants cite to their expert as identifying three uncertainties: whether real time covers (1) a PCI bus, (2) buses that meet the bandwidth requirement, or (3) buses having some undefined latency requirement. (*Id*. at 13-14).

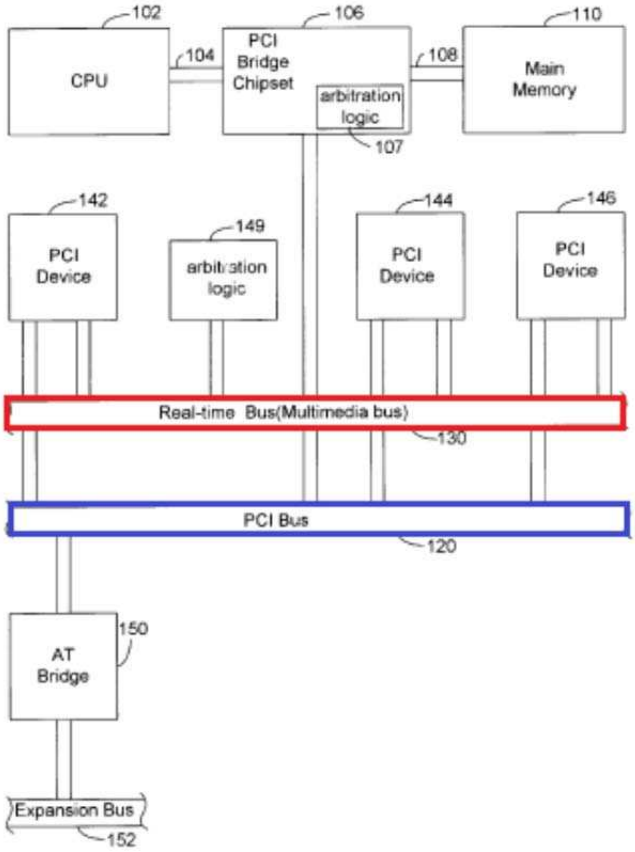
Defendants assert that PUMA's expert analysis is flawed. Specifically, Defendants assert that PUMA's expert uses circular logic. First, the expert limits the analysis to the specific context of a disclosed embodiment. Then, the expert states that Gulick is concerned with a broader range of applications than disclosed in the patents.

Defendants assert that nothing in the claims or specification supports this "context" distinction. Defendants assert that PUMA's expert then applies Gulick's "real time" performance gauge (latency) to distinguish Gulick from the pending claims. (*Id*. at 14). Defendants assert that the patents' real time performance gauge (bandwidth) should have controlled whether a PCI bus is "real time." Defendants assert that, in contrast, the Applicants affirmatively distinguished Gulick's PCI bus based on latency. (*Id*.).

Defendants assert that if the term is definite, PUMA must be held to the new latency requirement. Thus, Defendants assert that their construction is appropriate, if the term is found

definite. (*Id*. at 15). At the oral hearing, Defendants asserted that their "real position" is that the alternative construction should be adopted. (Dkt. No. 137 at 44-45).

In response, PUMA asserts that Defendants misread the prosecution history. PUMA asserts that in the prosecution, PUMA did not distinguish Gulick on the basis of using a PCI bus. Rather, PUMA asserts Gulick was distinguished on the basis that the PCI bus, as used in the specific context of Gulick, is insufficient for real time performance. (Dkt. No. 122 at 3 (citing Dkt. No. 122 Ex. D (Mangione-Smith Decl.) at ¶26)). PUMA points to Gulick Figure 1:



(Dkt. No. 122 at 4 (color coding added)). PUMA notes that Gulick included a real time bus 130 in addition to the PCI bus 120. PUMA asserts that, thus, Gulick itself represented that the PCI bus, as used in Gulick, was insufficient to guarantee real time performance. PUMA asserts it was the Gulick reference which raised the concern of latency in context of the specific system of

Gulick. PUMA asserts that the Applicants did not generally characterize "PCI bus" but rather characterized the specific use in Gulick. (*Id.*). PUMA asserts that the fact that Gulick represents that its PCI bus was not a real time bus has nothing to do with the parameters of PCI buses in general. Rather, PUMA asserts that Gulick shows that the specific context in which the PCI bus was used in Gulick establishes that the bus was not a real time bus. (*Id.*).

Analysis

The parties agree that the specification is clear. *See, e.g.*, '789 Patent 3:21-24, 6:41-52. Further, both PUMA and the Defendants agree that, as to the specification, the Court's construction in *STMicroelectronics* applies to this case. Against this backdrop, Defendants read more into the '164 Patent prosecution history than is proper.

Prosecution arguments, by nature, are often not clear. *Phillips*, 415 F.3d at 1317 (noting that the prosecution history represents an "ongoing negotiation" and "often lacks the clarity of the specification"). In order to show that the Applicants disavowed the well-known meaning of a term in the art, the prosecution history must show that the patentee clearly and unambiguously disclaimed or disavowed its meaning during prosecution to obtain claim allowance. *Middleton, Inc. v. Minn. Mining & Manuf. Co.*, 311 F.3d 1384, 1388 (Fed. Cir. 2002).

Here, the disputed prosecution history relates to the Gulick reference. The Defendants claim that the Applicants secured claim allowance by distinguishing Gulick on the grounds that Gulick's PCI bus did not allow for real time processing due to its latency. However, as evident from Figure 1 of Gulick (*see* Dkt. No. 122 at 4 (color coding added)) the system in Guilck provided a real time bus in addition to a PCI bus. Thus, as shown in Gulick Figure 1 and stated in Gulick, a "Real-time Bus (Multimedia bus) 130A" is provided to operate as "a dedicated real-time bus or multimedia bus" in addition to the PCI bus 120. (Dkt. No. 122 Ex. C (Gulick) Figure

1, 2:54-56). In context, clear statements of disclaimer regarding the bandwidth of the PCI bus were not made. The proper context to consider is (1) the prosecution history statements directed toward the particular overall prior art system of Gulick; and (2) the clear specification statements. In this context, real time has not been redefined in opposition to the specification.

The meaning of "real time," as found in the specification, is consistent with the *STMicroelectronics* construction: "fast enough to keep up with an input data stream."

The Court construes "real time" to mean "fast enough to keep up with an input data stream."

3. "fast bus" ('368 Patent claim 7 and '045 Patent claim 4)

PUMA's Construction	Defendants' Construction
"bus with a bandwidth equal to or greater than the required bandwidth to operate in real time"	Indefinite. Alternatively: "bus having a bandwidth greater than the bandwidth required for the decoder to operate in real time"

Positions of the Parties

PUMA points to two definitional passages in the specification: "a fast bus 70 is any bus whose bandwidth is equal to or greater than the required bandwidth" ('459 Patent 8:1-2) and "two devices are coupled to the memory through a fast bus having a bandwidth of at least the minimum bandwidth needed for the video and/or audio decompression and/or compression device to operate in real time" ('459 Patent at 4:59-62). PUMA asserts that "real time," as used in PUMA's construction, is definite for the reasons PUMA argues separately with regard to the "real time" term. (Dkt. No. 120 at 14). PUMA objects to Defendants' removal of the "equal to" language from the construction. PUMA points to the language quoted above in which a fast bus has "at least the minimum bandwidth." (*Id*.).

Defendants assert that to the extent "real time" is found to be indefinite, "fast bus" would also be indefinite. Defendants assert that their construction comes straight from the patents: "[t]he decoder/encoder 80 is coupled to the memory 50 through devices, typically a bus 70[4], that have a bandwidth greater than the bandwidth required for the decoder/encoder 80 to operate in real time." '459 Patent at 7:39-42.

Analysis

The primary issue presented by the parties is whether "real time" is definite. This dispute has been decided above with regard to the term "real time."

As to the dispute regarding "equal to or greater" versus "greater," the specification provides guidance. In one passage, bandwidth is described as being "equal to or greater than the required bandwidth." '459 Patent 8:1-2. Similarly, elsewhere "at least the minimum" is used. '459 Patent at 4:59-62. In one passage, the patent uses "greater than." '459 Patent at 7:39-42. However, this passage does not negate or disavow the other broader descriptions. Defendants' construction of "greater" would exclude the "equal to or greater" and "at least the minimum" passages. Defendants have not pointed to any reasons to exclude the broader disclosure that is provided in the specification.

The Court construes "fast bus" to mean "bus with a bandwidth equal to or greater than the bandwidth required to operate in real time."

[4] Defendants assert that the patents use reference number 70 for "bus" and "fast bus" interchangeably. (Dkt. No. 121 at 9, n.3).

4. Coupled Terms

"coupled" ('789 Patent claims 1, 5; '368 Patent claims 1, 7, 13, 19, 20; '045 Patent claims 1, 4, 5, 12; '753 Patent claims 1, 7; '315 Patent claim 1, 13, 15 and '164 Patent claims 1, 8, 9, 11)

"coupleable" ('045 Patent claims 1, 4, 12; '753 Patent claim 7; '315 Patent claim 1 and '164 Patent claim 1)

"coupling" ('789 Patent claim 1 and '194 Patent claims 1, 16, 17)

PUMA's Construction	Defendants' Construction
a. "directly or indirectly connected" b. "directly or indirectly connectable" c. "directly or indirectly connecting"	a. "attached resulting in an arrangement that includes no more than one bus" b. "attachable resulting in an arrangement that includes no more than one bus" c. "attaching resulting in an arrangement that includes no more than one bus"

The primary issues in dispute relate to whether the construction of "coupled" should include indirect connections and whether the term encompasses no more than one bus.

Positions of the Parties

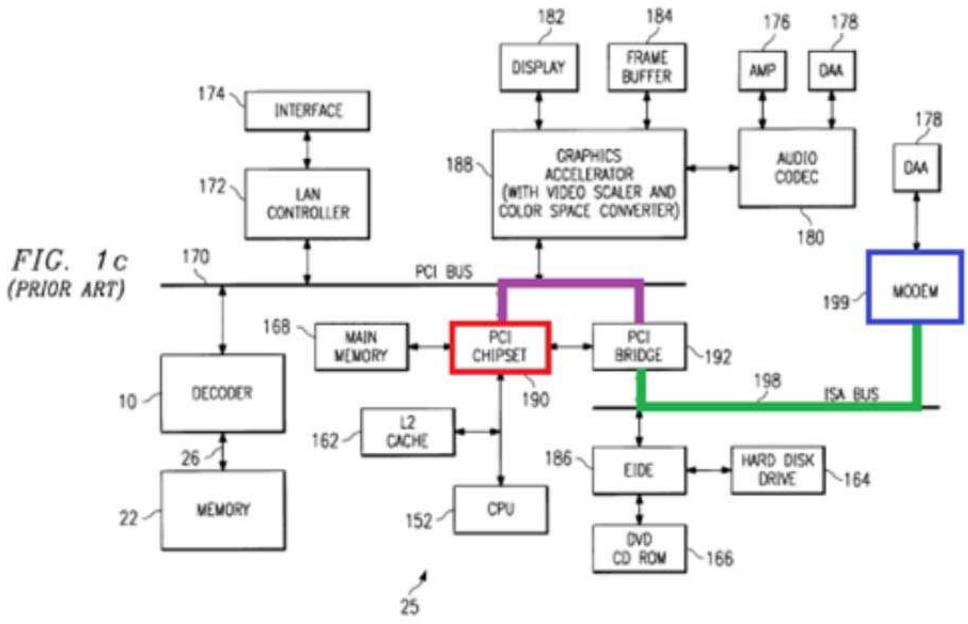
PUMA cites to three Eastern District of Texas cases which have construed "coupled" to mean directly or indirectly connected. (Dkt. No. 120 at 15-16). PUMA also asserts that the specifications utilize "coupled" to reference elements that are indirectly connected. For example, PUMA cites to '789 Patent Figure 1b which shows a memory interface 18 that connects to an audio decoding circuit 14, and the audio decoding circuit 14 is, in turn, connected to a memory 22. PUMA notes that the specification states that the "memory interface 18 is coupled to memory 22." '789 Patent 2:25. Similarly, PUMA points to '789 Patent Figure 2 which shows a decoder/encoder 45 connected to a memory interface 48, and shows the memory interface 48, in turn, connected to memory 50. PUMA notes that the specification states that "decoder/encoder 45 is coupled to the memory 50 through devices, typically a bus 70." *Id*. 6:29-30. PUMA notes

that the ’459 Patent has similar passages. (Dkt. No. 120 at 17 (citing ’459 Patent 2:28, 7:39-42)). PUMA also notes that the patents use “coupled” to refer to direct connections such as in ’789 Patent Figure 2: “DMA engine 60 of the first device is coupled to the arbiter 54 of the memory interface 48.” ’789 Patent 6:15-17.

PUMA objects to Defendants’ construction as being directly contradicted by the specification. Specifically, PUMA asserts that Defendants’ construction does not include indirect attachments. (Dkt. No. 120 at 17). PUMA also objects to Defendants’ “resulting in an arrangement that includes no more than one bus.” PUMA asserts that it is unclear what components are included or not included in an “arrangement.” PUMA asserts that the Asserted Patents do not use “coupled” is such a manner. (Dkt. No. 120 at 17-18). PUMA also asserts that Defendants’ “arrangement” language conflicts with the specification. Specifically, PUMA points to the language referencing ’789 Patent Figure 1c:

> Fig. 1c shows a computer 25 containing a decoder 10, a main memory 168 and other typical components such as a modem 199, and graphics accelerator 188. The decoder 10 and the rest of the components are coupled to the core logic chipset 190 through a bus 170.

’789 Patent 2:49-53. PUMA asserts, however, that as shown in Figure 1c, the modem 199 is “coupled” to the core logic chipset 190 through bus 170 and bus 198. PUMA asserts that, in such a case, the modem is coupled to the core logic chipset in an “arrangement” that includes two buses. (Dkt. No. 120 at 18). PUMA asserts that Defendants’ construction is directly contradicted by Figure 1c and the corresponding specification passages. PUMA illustrates Figure 1c

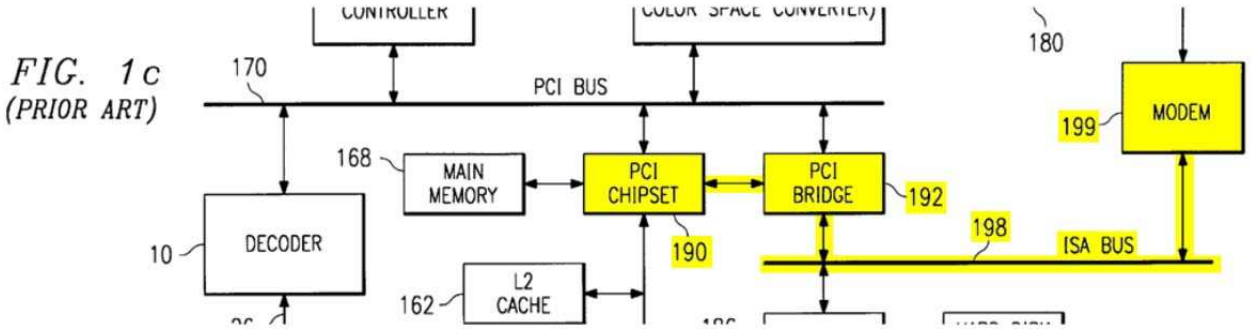


’789 Patent Figure 1c (color coding added). PUMA asserts that the figure shows that the modem 199 is coupled to the core logic chipset 190 through ISA bus 198 and PCI bus 170. (Dkt. No. 122 at 5). PUMA asserts that Defendants’ position, that the connection between the core logic chipset 190 and PCI bridge does not use the PCI bus 170, is contradicted by the specification. Specifically, PUMA points to the specification passages which state “the components are coupled to the core logic chipset 190 through a bus 170” (’789 Patent 2:52-53) and the PCI bridge 192 “bridges between the PCI bus 170 and the ISA bus 198.” (’789 Patent 9:33-34).

Defendants assert that the issue is not whether both indirect and direct connections are encompassed by “coupled.” Defendants assert that the real issue is whether or not “coupling” includes more than one bus. (Dkt. No. 121 at 15). Defendants assert that PUMA divorces the term “coupled” from its use in the specification and claims. Defendants assert that the claims only refer to attachments that involve no more than one bus and assert that the specification consistently shows embodiments that involve no more than one bus. (Dkt. No. 121 at 16-17).

Defendants assert that “coupled” is used 236 times in the ’789 Patent and file history and

47 times in the ’459 Patent and file history. Defendants assert that in every instance, “coupled” refers to an attachment that includes no more than one bus. (Dkt. No. 121 at 17). Defendants assert that in all cases, the coupling refers to (1) two components directly connected with no bus, (2) two components having a single bus between the components, or (3) a component connected to a bus. (*Id.*). Defendants assert that every usage of “coupled” is an arrangement that includes no more than one bus. As to PUMA’s reference to Figure 1c, Defendants assert that the modem 199 is connected to the PCI chipset 190 only through ISA bus 198 and PCI bridge 192 (not PCI bus 170):



’789 Patent Figure 1c (figure truncated and color coding added).

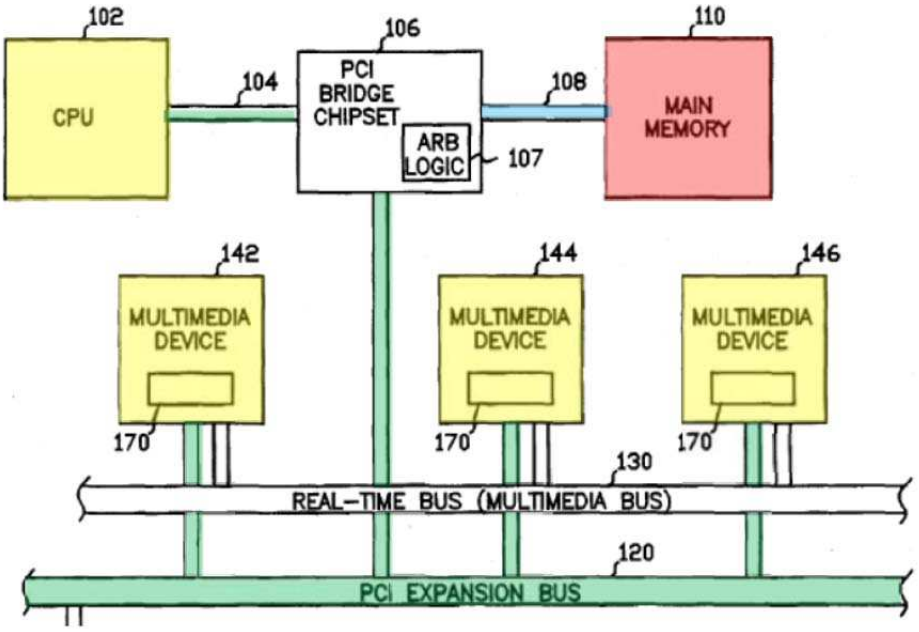
Defendants also assert that many of the claims refer to just one bus and use “couple” to reference a device “coupled” to the bus. (Dkt. No. 121 at 19-20 (citing ’789 Patent claim 1, 13; ’368 Patent claim 1)). Defendants note that some claims refer to more than one bus but assert that the claim language always references a “coupling” to a specific bus. (*Id*. at 20).

Defendants assert that the prosecution history describes “coupled” as an attachment involving no more than one bus. Defendants point to ’459 Patent file history statements regarding the Lambrecht reference. (Dkt. No. 121 at 21). In particular, Defendants assert that during prosecution of the ’459 Patent, the pending claims included “a decoder coupled to the first

memory to provide direct access to the first memory." (Dkt. No. 121 Ex. 5 at 0756).

The Examiner rejected these claims based on Lambrecht, and Defendants assert that the Applicants overcame this rejection by stating: "[t]he present claims are directed toward systems and methods for providing direct access for a first device and decoder to a first memory. . . .Unlike the claimed invention, [Lambrecht] uses a PCI bridge chipset for access between other first devices or decoders and a main memory." (Dkt. No. 121 Ex. 5 at 0763-64).

Defendants assert that the Applicants' argument to the Examiner was that Lambrecht did not provide "direct access" because two buses are used to connect devices to the memory (bus 108 and bus 104 or bus 108 and bus 120). Defendants point to the Lambrecht Figure 1 as an example:



(Dkt. No. 121 Ex. 3 Figure 1) (figure truncated and color coding added).

Defendants also assert that in prosecution, the Applicants rejected the notion of "indirect" coupling. Defendants point to the '368 Patent prosecution statement in which the Applicants

characterized the "present invention" as having "both decoder 80 and the device 42. . .**directly coupled** to the fast bus 70, which in turn is coupled to the memory 50." (Dkt. No. 121 Ex. 14 at 01256) (emphasis added). Further, at the oral hearing, the Defendants emphasized that in the Applicants' Appeal Brief to the Board of Patent Appeals and Interferences, the Applicants stated: "[a]ccording to the **present invention**, the microprocessor 42 and the video decoder 80 obtain access to the main memory 50 via the **same** fast bus 70. . . ." (Dkt. No. 121 Ex. 15 at 1278) (emphasis added).

Defendants further assert that in addition to Lambrecht, the Applicants distinguished other references as not providing "direct access" between the decoder and memory. Specifically, Defendants point to claims that contain the phrase "communicatively linked. . .without requiring a second bus" ('459 Patent and '194 Patent). (Dkt. No. 121 at 22 (citing Ex. 5 at 0763-64)). Defendants assert that the Applicants made the same arguments with regard to the "communicatively linked" claims as they made with regard to the "coupled" claims ('368 Patent). (*Id*. (citing Ex. 15 at 01282)). Defendants assert that because the Applicants made the same argument, the Applicants clearly intended "coupled" to mean without requiring a second bus. (*Id*.).

Defendants assert that other district court cases have little relevance, as here the specifications' consistent usage of "coupled" indicates an arrangement with no more than one bus. Defendants assert that PUMA's boundless construction of "coupling" provides no guidance to the jury. Defendants assert that, in the claims, the word "coupled" is used in the context of connecting or attaching components. (Dkt. No. 121 at 23).

Analysis

Defendants do not contest that the well-known meaning of "coupled" includes devices

that are both directly and indirectly connected. Defendants argue that the well-known meaning of "coupled" does not apply because all the disclosed embodiments show connections with only one bus.[5] However, even if specification discloses embodiments with only one bus, incorporating that limitation into the Court's construction is not mandated. *See Arlington Indus., Inc. v. Bridgeport Fittings, Inc.*, 632 F.3d 1246, 1254 (Fed. Cir. 2011) ("[E]ven where a patent describes only a single embodiment claims will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using words of expressions of manifest exclusion or restriction" (citation omitted)).

Indeed, the Applicants repeatedly use the term "coupled" in a manner consistent with its well-known meaning. For example, in the '789 Patent, the memory interface 18 of Figure 1b is described as "coupled" to memory 22. Yet, the path between the memory interface and the memory includes at least the audio decoding circuit and a bus between the audio decoding circuit and the memory. '789 Patent 2:25, Figure 1b.

Likewise, in the '789 Patent Figure 2, the decoder/encoder 45 is "coupled" to the memory 50 despite multiple intervening "devices" such as the memory interface 48 and bus 70. *Id.* Figure 2, 6:29-32. Similarly, the '789 Patent describes the modem 199 as "coupled" to the core logic chipset 190, despite the two components being linked through two busses: the ISA bus and the PCI bus. '789 Patent Figure 1c, 2:49-53. Although the parties dispute the proper interpretation of '789 Patent Figure 1c, the Court finds that the specification directly supports PUMA's interpretation. *See* '789 Patent Figure 1c, Figure 4, 2:49-53, 9:33-34.

[5] At the oral hearing, Defendants made assertions regarding "coupled" with regard to the "bus" disputes. Defendants asserted that PUMA's construction would provide no limits to coupling, asserting that PUMA's construction effectively has all the devices shown in the figures "coupled." (Dkt. No. 137 at 12-13). The Court rejects Defendants' assertions. The evidence submitted does not indicate that an interpretation by one skilled in the art would reach such a broad conclusion.

Finally, the Court notes that the ’368 Patent describes an alternative embodiment for Figure 7 in which peripherals such as the modem 199, disk drive 164 and DVD CD-ROM 166 are “coupled directly” to the PCI chipset. ’368 Patent at 12:65-13:5, Figure 7. Such “direct coupling” is achieved by incorporating the EIDE interface 186 into the PCI chipset 190 and eliminating the PCI bridge 192 and ISA bus 198. *Id.* This passage implies that absent the modifier “directly,” the word “coupled” has a broader meaning than the phrase “directly coupled.”

As the Court described above, the specification of the Asserted Patents applies the well-known meaning of “coupled.” However, Defendants argue that for four reasons the Applicants disavowed or disclaimed the well-known meaning “coupled” and adopted a definition that permits “coupling” only via one bus. The Court rejects each of these arguments in turn.

First, Defendants’ “direct access” arguments with regard to ’459 Patent and ’194 Patent prosecution history are not persuasive. The Applicants discussed “direct access” in the ’459 Patent prosecution because the Applicants added express claim limitations of “direct” access and “without also requiring a second bus.” (Dkt. No. 121 Ex. 5 at PUMA 0756, 0762-64); ‘459 Patent claim 1.

Second, with regard to the Applicants’ use of “directly coupled” in the ’368 patent’s prosecution history, the cited response indicates that the Applicants used the phrase to describe the arbiter’s ability to directly control the decoder’s and other devices’ access to memory. (Dkt. No. 121 Ex. 14 at 01256). Defendants accurately state that the Applicants describe the devices in an embodiment of the figures as “directly coupled” to the fast bus. But the Court finds that this statement does not create a global disclaimer to the well-known meaning of “coupled.” Rather, the Court finds that it is an example of the Applicants’ describing a particular embodiment of the

figure to the Examiner. Moreover, the example is not limiting because the Applicants' use of "direct" coupling again implies that "coupled" means more than "direct" coupling. *See Phillips,* 415 F.3d at 1314 ("[T]he claim term in this case refers to 'steel baffles,' which strongly implies that the term 'baffles' does not inherently mean objects made of steel.").

Third, as to the "present invention" language in the '368 Patent prosecution, the Court finds that such language also does not redefine "coupled." The first passage cited by Defendants emphasizes whether arbitration is "decoupled" from bus access. It does not state that all devices that are "coupled" must be "directly coupled" on the same bus. Specifically, the passage in question states "[i]n the present invention, arbitration is decoupled from bus access." (Dkt. No. 121 Ex. 14 at 01256). It then goes on to describe devices that are both "directly coupled" and "coupled" to the bus. (*Id*. ("decoder 80 and the device 42 are directly coupled to the fast bus, which in turn is coupled to the memory 50")). Nowhere in this passage do the Applicants adopt a one bus limitation to the term "coupled."

Finally, as to the statement in the '368 Patent Appeal Brief that "according to the present invention" several devices are connected to the same fast bus, the Court finds that the Applicants' statement was made in the course of explaining Figure 2. Indeed, the Applicants expressly next state that Figure 2 "provides one example of the inventive features." (Dkt. No. 121 Ex. 15 at 01277). Because Figure 2 is just an "example" of the claimed invention, on the whole, the Applicants' statement in the Appeal Brief does not show an unmistakable intent to disavow or disclaim the well-known meaning of "coupled." (*Id*. at 1277-79; *see also Pacing Techs., LLC v. Garmin Int'l, Inc.*, 778 F.3d 1021, 1025 (Fed. Cir. 2015) (finding disclaimer when the applicant states that one embodiment accomplishes all of the objects of the invention)). In the context of the overall intrinsic record, including the specifications and various file history

statements, a clear disclaimer of the term "coupled" was not made.

The court construes "coupled" to mean "directly or indirectly connected," "coupleable" to mean "directly or indirectly connectable," and "coupling" to mean "directly or indirectly connecting."

5. "directly supplied" ('194 Patent claim 15 and '368 Patent claim 3) and "directly supplies" ('368 Patent claim 2, 14, 21; '045 Patent claim 2, 6, 13; '753 Patent claim 3)

PUMA's Construction	Defendants' Construction
No construction necessary. Alternatively: a. "supplied without being stored in main memory for purposes of decoding subsequent images" b. "supplies without being stored in main memory for purposes of decoding subsequent images"	a. "provided via a single bus with no intervening components" b. "provides via a single bus with no intervening components"

The dispute between the parties relates to whether "directly supplied" describes the physical connection of the components or describes the decoding method in which some frames are not sent to the main memory for subsequent use to decode other frames.

Positions of the Parties

PUMA asserts that "directly supplied" concerns the system's use of decompressed frames in the context of video coding. PUMA asserts that the phrase "directly supplied" means that certain types of frames do not need to be transferred to main memory for use in the subsequent decoding of other frames. PUMA asserts that Defendants' arguments take the term out of context. (Dkt. No. 120 at 18-19). PUMA asserts that, contrary to Defendants' position, the term

"directly supplied" has nothing to do with architectural limitations or the absence of "intervening components."

PUMA points to '194 Patent claim 14 as illustrative of its position that the term "directly supplied" refers to whether frames must be transferred to memory for use in decoding other frames. Claim 14 states that a "decoder directly supplies a display adapter of the display device with an image for use other than decoding a subsequent image." PUMA also notes that the '194 Patent claim 15 states: "the images directly supplied to the display adapter being bidirectional images obtained from two preceding intra and predicted images." PUMA asserts that the term "directly supplied" must be viewed in context of MPEG bidirectional decoding which uses video frames stored in memory to decode other frames. (*Id*. at 19).

PUMA notes that MPEG video includes I-frames, P-frames, or B-frames. I-frames (intra-coded frames) are images that do not require data from other frames. P-frames (predicted frames) use data from previous frames. B-frames (bidirectional frames) use data from both previous and forward frames. (*Id*.). PUMA notes that the specification states "[t]he intra and predicted images are likely to be used to reconstruct subsequent predicted and bidirectional images, while bidirectional images are not used again." '194 Patent 3:21-25. PUMA asserts that the specification thus notes that "a buffer associated with bidirectional images is not required, these bidirectional images B being directly supplied to display adapter 120 as they are being decoded." '194 Patent 10:39-42. PUMA notes that the patent also states: "[i]n the case where the compressed data correspond to bidirectional images, the decoder/encoder 80 decodes these data and directly supplies display adapter 120 with the decoded data." '194 Patent 10:48-51. PUMA asserts that it is because a bidirectional image is not used to reconstruct subsequent predicted or

bidirectional images that the bidirectional image can be "directly supplied" to the display adapter. (Dkt. No. 120 at 20).

Because the term "directly supplied" relates to whether bidirectional images must be stored in memory, PUMA asserts that the term is not intended to be a limitation on the physical architecture or to exclude the use of intervening components. PUMA asserts that Defendants' construction would exclude disclosed embodiments that include intervening components. Specifically, PUMA points to '194 Patent Figure 3:

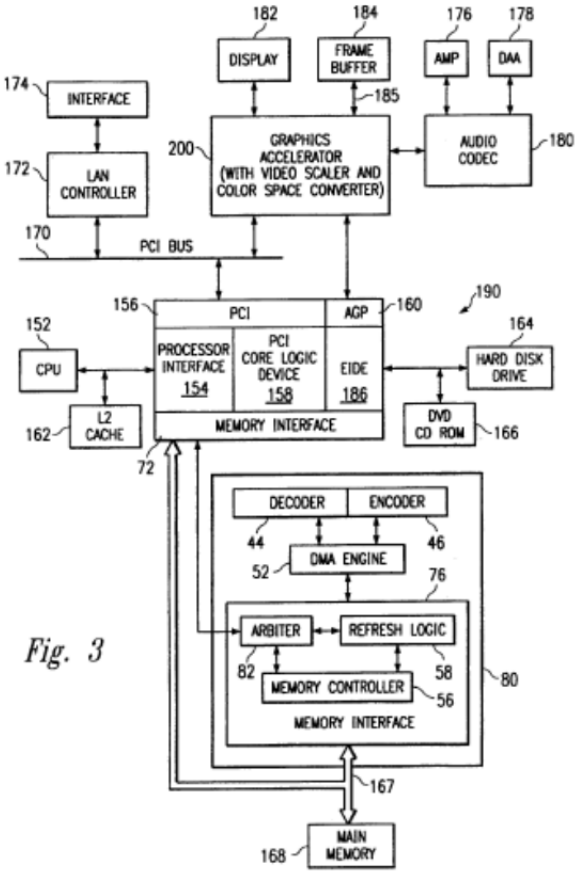


Fig. 3

'194 Patent Figure 3. PUMA asserts that in Figure 3, the decoder/encoder 80 is connected to the graphics accelerator 200 and the display 182 through the core logic chipset 190. PUMA asserts that Defendants' construction would not encompass this embodiment due to the intervening core logic chipset 190 and the use of multiple buses. (Dkt. No. 122 at 6-7). PUMA asserts that

Defendants' added phrase "with no intervening components" is directly at odds with the specification and would read out every embodiment in which an intervening bus is used to transfer data from the decoder to the display adapter. (Dkt. No. 120 at 21). PUMA asserts that the patents do not use "directly supplied" in the context of no other intervening components and a single bus. PUMA asserts that the only use of "directly supplied" is in the context of bidirectional decoding.

Defendants assert that images are directly supplied to a display adapter from a decoder. Defendants assert that '194 Patent Figure 4 illustrates how bidirectional images "B" are provided from the decoder/encoder 80 to the video controller 120.

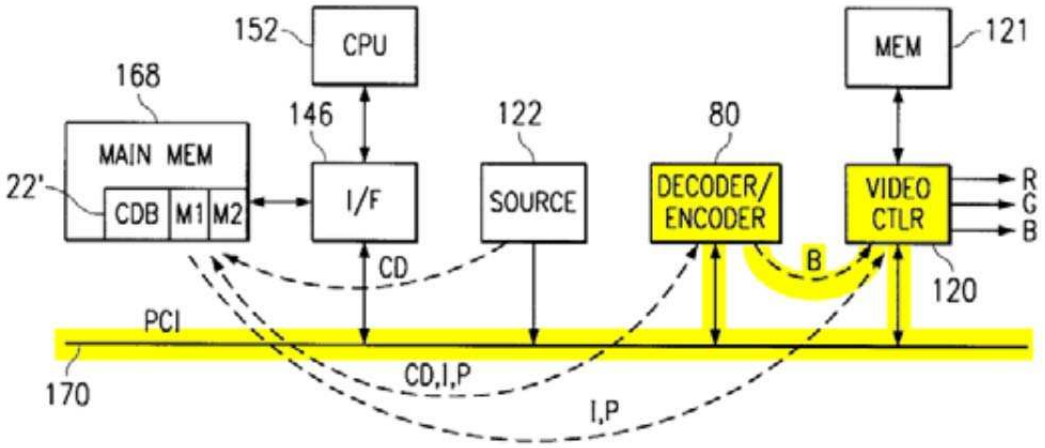


FIG. 4

'194 Patent Figure 4 (color coding adding). Defendants point to the specification description, which states that for bidirectional images "the decoder/encoder 80 decodes these data and directly supplies display adapter 120 with the decoded data." '194 Patent 10:48-51. Defendants assert that the decoder "directly supplies" the images, because the images are sent via a single bus with no other intervening components. (Dkt. No. 121 at 24).

Defendants assert that PUMA's construction ignores the plain language of the claim read in light of the specification. Defendants assert that the claims are clear: "the images directly supplied to the display adapter being bidirectional images." '194 Patent claim 15. Defendants assert that this is shown by the "B" image path in Figure 4. Defendants assert the bidirectional image "B" is directly supplied, not simply because it is "not used in coding subsequent or bidirectional images," but because it is supplied via a single bus with no other intervening components. Defendants assert that this is in contrast to the prior art Figure 1c where the bidirectional images are stored in the decoder's memory 22 and must pass through the decoder before reaching the video controller 120. (Dkt. No. 121 at 25). At the oral hearing, Defendants asserted that Figure 3 is not relevant as "directly supplied" is only used in passages describing Figure 4. (Dkt. No. 137 at 76-77).

At the oral hearing, Defendants further objected to PUMA's use of "main memory." Defendants asserted that in some claims "main memory" is not utilized, rather the claims utilize "a memory" or "system memory." (Id. at 76 (noting that '194 Patent claim 11 and '368 Patent claim 21 use "a memory" and that '368 Patent claim 14 and '045 Patent claim 6 use "system memory")).

Analysis

The claim terms arise in the context of decoded images. The specification passages in which "directly supplied" is utilized provide guidance as to the term's meaning in the context of the specification.

> FIG. 4 shows another embodiment of a computer where the decoder/encoder 80 is sharing the main memory 168. In this embodiment, the main memory 168 corresponds to the shared memory 50 of FIG. 2. In FIG. 4, the decoder/encoder 80 according to the present invention is connected as a peripheral to a conventional computer equipped with a fast peripheral bus 170, for example, a PCI bus, although the bus can be VESA Local Bus (VLB), an Accelerated Graphics Port

> (AGP) bus, or any bus having the required bandwidth. In this embodiment, the fast peripheral bus 170 corresponds to the fast bus 70. **As shown, the decoder/encoder 80 does not have a dedicated memory, but utilizes a region 22' of the main memory 168 of the computer.**
>
> Region 22' includes a Compressed Data Buffer (CDB), into which image source 122 writes the compressed image data, and **two image buffers M1 and M2 associated with intra or predicted images. As will be seen hereafter, a buffer associated with bidirectional images is not required, these bidirectional images B being directly supplied to display adapter 120 as they are being decoded.**
>
> Thus, in the system of FIG. 4, compressed or coded data CD are transferred from image source 122 to buffer CDB of memory 168. **These same compressed data are then transferred to the decoder/encoder 80 which, if they correspond to intra or predicted images, retransmits them in decoded form to buffers M1 and M2 of memory 168. In the case where the compressed data correspond to bidirectional images, the decoder/encoder 80 decodes these data and directly supplies display adapter 120 with the decoded data.** The display adapter then supplies these data to a display device such as a screen. **The intra or predicted images stored in buffers M1 and M2 are transferred to display adapter 120 at the appropriate time and are used in the decoding of subsequent predicted or bidirectional images.**

’194 Patent 10:22-56 (emphasis added). These passages above show that bidirectional images are not decoded by the decoder and then provided to the main memory for later transfer to the display adaptor. Rather, bidirectional images are provided from the decoder to the display adaptor without storage in the main memory. The bypassing of the main memory is the context in which “directly supplied” is utilized in the specification.

Defendants’ emphasis of “no intervening” components lacks support in the specification. First, in all embodiments, the decoder provides the bidirectional images to the display adaptor through an intervening bus. Thus, Defendants’ “directly supplied” architecture approach needs the qualification contained in Defendants’ proposed construction (“via a single bus”).

Second, as noted by PUMA, the Figure 3 embodiment teaches the use of intervening components, the core logic chipset, in addition to the multiple buses (the memory bus 167 and

PCI bus 170). ’194 Patent Figure 3, 9:53-10:21. The Court rejects Defendants’ argument that the Figure 3 embodiment is not relevant to the discussion of the frames of Figure 4. Although the movement of the MPEG I, P, and B frames is shown with regard to Figure 4, the context of the specification indicates that Figures 2 and 3 would also be relevant to MPEG frames.

For example, an MPEG decoder is described with relation to the prior art Figure 1b embodiment. ’194 Patent at 2:35-36. Further, decoder 80 may be found in Figures 2, 3 and 4. The discussion of applicability of MPEG and intrapicture/interpicture decoding and encoding is made generally with regard to decoder/encoder 80 and is not limited to Figure 4. *Id*. at 8:59-9:52.

Finally, the description of “directly supplied” images is discussed in the Summary of the Invention without limit to Figure 4. *Id*. at 5:31-41. In context of the overall specification, the understanding of directly supplying certain frames would be understood to be applicable to Figure 3. *Id*. at 5:31-41, 10:22-56. Defendants’ construction would exclude Figure 3. “A claim interpretation that excludes a preferred embodiment from the scope of the claim ‘is rarely, if ever, correct.’” *On-Line Techs., Inc. v. Bodenseewerk Perkin-Elmer GmbH*, 386 F.3d 1133, 1138 (Fed. Cir. 2004) (citation omitted).

The Court construes “directly supplied” to mean “supplied without being stored in main memory for purposes of decoding subsequent images” and “directly supplies” to mean “supplies without being stored in main memory for purposes of decoding subsequent images.” [6]

[6] With regard to claims that do not recite “main memory,” the term “main memory” is replaced to conform to the usage in each particular claim. Thus, “main memory” is replaced with “the memory” for ’194 Patent claim 15, ’368 Patent claim 21 and ’045 Patent claim 13. “Main memory” is replaced with “system memory” for ’368 Patent claim 14 and ’045 Patent claim 6.

6. "control circuit" ('464 Patent claim 1, 2, 7-13, 16-24, 32)

PUMA's Construction	Defendants' Construction
No construction necessary.	"an electronic control device that is separate from the CPU or processor and that interacts with the operating system"

The primary issue raised in the briefing is whether the "control circuit" must be separate from the processor/device. At the oral hearing, Defendants asserted that a key issue is whether the control circuit is a hardware device, as opposed to software.

Positions of the Parties

PUMA asserts that the term is effectively defined by the surrounding claim language. PUMA points to '464 Patent claim 1, which specifies that the "control circuit" is coupled to the decoding circuit, the processor, and the main memory. Further, PUMA notes that the claim states that the "control circuit" is configured to "request continuous use of several portions of the main memory from the operating system" and "translate the noncontiguous addresses to contiguous addresses of a block memory." '464 Patent claim 1.

PUMA objects to Defendants' construction for multiple reasons. First, PUMA asserts that Defendants' insertion of "device" in place of "circuit" provides no additional meaningful guidance. (Dkt. No. 120 at 26). Second, PUMA objects to Defendants' requirement that the "control circuit" be "separate." PUMA asserts that the specification does not define what "separate" means. PUMA also asserts that Defendants require the control circuit to be "separate" from "the CPU" but the term "CPU" is not used in the claims that include "control circuit." PUMA asserts that the addition of "CPU" would cause more confusion. (Dkt. No. 120 at 26-27). Third, PUMA asserts that Defendants' "separate" requirement conflicts with the specification. PUMA asserts that the '464 Patent explicitly contemplates that multiple components "can be

monolithically integrated as a single chip." '464 Patent 5:10-13. PUMA asserts that the claim requires only that the "control circuit" to be "coupled" to the processor. That can be the case even if the components are monolithically integrated as a single chip.

Defendants assert that the dispute reduces to whether the "control circuit:" (1) is an electronic device, (2) is separate from the CPU/processor and (3) interacts with the operating system. Defendants assert that support for their construction is found in this passage:

> Broadly stated, the present invention embodies a control circuit for use in a computer system. The computer system is controlled by an operating system and has a main memory. An electronic device is coupled to the processor and the main memory and is configured to request continuous use of several portions of the main memory from the operating system.

'464 Patent 3:37-43. Defendants assert that the figures also support their construction. Defendants point to '464 Patent Figures 1 and 2:

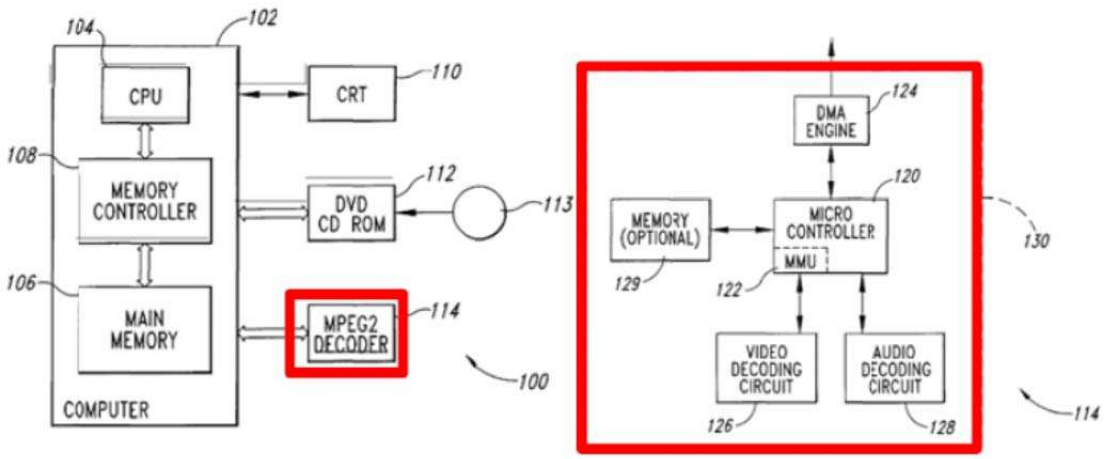


Fig. 1 *Fig. 2*

'464 Patent Figures 1 and 2 (color coding added). Defendants assert that the microcontroller 120, inside the MPEG decoder 114, performs the tasks of the claimed "control circuit." (Dkt. No. 121 at 27 (citing '464 Patent 6:63-7:50)). Defendants assert that the figures confirm that the MPEG decoder 114 is not part of the CPU and is a separate device coupled to the computer 102. Defendants assert that the specification repeatedly identified this divided architecture in the

context of being "the present invention." Defendants point to the passages: "[t]he present invention relates to the field of electronic systems requiring blocks of memory" ('464 Patent 1:19-20), "the present invention shares the main memory 108 with the computer 102" ('464 Patent 6:60-62) and "[t]he present invention interacts with the Windows 95 operating system 152 to act like a software application" but "actually employs hardware" that "is not a CPU, or other processor, or Intel-based microprocessor" ('464 Patent 9:14-21). (Dkt. No. 212 at 27-29).

Defendants further assert that during prosecution, the Applicants amended independent claim 25 to include the "control circuit." Defendants assert that when adding "control circuit," the Applicants argued that "[the prior art] does not teach the administration of a memory management method through a separate control circuit…." (Dkt. No. 121 at 28 (quoting Dkt. No. 121 Ex. 16 at 0509)).

As to the term "device," Defendants assert that the term is used at '464 Patent 3:40-43 to describe "control circuit." Defendants assert that their construction, unquestionably, grounds the "control circuit" in the realm of the physical, not mere software. (Dkt. No. 121 at 28). At the oral hearing, Defendants asserted that they would accept the plain meaning if it was clear that the circuit was hardware. (Dkt. No. 137 at 80-81).

As to the term "separate," Defendants assert that the Applicants used this term to distinguish the prior art. Defendants assert that the fact that the patent does not provide a special definition for "separate" reinforces the fact that the jury should be well-equipped to understand the word based on common parlance. (Dkt. No. 121 at 29).

Defendants assert that the surrounding claim language conforms to their construction. Specifically, Defendants assert the claim language requires the "control circuit" to be "coupled" to the "processor" and "configured to request…from the operating system." (*Id.*). Defendants

assert that there should, thus, not be a dispute. Defendants assert that the fact that PUMA disputes Defendants' construction indicates that PUMA intends to have PUMA's expert assert that hardware "coupled" to the processor can itself be part of the processor. (*Id.*). Defendants assert that the Court should resolve this issue now, rather than allowing the dispute to be argued to the jury.

Analysis

The '464 Patent specification provides an example with regard to Figures 1 and 2 in which various components are shown as separate components. The specification does not, however, emphasize the importance of such separation. The passage at '464 Patent 9:14-21, cited by Defendants, merely emphasizes that the circuitry in question acts "like a software application" but "actually employs hardware." Further, the passage states that the decoder may be a simple hardware circuit. The passage does not emphasize that such circuitry must be physically separate from the processor or cannot be integrated on a common device that has both a processor and a decoder. '464 Patent 9:14-29. This conforms to the claim term itself which merely states "circuit." The remaining claim language provides guidance as to what the circuit is coupled to and what the circuit does. It does not specify whether the "control circuit" must be separate. Defendants have pointed to no more than a preferred embodiment. *See Arlington Indus., Inc. v. Bridgeport Fittings, Inc.*, 632 F.3d 1246, 1254 (Fed. Cir. 2011) ("[E]ven where a patent describes only a single embodiment claims will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using words of expressions of manifest exclusion or restriction" (citation omitted)).

As to the prosecution history arguments cited by Defendants, Defendants are correct that there is one reference to "separate." But there is no argument that "separate" requires the

circuitry to be a stand-alone device as opposed to a separate portion of one device. Moreover, when reviewing the argument as a whole, there is no argument that patentability is based on separateness. (Dkt. No. 121 Ex. 16 at 0507-09). In context, the prosecution history does not stand for Defendants' proposition that the control circuit must be a separate device.

The use of "circuit" makes clear that hardware is being recited and the parties do not appear to disagree that a control circuit includes hardware. (Dkt. No. 137 at 80-82). Thus, there is no dispute that ordinary meaning includes hardware. An ordinary meaning does not, however, mean that the circuit cannot have associated software.

The Court finds that "control circuit" needs no further construction.

7. "algorithmically translate the noncontiguous addresses to the contiguous addresses" ('464 Patent claims 7, 22)

PUMA's Construction	Defendants' Construction
"convert the noncontiguous addresses to the contiguous addresses according to at least one mathematical operation"	"convert the noncontiguous addresses to the contiguous addresses according to mathematical operations performed on the noncontiguous addresses"

The primary dispute relates to whether multiple operations are required and whether the operations have to be performed on the addresses themselves.

Positions of the Parties

PUMA asserts that its construction is consistent with the specification. PUMA asserts that the specification states "the memory management unit 122 algorithmically maps a contiguous address to a noncontiguous address in the main memory 106." '464 Patent 8:20-23. PUMA further quotes the passage:

> For example, if two 1 megabyte blocks of the main memory 106 were provided under step 204, the memory management unit 122 can simply perform simple mathematical operations such as addition to add the offset addresses of such 1

> megabyte blocks of memory to addresses in the 2 megabyte block of contiguous memory.

'464 Patent 8:23-28. PUMA asserts that Defendants' construction requires a plurality of "operations" and would, thus, exclude embodiments that use a single mathematical operation to translate addresses. (Dkt. No. 120 at 27).

PUMA further asserts that nothing in the claims, specification, or prosecution history requires the mathematical operations to be "performed on the noncontiguous addresses." (*Id*. at 28). PUMA objects that Defendants' construction would improperly restrict the claims to requiring the mathematical operation to be performed directly on the noncontiguous addresses. (Dkt. No. 122 at 10). PUMA asserts that the patent teaches that addresses may be translated by performing mathematical operations on "page descriptors." (*Id*.). PUMA asserts that the page descriptors are essentially shorthand that corresponds to a group of addresses. PUMA cites to the passage: "page descriptors typically include an offset address and a page size that correspond to a starting address of a block of contiguous pages and the number of pages in the block." '464 Patent 7:51-54. PUMA also points out that mapping may be accomplished by mapping the page descriptors:

> the memory management unit 122 can be programmed to rapidly perform such memory mapping of the **noncontiguous page descriptors** to the contiguous string of 2-megabyte addresses. Under such an alternative, the memory management unit 122 **algorithmically maps a contiguous address to a noncontiguous address** in the main memory 106.

'464 Patent 8:17-23 (emphasis added). PUMA asserts that Defendants' limitation, thus, improperly limits the term to operations performed on the addresses because the specification describes that the operations can be performed on the page descriptors. (*Id*.).

Defendants assert that they agree that one mathematical operation can translate an address. Defendants assert, however, that there are multiple "addresses" being translated and,

thus, simple English parallelism requires plural "mathematical operations," *i.e.*, at least one per address. (Dkt. No. 121 at 29-30). Defendants assert that the claim language states that the noncontiguous addresses are being translated. Defendants assert that, as a necessity, the mathematical operations must be performed on the noncontiguous addresses. Defendants note that this is the case with the example that PUMA cites to from the specification. Defendants assert that any operation that "translates" a first address to a second address will by definition operate on the first address. (*Id*. at 30). At the oral hearing, Defendants emphasized that they just want to make clear that an operation is performed on each address. (Dkt. No. 137 at 83-84). Defendants assert that translating a page descriptor is not translating an address. (Id. at 84-85).

Analysis

PUMA presents the stronger arguments. Though Defendants argue "English parallelism" requires multiple operations, Defendants' construction opens the door to confusion as to whether multiple operations must be performed on each address. As the parties agree that a single operation on an address should be encompassed, PUMA's construction would be more beneficial to the jury.

Furthermore, the specification indicates that page descriptors may be used in the translating process. '464 Patent 8:17-23. Specifically, the specification describes a lookup table approach but describes an alternative algorithmic approach:

> instead, the memory management unit 122 can be programmed to rapidly perform such memory mapping of the **noncontiguous page descriptors** to the contiguous string of 2-megabyte addresses. Under such an alternative, the memory management unit 122 **algorithmically maps a contiguous address to a noncontiguous address** in the main memory 106.

'464 Patent 8:17-23 (emphasis added). Thus, as disclosed, the mathematical operations need not be performed on the addresses themselves. Rather, the addresses may be translated by

performing the operations on the associated page descriptors. *Id*. As explicitly stated, such operations translate the addresses. Defendants' construction would exclude a disclosed embodiment. "A claim interpretation that excludes a preferred embodiment from the scope of the claim 'is rarely, if ever, correct.'" *Globetrotter Software, Inc. v. Elam Computer Group Inc.*, 362 F.3d 1367, 1381 (Fed. Cir. 2004) (quoting *Vitronics Corp.*, 90 F.3d at 1583).

The Court construes "algorithmically translate the noncontiguous addresses to the contiguous addresses" to mean "convert the noncontiguous addresses to the contiguous addresses according to at least one mathematical operation"

CONCLUSION

The Court adopts the constructions of the disputed terms as set forth in this opinion. It is **ORDERED** that in the presence of the jury the parties may not refer, directly or indirectly, to the other parties' claim construction positions and may not mention any portion of this opinion other than to recite the actual definitions adopted by the Court.

SIGNED this 30th day of July, 2015.

ROY S. PAYNE
UNITED STATES MAGISTRATE JUDGE