UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

PARTHENON UNIFIED MEMORY ARCHITECTURE LLC, Plaintiff, v. SAMSUNG ELECTRONICS CO., LTD ET AL.,	§ § § § § § § §	Case No. 2:14-cv-0902-JRG-RSP (Lead)
v. HUAWEI TECHNOLOGIES CO., LTD., ET AL.,	§ § § §	Case No. 2:14-cv-0687-JRG-RSP (Consolidated)
v. MOTOROLA MOBILITY LLC, Defendants.	§ § § § §	Case No. 2:14-cv-0689-JRG-RSP (Consolidated)

MEMORANDUM OPINION AND ORDER

On August 31, 2015 the Court held a hearing to determine the proper construction of the disputed terms in nine Asserted Patents. The Court, having considered the parties' claim construction briefing (Dkt. Nos. 78, 86, 88) and their arguments at the hearing, issues this Memorandum Opinion and Order construing the disputed terms.

BACKGROUND AND THE ASSERTED PATENTS

Parthenon Unified Memory Architecture LLC ("PUMA") brings three actions: one against Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc., a second against Huawei Technologies Co., LTD., Huawei Technologies USD, Inc. and Huawei Device USA,

Inc., and a third against Motorola Mobility LLC (all defendant parties collectively, "Defendants"). The actions allege that Defendants infringe U.S. Patent Nos. 5,812,789 ("the '789 Patent"), 6,058,459 ("the '459 Patent"), 6,427,194 ("the '194 Patent"), 7,321,368 ("the '368 Patent"), 7,542,045 ("the '045 Patent"), 7,777,753 ("the '753 Patent"), 8,054,315 ("the '315 Patent"), 8,681,164 ("the '164 Patent") and 5,960,464 ("the '464 Patent") (collectively, "the Asserted Patents").

The '789 Patent and the '459 Patent were filed on the same day, have similar specifications, and incorporate each other by reference. Six patents are based on continuation applications of the '459 Patent: the '194 Patent, the '368 Patent, the '045 Patent, the '753 Patent, the '315 Patent, and the '164 Patent.[1] All nine Asserted Patents were subject to a claim construction order issued by this Court in *Parthenon Unified Memory Architecture, LLC v. HTC Corp. et al.*, Civil Action No. 2:14-cv-0690-JRG-RSP, Dkt. No. 155 (ED. Tex. July 30, 2015) ("the *Parthenon I* Order"). Furthermore, one additional prior Eastern District of Texas claim construction order involved the '789 Patent. *STMicroelectronics, Inc. v. Motorola, Inc.*, 327 F. Supp. 2d 687 (E.D. Tex. 2004).

In general, the '789 Patent, the '459 Patent, the '194 Patent, the '368 Patent, the '045 Patent, the '753 Patent, the '315 Patent, and the '164 Patent relate to systems in which a first device (for example a processor) and a decoder/encoder share a common memory. The '459 Patent abstract recites:

> An electronic system provides direct access between a first device and a decoder/encoder and a memory. The electronic system can be included in a computer in which case the memory is a main memory. Direct access is accomplished through one or more memory interfaces. Direct access is also accomplished in some embodiments by direct coupling of the memory to a bus, and in other embodiments, by direct coupling of the first device and

[1] The specification of the '464 Patent is not shared by the other Asserted Patents.

> decoder/encoder to a bus. The electronic system includes an arbiter for determining access for the first device and/or the decoder/encoder to the memory for each access request. The arbiter may be monolithically integrated into a memory interface of the decoder/encoder or the first device. The decoder may be a video decoder configured to decode a bit stream formatted to comply with the MPEG-2 standard. The memory may store predicted images which are obtained from a single preceding image and may also store intra images. Bidirectional images which are directly supplied to a display adapter may be obtained from two preceding intra or predicted images.

’459 Patent Abstract.

The ’464 Patent relates, generally, to a system whereby a decoder, which requires contiguous blocks of memory, can utilize noncontiguous blocks of the system’s memory. The ’464 patent abstract recites:

> A method and apparatus employing a memory management system that can be used with applications requiring a large contiguous block of memory, such as video decompression techniques (e.g., MPEG 2 decoding). The system operates with a computer and the computer's operating system to request and employ approximately 500 4-kilobyte pages in two or more noncontiguous blocks of the main memory to construct a contiguous 2-megabyte block of memory. The system can employ, on a single chip, a direct memory access engine, a microcontroller, a small block of optional memory, and a video decoder circuit. The microcontroller retains the blocks of multiple pages of the main memory, and the page descriptors of these blocks, so as to lock down these blocks of memory and prohibit the operating system or other applications from using them. The microcontroller requests the page descriptors for each of the blocks, and programs a lookup table or memory mapping system in the on-chip memory to form a contiguous block of memory. As a result, the video decoder circuit can perform operations on a 2-megabyte contiguous block of memory, where the microcontroller employs the lookup table to translate each 2-megabyte contiguous address requested by the video decoder circuit to its appropriate page in the main memory. As soon as the video decoding operations are complete, the microcontroller releases the blocks of multiple pages of memory back for use by the computer.

’464 Patent Abstract.

APPLICABLE LAW

1. Claim Construction

"It is a 'bedrock principle' of patent law that 'the claims of a patent define the invention to which the patentee is entitled the right to exclude.'" *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (quoting *Innova/Pure Water Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)). To determine the meaning of the claims, courts start by considering the intrinsic evidence. *Id.* at 1313; *C.R. Bard, Inc. v. U.S. Surgical Corp.*, 388 F.3d 858, 861 (Fed. Cir. 2004); *Bell Atl. Network Servs., Inc. v. Covad Commc'ns Group, Inc.*, 262 F.3d 1258, 1267 (Fed. Cir. 2001). The intrinsic evidence includes the claims themselves, the specification, and the prosecution history. *Phillips*, 415 F.3d at 1314; *C.R. Bard, Inc.*, 388 F.3d at 861. Courts give claim terms their ordinary and accustomed meanings as understood by one of ordinary skill in the art at the time of the invention in the context of the entire patent. *Phillips*, 415 F.3d at 1312–13; *Alloc, Inc. v. Int'l Trade Comm'n*, 342 F.3d 1361, 1368 (Fed. Cir. 2003).

The claims themselves provide substantial guidance in determining the meaning of particular claim terms. *Phillips*, 415 F.3d at 1314. First, a term's context in the asserted claim can be very instructive. *Id*. Other asserted or unasserted claims can also aid in determining the claim's meaning, because claim terms are typically used consistently throughout the patent. *Id*. Differences among the claim terms can also assist in understanding a term's meaning. *Id*. For example, when a dependent claim adds a limitation to an independent claim, it is presumed that the independent claim does not include the limitation. *Id*. at 1314–15.

"[C]laims 'must be read in view of the specification, of which they are a part.'" *Id*. (quoting *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995) (en banc)). "[T]he specification 'is always highly relevant to the claim construction analysis. Usually, it is

dispositive; it is the single best guide to the meaning of a disputed term.'" *Id*. (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)); *Teleflex, Inc. v. Ficosa N. Am. Corp.*, 299 F.3d 1313, 1325 (Fed. Cir. 2002). This is true because a patentee may define his own terms, give a claim term a different meaning than the term would otherwise possess, or disclaim or disavow the claim scope. *Phillips*, 415 F.3d at 1316. In these situations, the inventor's lexicography governs. *Id*. The specification may also resolve ambiguous claim terms "where the ordinary and accustomed meaning of the words used in the claims lack sufficient clarity to permit the scope of the claim to be ascertained from the words alone." *Teleflex, Inc.*, 299 F.3d at 1325. But, "'[a]lthough the specification may aid the court in interpreting the meaning of disputed claim language, particular embodiments and examples appearing in the specification will not generally be read into the claims.'" *Comark Commc'ns, Inc. v. Harris Corp.*, 156 F.3d 1182, 1187 (Fed. Cir. 1998) (quoting *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1560, 1571 (Fed. Cir. 1988)); *see also Phillips*, 415 F.3d at 1323. The prosecution history is another tool to supply the proper context for claim construction because a patent applicant may also define a term in prosecuting the patent. *Home Diagnostics, Inc., v. Lifescan, Inc.*, 381 F.3d 1352, 1356 (Fed. Cir. 2004) ("As in the case of the specification, a patent applicant may define a term in prosecuting a patent.").

Although extrinsic evidence can be useful, it is "'less significant than the intrinsic record in determining the legally operative meaning of claim language.'" *Phillips*, 415 F.3d at 1317 (quoting *C.R. Bard, Inc.*, 388 F.3d at 862). Technical dictionaries and treatises may help a court understand the underlying technology and the manner in which one skilled in the art might use claim terms, but technical dictionaries and treatises may provide definitions that are too broad or may not be indicative of how the term is used in the patent. *Id*. at 1318. Similarly, expert

testimony may aid a court in understanding the underlying technology and determining the particular meaning of a term in the pertinent field, but an expert's conclusory, unsupported assertions as to a term's definition are entirely unhelpful to a court. *Id*. Generally, extrinsic evidence is "less reliable than the patent and its prosecution history in determining how to read claim terms." *Id*.

2. Claim Indefiniteness

Patent claims must particularly point out and distinctly claim the subject matter regarded as the invention. 35 U.S.C. § 112, ¶ 2. "[I]ndefiniteness is a question of law and in effect part of claim construction." *ePlus, Inc. v. Lawson Software, Inc.*, 700 F.3d 509, 517 (Fed. Cir. 2012). A party challenging the definiteness of a claim must show it is invalid by clear and convincing evidence. *Young v. Lumenis, Inc.*, 492 F.3d 1336, 1345 (Fed. Cir. 2007).

The definiteness standard of 35 U.S.C. § 112, ¶ 2 requires that:

> [A] patent's claims, viewed in light of the specification and prosecution history, inform those skilled in the art about the scope of the invention with reasonable certainty. The definiteness requirement, so understood, mandates clarity, while recognizing that absolute precision is unattainable. The standard we adopt accords with opinions of this Court stating that "the certainty which the law requires in patents is not greater than is reasonable, having regard to their subject-matter.

Nautilus, Inc. v. Biosig Instruments, Inc., 134 S. Ct. 2120, 2129–30 (2014) (internal citations omitted).

3. Construing Claim Terms that Have Previously Been Construed by This Court or Other Courts

The Court has construed several of the disputed terms in *Parthenon I*. Additionally, in *STMicroelectronics* the Court construed the '789 Patent. These constructions do not control but are instructive and will, at times, provide part of the basis for the Court's analysis. *See Burns, Morris & Stewart Ltd. P'ship v. Masonite Int'l Corp.*, 401 F. Supp. 2d 692, 697 (E.D. Tex. 2005)

(while a previous construction may be instructive and provide the basis of the analysis, the previous construction is not binding on the court, particularly when there are new parties and those parties have presented new arguments).

AGREED TERMS

The parties agreed to the following constructions in their joint claim construction chart:

Term	Agreed Construction
"simultaneously accesses the bus"	"accesses the bus at the same time"
"translate"	"convert"
"algorithmically translate"	"convert using at least one mathematical operation"
"display device"	"screen and its circuitry
"display adapter"	"an adaptor that processes images for a display device"

Dkt. No. 90-2 at 6-7. The parties have agreed that the following terms require no construction: "direct memory access (DMA) engine" "direct memory access engine" and "refresh logic." (Dkt. No. 78 at 24); (Dkt. No. 86 at 2).

DISPUTED TERMS

1. **"bus" ('789 Patent claims 1, 13, 15, 28; '459 Patent claims 1, 2, 7, 11, 13; '194 Patent claims 1, 2, 9, 11, 16-18, 23; '368 Patent claims 1, 5, 7, 13, 19, 20, 23; '045 Patent claims 1, 4, 5, 12, 15; '753 Patent claims 1, 7; '315 Patent claim 1 and '164 Patent claims 1, 6, 7)**

PUMA's Construction	Defendants' Construction
No construction necessary. Alternatively: "a signal line or a set of associated signal lines to which a number of devices are coupled and over which information may be transferred between them"	"a signal line or set of associated signal lines to which a number of devices are directly connected and over which information may be transferred by only one device at a time"

The parties' dispute whether devices must be "directly" connected to a bus and whether a bus may only transfer information one device at a time.

Positions of the Parties

PUMA asserts that the term "bus" is known in the art and does not need construction. Its alternative construction comes from *STMicroelectronics*. In *STMicroelectronics*, the parties agreed to "a signal or set of signal lines to which a number of devices are coupled and over which information may be transferred between them." *STMicroelectronics*, 327 F. Supp. 2d at 711. PUMA asserts that its construction is consistent with an IEEE extrinsic evidence dictionary. (Dkt. No. 78 at 6). PUMA further asserts that in a prior art patent, Defendants' own expert, Dr. Stone, defined "bus" as "a series of electrical lines interconnecting the modules in the computer." (Dkt. No. 78 at 8 (quoting Dkt. No. 78 Ex. L (U.S. Patent No. 5,093,890) at 1:19-21)).

PUMA contends that the use of intervening components, such as a switch, still renders a device a "bus." PUMA cites to the prior art SPARC memory bus, the MBus, and similar buses that feature switches, tri-state buffers, and multiplexers. (Dkt. No. 78 at 8 (citing Ex. P)). PUMA notes that Defendants' expert, Dr. Stone, characterized the MBus tri-state buffer as a switch that disconnects drivers from the bus. (*Id*.).

Defendants assert that the Court's preliminary construction in *Parthenon I* is incomplete because it does not give guidance as to where one bus ends and another bus begins. (Dkt. No. 86 at 3). Defendants contend that this is important because some claims specifically require no more than one bus. (*Id*. (citing '459 Patent claim 1 and '194 Patent claim 1)). Defendants assert that applying the Court's preliminary construction to a complex circuit, one of ordinary skill may improperly conclude that the entire circuit is one bus. Defendants assert that the phrases "by only one device at a time" and "directly" address this issue. Defendants assert that these limitations

are supported by both the intrinsic evidence and the understanding of one skilled in the art in 1996. (*Id.*).

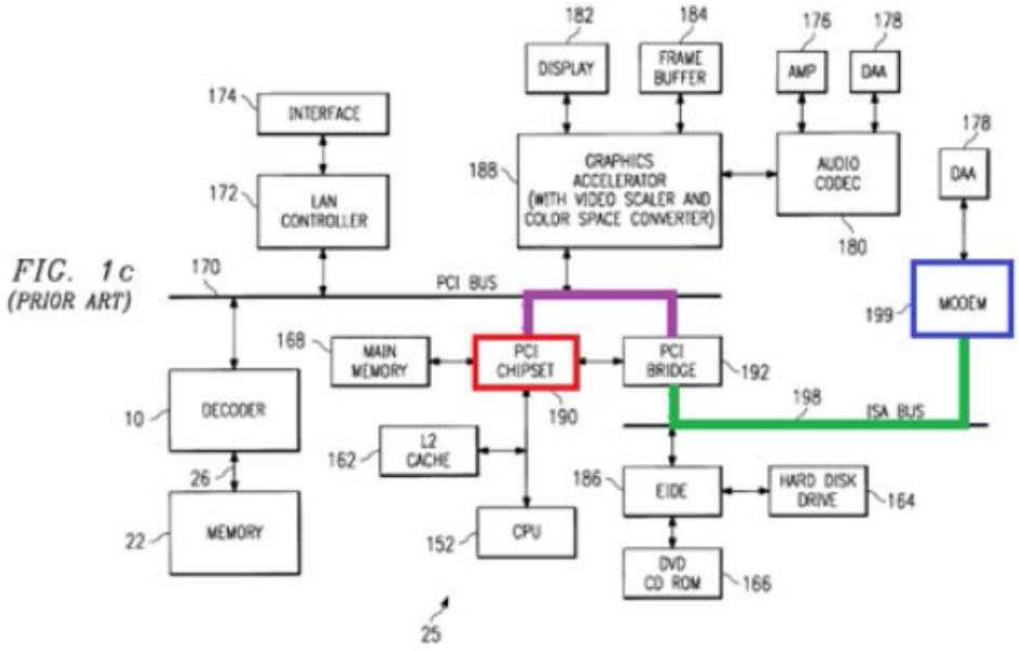
As to the phrase "one device at a time," Defendants contend that a fundamental characteristic of a bus is that only one device may transfer information at a time. (*Id.* at 4 (citing Stone Declaration)). Defendants assert that to prevent contentions on the bus lines, there must be a mechanism to ensure that only one device is allowed to transfer information at a time. (*Id.*). Defendants cite column 12 line 49 to column 13 line 36 of the '459 Patent as support for including the phrase "one device" at a time. (*Id.*) At the oral hearing, Defendants also cited to a specification table, which disclosed the arbiter functions and states. '459 Patent 13:15-27. Defendants state that the arbiter states teach that only one device can gain access to the bus at a time.

Defendants contend that PUMA has mischaracterized prior art buses such as the MBus. Defendants state that PUMA states the MBus includes intervening components such as tri-state buffers and multiplexers. (*Id.* at 7). Defendants assert, however, that these components are not part of the bus, but rather, part of the bus interface circuitry that resides within the devices connected to the bus. (*Id.* (citing Stone Deposition)). Defendants contend that it is important to distinguish a bus from the bus interface circuitry within each device.

Defendants claim that this distinction is important because some claims require that devices be coupled to other devices through an interface. Defendants point to the '045 Patent claim 4: "a video decoder configured to be coupled to the main memory via a first bus interface" and "a central processing circuit configured to be coupled to the main memory via a second bus interface." (*Id.* at 8). Defendants assert that the specification teaches a distinction between a bus and bus interface circuitry. (*Id.* (quoting "FIFO 30 is supplied with compressed data from bus 10

via an interface circuit PCI I/F 39" ('459 Patent 11:59-60, Figure 6) and "bus interface 210 for any system busses 170 to which it is coupled" ('459 Patent 12:17-18, Figure 7))).

As to construing "coupled" using the phrase "directly connected," Defendants assert that another construction of "coupled" makes it impossible to differentiate between one bus and two buses. (*Id*. at 4-5). Defendants assert that PUMA's construction would render all devices in the circuit "directly or indirectly" coupled to one another. (*Id*. at 5). Defendants cite to PUMA's color-coded illustration of '789 Patent Figure 1c as illustrative.



(*Id*. at 6).

Defendants assert that PUMA says that the modem 199 is coupled to the core logic chipset 190 through a bus 170. (*Id*.). However, Defendants note that to couple those two devices, the communication must pass through two buses, the ISA bus 198 and PCI bus 170. Defendants assert that PUMA's use of "coupled" would allow the PCI and ISA buses to be viewed as one bus. (*Id*.). Defendants assert that this conflicts with the specification and would not be feasible because the PCI and ISA buses operate under different specifications. (*Id*.). Defendants assert

that the modem 199 is configured to communicate over the ISA bus 198, but the modem 199 cannot communicate over the PCI bus 170 without first going through a separate element – the PCI bridge 192.

Defendants assert that, similarly, the PCI chipset is "directly connected" to the PCI bus 170. Defendants state that the decoder 10 is configured to communicate over the PCI bus 170. But, in order for the decoder 10 to communicate with the modem 199, the decoder needs to match the ISA protocol, which is the function of the PCI bridge 192. (*Id*. at 7). Defendants assert that only devices that are "directly connected" to a bus may readily transfer information and communicate on that bus. Finally, at the oral hearing, Defendants cited *Ethicon* as an example of a case where the Federal Circuit rejected a meaning for "connected" that included indirect and direct connections. *Ethicon Endo-Surgery, Inc. v. U.S. Surgical Corp.*, 93 F.3d 1572, 1578 (Fed. Cir. 1996).

In reply, PUMA argues that the passage that Defendants have cited in support of using the phrase "one device at a time" does not show that the phrase should be included in the Court's construction. PUMA asserts that the passage does not state a bus can only transfer information one device at a time, but merely describes an arbiter of one of the preferred embodiments. (Dkt. No. 88 at 2).

PUMA asserts that Defendants are rewording the "controlled by an arbiter" language that Defendants included in their original construction. PUMA asserts that the "one device" language is improper for the same reasons. PUMA contends that not every claim requires an "arbiter" and for the claims that do, the operation of the arbiter stands separate, apart and distinct from the term "bus." (*Id*.). PUMA asserts that Defendants' construction would read out any bus that is not implemented with an arbiter. For example, PUMA asserts that though claim 15 of the '789

Patent recites a "bus," an arbiter limitation is only added in dependent claim 19. (Dkt. No. 78 at 7).

PUMA further asserts that Defendants' construction reads out common bus technologies like split-transaction buses and other bus technologies that can transfer information between multiple devices at the same time. (Dkt. No. 88 at 2). PUMA asserts that prior art U.S. Patent 4,785,394 (issued Nov. 15, 1988) describes multiple devices that use a bus at the same time. The prior art patent states: "During the time period which elapses between the read address signal and the response from the memory, other processors in the computer system are communicating other signals to other components of the system over the bus." (Dkt. No. 88 Ex. A, U.S. Patent 4,785,394 1:58-62).

PUMA also argues that adding the phrase "directly connected" to the Court's construction would read out buses that use tri-state buffers, other intervening components, or switches that disconnect various devices from the bus. PUMA contends that Defendants' construction would restrict the claim to the most primitive form of a bus and should be rejected. (*Id*. at 2-3).

PUMA contends that Defendants manufactured an argument as to the ISA bus and PCI bus of Figure 1c of the '789 Patent being considered one bus under PUMA's construction. PUMA asserts that it has never taken such a position. (*Id*. at 3). PUMA asserts that the Court's proposed insertion of "associated" addresses Defendants' concern. PUMA asserts that a person of skill in the art would not view the signal lines of the PCI bus and the ISA to be a "set of associated signal lines." (*Id*.).

At the oral hearing, with regard to the "one device at a time" limitation, much of the discussion by both parties focused upon the content of extrinsic evidence prior art buses.

Defendants argued that the extrinsic evidence U.S. Patent No. 4,785,394, cited by PUMA, states that even in split transaction buses, "[t]he arbitration technique determines which one of the particular components of the system has exclusive access to the bus at any particular time." (Dkt. No. 88 Ex. A, U.S. Patent 4,785,394 1:66-2:1). As to the MBus, Defendants cited to a passage that indicated that for any given signal, the signal is driven in the same cycle by only one source. Both parties also discussed four exhibits (Exhibits A-D) filed by PUMA after Defendants changed their construction in the briefing to include the "one device at a time" limitation. (Dkt. No. 104, Ex. A-D). Defendants assert that the additional disclosures relate not to buses but rather to crossbar switches and switch fabrics. Defendants assert that such structures are network topologies, different from the linear topology of the buses disclosed in the Asserted Patents. Defendants contend that the patentees could have claimed these network topologies but did not. PUMA, in response, cited to Ex. A section 2.2 which described what Defendants characterized as "network topologies" (including the Mercury RACEway) to be a "bus." (Dkt. No. 104, Ex. A at 203). PUMA also cited to Ex. C which described the RACEway crossbar topology to be a "bus." (Dkt. No. 104, Ex. C at 31).

Analysis

Defendants seek with the "one device at a time" limitation, a negative limitation that excludes certain categories of devices. The use of a negative limitation in the construction of a claim generally requires support from the intrinsic evidence. *See Omega Eng'g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1322-23 (Fed. Cir. 2003) (declining to add a negative limitation when there was no "express disclaimer or independent lexicography in the written description that would justify adding that negative limitation"). As to the intrinsic evidence, Defendants only cite to an embodiment. Defendants do not cite to any disclaimer or disavowal. Even if only a single

embodiment exists, the preferred embodiment is not inherently required to be read into the claims. *See Arlington Indus., Inc. v. Bridgeport Fittings, Inc.*, 632 F.3d 1246, 1254 (Fed. Cir. 2011) ("Even where a patent describes only a single embodiment, claims will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using words or expressions of manifest exclusion or restriction.") (internal citations omitted).

Moreover, Defendants' construction, in essence, reads the arbiter concept into the "bus" term. However, as described in the patents, the arbiter is a separate structure that has a separate function. '459 Patent Figure 7, 12:49-13:36; '789 Patent Figure 2, 4:4-11, 9:42-57. The fact that the specification discloses a separate arbiter and arbitration function is indicative that such functionality is not inherent in the term "bus." As pointed out by PUMA, the claims also confirm that the arbiter function is not inherently part of the claimed bus. Some claims recite the arbiter and arbitration and some claims do not. *See*, *e.g.*, '789 Patent Claims 15 and 19. The intrinsic record does not teach that buses that allow multiple devices to access at the same time are excluded.

As to the extrinsic evidence, Defendants rely primarily on the declaration of Dr. Stone. But PUMA presents contradicting evidence, such as the MBus, U.S. Patent No. 4,785,394, and Dkt. No. 104 Exhibits A-C.[2] On balance, the extrinsic evidence does not require the Court to construe the "bus" term to include "only one device at a time." Rather, the evidence indicates that buses may include tri-state buses, split transaction buses, and "network topology" buses.[3] In

[2] There appears to be a debate between the parties as to the date of Exhibit D. This Order does not rely on Exhibit D.

[3]With regard to split transaction buses, the dispute shifts to what is meant by "one device at a time." U.S. Patent 4,785,394 teaches that an operation may be split so that for a given memory request a read address may be sent and during the time between the read address signal and the response from the memory, another device may utilize the bus. (Dkt. No. 88 Ex. A, U.S. Patent 4,785,394 1:58-62). Thus, during one device's read operation another device may utilize the bus

sum, the Court finds that the extrinsic evidence does not support the negative limitation sought by Defendants.

Furthermore, the Court does not accept Defendants' argument that the claim construction should include the word "directly." Whether a device is directly or indirectly connected to a bus does not change the nature and status of the bus. The examples in the '789 Patent are illustrative. For example, the '789 Patent describes the structure of Figure 2 as the decoder/encoder 45 being "coupled to the memory 50 through devices, typically a bus 70." '789 Patent 6:29-30. Figure 2 shows that the decoder 45 is indirectly coupled to the memory 50 through an intervening memory interface 48 and a bus 70. The meaning of the term "bus" and "bus 70" does not change just because the memory interface 48 separates the bus 70 and the decoder 45. Other figures are illustrative. Decoder 10 may be directly connected to PCI bus 170 such as in Figure 1c of the '789 Patent. Alternatively, the decoder/encoder 45 may be indirectly connected to the PCI bus 170 through a PCI bus interface 210 such as shown in Figure 4 of the '789 Patent. These variations do not impact whether the PCI bus 170 is a bus. Indeed, Defendants' proposed construction would exclude disclosed configurations such as '789 Patent Figure 2 where the decoder is indirectly connected to the bus. Constructions that exclude a disclosed embodiment are rarely correct. *On-Line Techs., Inc. v. Bodenseewerk Perkin-Elmer GmbH*, 386 F.3d 1133, 1138 (Fed. Cir. 2004).

Finally, Defendants' citation to *Ethicon* as support for including the word "directly" is not persuasive. First, the Court noted that *Ethicon* dealt with the narrower term "connected" not "coupled." *Ethicon*, 93 F.3d at 1578. Second, *Ethicon* states that the context of a term's usage in the intrinsic evidence is highly relevant to claim construction. *See id.* ("We acknowledge that the

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during the response time. Defendants' construction creates ambiguity as to whether such operations are "one device at a time" or two devices at a time.

term ‘connected to’ could, in other contexts, be broadly construed.”). Here, as discussed above, the specification teaches that devices may be coupled to the bus through indirect connections which include an intervening component.

Finally, the Court rejects Defendants’ argument that, under PUMA’s construction, one skilled in the art would consider the PCI bus and ISA bus (and in fact the entire circuit) to be one bus. First, the patents clearly state these structures are different buses. Second, as noted in *Parthenon I*, in prosecution, the Applicants distinguished the memory bus 108 and the PCI bus 120 of Lambrecht. Specifically, Applicants distinguished the Lambrecht buses as being two separate buses. As shown in the patents and the prosecution history, the “set of signal lines” is not just any lines chosen randomly to form “a set.” Rather, the “set” is a set of “associated” lines, for example the PCI bus lines, ISA bus lines, or memory bus lines, each being a separate set. The Court’s construction requires the set of signal lines to be “a set of associated signal lines.” This addresses the argument of Defendants.

The Court construes “bus” to mean “a signal line or a set of associated signal lines to which a number of devices are coupled and over which information may be transferred between them.”

2. “memory bus” (’164 Patent claims 1, 6, 7)

PUMA’s Construction	Defendants’ Construction
No construction necessary. Alternatively: “a signal line or a set of associated signal lines to which a number of devices, including a memory, are coupled and over which information may be transferred”	“bus [as construed] that connects directly with a memory”

The primary issue in dispute between the parties is whether a memory bus requires a direct connection.

Positions of the Parties

PUMA asserts that a person skilled in the art would understand that a memory bus is a bus that is coupled to a memory. (Dkt. No. 88 at 4). PUMA asserts that Defendants' use of "connects directly" would read out common buses that include intervening components or interfaces, such as the MBus. PUMA asserts that nothing in the specification suggests that the patentee intended to restrict the generic term "memory bus" in such a narrow fashion. (Dkt. No. 78 at 9).

Defendants contend that the specification shows memory buses that are connected directly to memory. (Dkt. No. 86 at 9 (citing '459 Patent at 8:13-14, Figure 2, 9:61-62, Figure 3, 12:23-32, Figure 7)). Defendants assert that PUMA's argument about the MBus is incorrect because a person skilled in the art would not consider the intervening components or interface to be part of the bus. (*Id*. at 9, n. 4). Defendants assert that PUMA's construction does not differ from PUMA's construction of "bus." Defendants assert that under PUMA's construction, a bus is a "memory bus" merely if data transmitted over a bus eventually reaches the memory. (*Id*. at 9). Defendants assert that the intrinsic record does not suggest that any bus in the data transmission path falls within the meaning of memory bus so long as the data eventually ends up at a memory. Rather, Defendants assert that the intrinsic record supports Defendants' narrower construction. (*Id*.).

The parties did not argue this term at the oral hearing.

Analysis

The dispute regarding "directly" connected raises the issues described in the Court's analysis of the term "bus." For the reasons described above, the Court finds that a "direct"

connection is not required. As to the wording the construction, the Court finds that Defendants' approach is more understandable to a jury.

The Court construes "memory bus" to mean "bus [as construed] that is coupled with memory."

3. "in real time" ('789 Patent claims 1, 13, 15, 28; '315 Patent claim 1 and '164 Patent claims 1, 6)

PUMA's Construction	Defendants' Construction
"fast enough to keep up with an input data stream"	Indefinite: Alternatively: "fast enough to keep up with the input data stream, wherein obtaining bus mastership does not consume bus cycles"

The fundamental dispute between the parties relates to the question of whether certain prosecution history statements limit determining "real time" by bus latency which is in conflict with the specification.

Positions of the Parties

PUMA notes that in *STMicroelectronics* the Court construed "real time" to mean "processing fast enough to keep up with an input data stream." *STMicroelectronics*, 327 F.Supp. 2d at 693, 710. PUMA asserts that construction comports with the intrinsic and extrinsic evidence. For example, PUMA points out that the patent specification states: "If the decoder does not operate in real time the decoded movie would stop periodically between images until the decoder can get access to the memory." '789 Patent 3:21-24. Elsewhere, the specification similarly states:

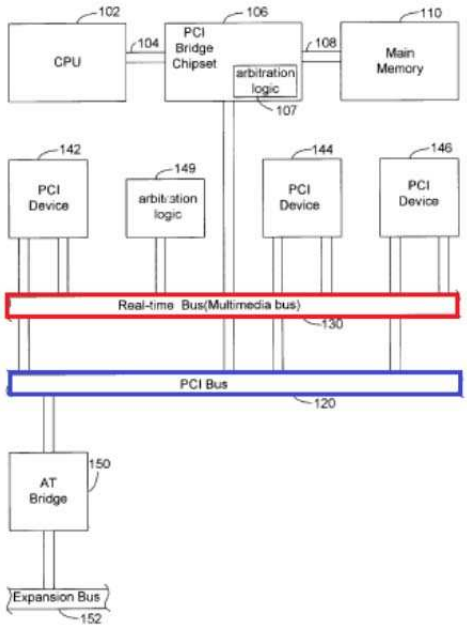
> A goal is to have the decoder/encoder 45 operate in real time without dropping so many frames that it becomes noticeable to the human viewer of the movie. To operate in real time the decoder/encoder 45 should decoder [sic] and/or encode images fast enough so that any delay in decoding and/or encoding cannot be

> detected by a human viewer. This means that the decoder/encoder 45 has a required bandwidth that allows the decoder/encoder 45 to operate fast enough to decode the entire image in the time between screen refreshes, which is typically 1/30 of a second, with the human viewer not being able to detect any delay in the decoding and/or encoding.

Id. at 6:41-52. PUMA also cites to an IEEE dictionary and statement in *STMicroelectronics* that "[t]he relevant dictionary definition indicates that real time concerns the processor's ability to 'keep up with' the data input." (Dkt. No. 78 at 10 (quoting *STMicroelectronics*, 327 F.Supp. 2d at 693)).

On the issue of indefiniteness, PUMA asserts that the specification informs a person of skill in the art with a "reasonable certainty" of the scope of the invention. First, PUMA notes that Defendants' own expert uses the term "real time" in a variety of his own publications. (Dkt. No. 78 at 11). Second, PUMA asserts that the Court should reject Defendants' argument for the reason that it rejected this argument in *Parthenon I*. PUMA asserts that Defendants misread the prosecution history. PUMA contends that in the prosecution history, PUMA did not distinguish Gulick on the basis of using a PCI bus, and did not distinguish Gulick by narrowing the ordinary meaning of "real time." Rather, PUMA argues that the Applicant distinguished Gulick on the basis that the PCI bus, as used in the context of Gulick, was insufficient for real time performance. (Dkt. No. 78 at 11-12 (citing Dkt. No. 78 Ex. J (Mangione-Smith Decl.) at ¶25-29)).

For example, PUMA emphasizes that Figure 1 of Gulick represents that the Gulick PCI bus was used in addition to a "real time" bus. PUMA asserts that Gulick represents that the PCI bus in Gulick was insufficient to guarantee real time performance for its purposes. (Dkt. No. 88 at 4). PUMA points to Gulick Figure 1:



(Dkt. No. 78 at 12 (color coding added)). PUMA notes that Gulick included a real time bus 130 in addition to the PCI bus 120. PUMA asserts that, thus, Gulick itself represented that the PCI bus, as used in Gulick, was insufficient to guarantee real time performance. PUMA contends that it was the Gulick reference which raised the concern of latency in context of the specific system of Gulick. PUMA asserts that the Applicants did not generally characterize the term "PCI bus" but rather characterized the specific use of that term in Gulick. (*Id*.). PUMA argues that the fact that Gulick represents that its PCI bus was not a real time bus has nothing to do with the parameters of PCI buses in general. Rather, PUMA asserts that Gulick shows that the specific context in which the PCI bus was used in Gulick establishes that the bus was not a real time bus. (*Id*.).

Defendants assert that the term "real time" is indefinite because the Applicants took inconsistent positions in the intrinsic record on whether a PCI bus is a real time bus. Defendants assert that these contradictions introduced ambiguity such that the term is not reasonably certain. (Dkt. No. 86 at 10).

Defendants assert that several performance requirements affect whether a bus can operate in real time, including bus bandwidth and bus latency. (*Id*. (citing Ex. E (Mangione-Smith Decl.) at ¶22; Ex. F (Mangione-Smith Depo) at 71:21-25, 91:4-15)). Defendants assert that the bus bandwidth refers to the amount of data that the bus can transfer at a given time. Defendants assert that bus latency refers to the delay for devices to get access to the bus. (*Id*.). Defendants assert that bandwidth is the factor on which the asserted patents rely. (*Id*.). Defendants assert that the patents do not emphasize latency, and the entire focus of the patents is on bandwidth. (*Id*. at 10-11). Defendants also assert that the patents confirm that a PCI has more than enough bandwidth for real-time operation. (*Id*. at 11-12 (citing '459 Patent 5:14-20; Ex. E (Mangione-Smith Decl.) at ¶27)).

Defendants assert that despite the patents clearly stating that a PCI bus is a real time bus due to sufficient bandwidth, the Applicants argued in prosecution that a prior art PCI bus was not "real time" because of its latency. (Dkt. No. 86 at 12). In particular, Defendants point to the prosecution statements regarding Gulick:

> *Gulick's* PCI devices must communicate with the main memory using PCI bus 120, which is <u>not</u> a real time bus. *Gulick* at 5:29-38. Instead, the PCI devices 142, 144, 146 must obtain bus mastership, which consumes PCI cycles. *Id.* The PCI devices in *Gulick's* FIG. 1 may communicate data between each other in real-time using the multimedia bus 130, but this is different from claim 1, which calls out a memory bus configured to pass data in real time between a shared main memory and a decoder/encoder.

(Dkt. No. 86 Ex L at 02591) (emphasis in original). Defendants contend that the reference to "consumes PCI cycles" is a direct reference to latency but not bandwidth. (*Id*. at 12). Defendants also point to the next paragraph which states: "[in Gulick] the PCI devices must still obtain non-real-time bus mastership in order to receive data from main memory 110." (*Id*.). Defendants assert that the Applicants did not comment on the bandwidth of Gulick's PCI bus or on whether

it was fast enough to keep up with an input data stream. (Dkt. No. 86 at 12). Defendants assert that these statements contradict the specification. Defendants state that, in the specification, a PCI bus is real time because it has enough bandwidth. Defendants assert that, according to the file history, a PCI bus is not a real time bus because of its latency. (*Id*. at 13). Defendants assert that PUMA cannot have it both ways.

Defendants assert that PUMA's argument that the "context" of the prior art limits the prior art's disclosure is flawed. Defendants contend that it is black letter law that the prior art is relevant for all that it teaches and is not limited by the specific problem that the prior art was intended to solve. (*Id*. at 13-14). Defendants assert that Gulick is prior art for all that it teaches, regardless of context. Defendants claim that it is undisputed that Gulick taught a PCI bus and that the patentees considered a PCI bus to have sufficient bandwidth for real time operation. (*Id*. at 14). Defendants assert that, importantly, the Applicants did not dispute that the prior art PCI bus was fast enough to keep up with an input data stream. Defendants assert that any contextual differences between the asserted patents and the prior art do not change the fact that the Applicants made conflicting statements. Defendants assert that a person of ordinary skill in the art could not read the intrinsic record and know whether a PCI bus falls within the scope of the claims or not. (*Id*.).

Defendants assert that bus latency may not impact the bus's ability to keep up with the input data stream. Defendants contend that bus latency impacts the speed at which new data can be placed on the bus. (*Id*. at 16 (citing Ex. B (Stone Depo.) at 21:2-22:14)). Defendants assert even when there is substantial delay (latency) for placement of new data, once the new data is placed on the bus, a bus with enough bandwidth is still fast enough to keep up with that input data stream. (*Id*. at 16). Defendants argue that because the patentees relied on latency to

distinguish the prior art instead of bandwidth, the construction of the term "real time," based on the intrinsic record, must include latency as well. (*Id*). Thus, Defendants assert that if the term is definite, PUMA must be held to the new latency requirement. Defendants argue that, in prosecution, the Applicants modified the test for "real time" by introducing the concept of latency. Defendants assert that latency was what was used to distinguish the prior art, thus, their construction is appropriate, if the term is found definite. (*Id*. at 15).

At the oral hearing, Defendants further asserted that the specification teaches that both bandwidth and latency should be considered. In particular, Defendants cite to a passage of the '164 Patent: "a bandwidth greater than the bandwidth required for the decoder/encoder 80 to operate in real time . . . . Additionally, the latency of the bus 70 that couples the decoder/encoder 80 to the memory 50 should be considered." '164 Patent 7:60-8:2; '789 Patent 3:19-20 ("Additionally, the latency of the bus that couples the decoder to the memory should be considered.").

Analysis

PUMA and the Defendants agree that, as to the specification, the *STMicroelectronics* construction is appropriate. (Dkt. No. 78 at 9-10); (Dkt. No. 86 at 10-12, 15). In the briefing, Defendants assert that "[b]andwidth is the factor that the asserted patents rely on. The asserted patents neither focus on nor emphasize the importance of latency when they describe real time operation. Their focus is entirely on bandwidth." (Dkt. No. 86 at 10). At the oral hearing, however, Defendants position shifted as noted in the slide titled "The Specifications are Clear - Bandwidth & Latency both are Factors to Consider Whether a Bus may Operate 'In Real Time.'" Defendants pointed to the passages cited above ('164 Patent 7:60-8:2; '789 Patent 3:19-20) to

indicate that latency was also mentioned in the specification as being relevant. Against this backdrop, Defendants read more into the '164 Patent prosecution history than is proper.

Prosecution arguments, by nature, are often not clear. *Phillips*, 415 F.3d at 1317 (noting that the prosecution history represents an "ongoing negotiation" and "often lacks the clarity of the specification"). In order to show that the Applicants disavowed the well-known meaning of a term, the prosecution history must show that the patentee clearly and unambiguously disclaimed or disavowed its meaning during prosecution to obtain claim allowance. *Middleton, Inc. v. Minnesota Mining & Manuf. Co.*, 311 F.3d 1384, 1388 (Fed. Cir. 2002); *EMD Millipore Corp. v. AllPure Techs., Inc.*, 768 F.3d 1196, 1203 (Fed. Cir. 2014).

Here, the disputed prosecution history relates to the Gulick reference. The Defendants claim that the Applicants secured claim allowance by distinguishing Gulick on the grounds that Gulick's PCI bus did not allow for real time processing due to its latency. However, as evident from Figure 1 of Gulick (*see* Dkt. No. 78 at 12 (color coding added)) the system in Guilck provided a real time bus in addition to a PCI bus. Thus, as shown in Figures 1 and 3 of Gulick and stated in Gulick, a "Real-time Bus (Multimedia bus) 130A" is provided to operate as "a dedicated real-time bus or multimedia bus" in addition to the PCI bus 120. (Dkt. No. 78 Ex. R (Gulick) Figures 1 and 3, Abstract, 2:55-56). In context, the Applicants' statements were directed toward the teaching of Gulick in which Gulick clearly stated that in the system of Gulick a separate real time bus was needed in addition to the PCI bus. The Applicants did not make a clear statement of disclaimer regarding the bandwidth of the PCI bus and a PCI bus in general. The proper context to consider is (1) the prosecution history statements directed toward the particular overall prior art system of Gulick; and (2) the clear specification statements. In this context, real time has not been redefined in opposition to the specification.

As the specification states: "[t]o operate in real time the decoder/encoder 45 should decoder [sic] and/or encode images fast enough so that any delay in decoding and/or encoding cannot be detected by a human viewer." '789 Patent 6:43-46. The specification describes that bandwidth and latency can have an impact on whether a bus is fast enough to keep up with the input data. *Id*. at 3:13-20, 6:41-52; '164 Patent 7:59-8:2. The intrinsic record shows that the claim term is definite as the term has a reasonably certain meaning. *See Nautilus*, 134 S. Ct. at 2129–30. The meaning of "real time," as found in the specification, is consistent with the *STMicroelectronics* construction: "fast enough to keep up with an input data stream."

The Court construes "real time" to mean "fast enough to keep up with an input data stream."

4. "fast bus" ('368 Patent claim 7 and '045 Patent claim 4)

PUMA's Construction	Defendants' Construction
"bus with a bandwidth equal to or greater than the required bandwidth to operate in real time"	Indefinite. Alternatively: "bus [as construed] having a bandwidth sufficient to allow real time operation"

Positions of the Parties

PUMA asserts that two passages in the specification are definitional: "a fast bus 70 is any bus whose bandwidth is equal to or greater than the required bandwidth" ('459 Patent 8:1-2) and "two devices are coupled to the memory through a fast bus having a bandwidth of at least the minimum bandwidth needed for the video and/or audio decompression and/or compression device to operate in real time" ('459 Patent at 4:59-62). PUMA asserts that "real time," as used in PUMA's construction, is definite for the reasons PUMA argues separately with regard to the "real time" term. (Dkt. No. 78 AT 13). PUMA asserts that Defendants' alternative construction is

similar to PUMA's. However, PUMA asserts that its construction tracks the explicit language used in the specification. (*Id*. at 14).

Defendants did not separately brief "fast bus." At the oral hearing, Defendants acknowledged that their indefiniteness argument relies on their "real time" indefiniteness argument.

Analysis

Having found the term definite, the Court's construction relies upon the statements made in the specification. Specifically, "a fast bus 70 is any bus whose bandwidth is equal to or greater than the required bandwidth" ('459 Patent 8:1-2) and "two devices are coupled to the memory through a fast bus having a bandwidth of at least the minimum bandwidth needed for the video and/or audio decompression and/or compression device to operate in real time" ('459 Patent at 4:59-62).

The Court construes "fast bus" to mean "bus with a bandwidth equal to or greater than the bandwidth required to operate in real time."

5. "arbiter" / "arbitration circuit" / "memory arbiter" / "arbiter circuit" ('789 Patent claims 1, 19; '459 Patent claims 1-3, 7, 9, 11, 13; '194 Patent claims 1-3, 7, 9, 11, 16-18, 22, 23; '368 Patent claims 1, 5, 7, 13, 17, 19, 20, 23; '045 Patent claims 1, 4, 5, 12, 15; '753 Patent claims 1, 4, 7-10, 12; and '164 Patent claims 1, 8, 12)

PUMA's Construction	Defendants' Construction
"circuitry that uses a priority scheme to determine which requesting device will gain access"	"circuitry that uses a priority scheme to determine which requesting device will gain direct access"

The sole difference between the parties' construction is Defendants' inclusion of "direct" in their construction.

Position of the Parties

PUMA asserts that Defendants' construction relies on the prosecution history for the '459 Patent. PUMA notes that in prosecution of the '459 Patent, the patentees amended the claims to add language concerning "direct access." PUMA asserts that the amendment, for example, made the following changes: "an arbiter coupled to the decoder, the arbiter configured to determine which of at least the first device and the decoder receives direct access [for selectively providing access for the first device and the decoder] to the first memory…." (Dkt. No. 78 Ex. S at 2) (underlined and bracketed language in original). PUMA asserts that the patentee did not redefine "arbiter" but rather added other language to traverse the cited prior art. (Dkt. No. 78 at 20). PUMA asserts that the Applicants traversed the prior art by describing a specific configuration of the arbiter. (Dkt. No. 88 at 8). PUMA further notes that the claims at issue were never allowed and were subsequently cancelled and replaced with other claims. PUMA asserts that such claims did not use "direct access" but used "without also requiring a second bus." (Dkt. No. 78 at 20). PUMA asserts that Defendants, thus, seek to import a limitation into the claims that would improperly change the scope of the actual issued claims. PUMA finally notes that the agreed construction in *STMicroelectronics* conforms to PUMA's construction. *STMicroelectronics*, 327 F. Supp. 2d at 710.

Defendants assert the pending claims of the '459 Patent were rejected over the Pollmann reference which disclosed an arbiter positioned between the memory and the device needing access to the memory. (Dkt. No. 86 at 17). Defendants assert that the Applicants amended the claims to state that the arbiter provided "direct access" to the memory. (*Id.* at 17-18). Defendants assert that the Applicants amended the claims to explain how the claimed arbiter was different than the prior art. Defendants assert such amendment was a disavowal of the meaning of "arbiter."

As to PUMA's assertion that the claims were canceled and therefore no disclaimer could occur, Defendants assert that is not the law. (*Id.* at 19 (citing *Hakim v. Cannon Avent Grp., PLC*, 479 F.3d 1313, 1317 (Fed. Cir. 2007))). Defendants also assert that, in subsequent prosecution, the patentee continued to argue that arbitration was decoupled from bus access. (*Id.* at 19 (citing Dkt. No. 86 Ex. C at 1256, 1283)). As to whether disclaimer in one patent can apply to other patents, Defendants assert that the law is clear that disclaimer can apply to other related patents. At the oral hearing, Defendants further asserted that the disclaimer in question was within the "four corners" of the disclaimer in *Hakim.*

Analysis

Defendants assert that during prosecution the Applicants redefined "arbiter" in the '459 Patent. Upon review of the prosecution history in question, it is clear that the term "arbiter" itself was not redefined. The claim amendments in question did not rely on a definition of "arbiter" but rather added language which called out a particular arbiter arrangement: "an arbiter coupled to the decoder, the arbiter configured to determine which of at least the first device and the decoder receives direct access [for selectively providing access for the first device and the decoder] to the *first* memory…" (claim 1) and "an arbiter [for coupling to the memory, the arbiter] coupled to the first device, and to the decoder, the arbiter configured to control the direct access" (claim 18). (Dkt. No. 78 Ex. S at 2-3).

Reviewing the prosecution history makes clear that the Applicants did not assert that the "arbiter" distinguished the invention from prior art. Rather, it is clear that additional limitations requiring specific arbiter arrangements distinguish the invention from the prior art. For example, the Applicants added "the arbiter configured to control the direct access." The fact that words modifying "arbiter" were used in addition to the word "arbiter" indicates that "arbiter" itself does

not describe the limitations that are imposed by those other words. *See Phillips*, 415 F.3d at 1314 ("[T]he claim term in this case refers to 'steel baffles,' which strongly implies that the term 'baffles' does not inherently mean objects made of steel."). Moreover, the claims at issue explicitly do not include the referenced additional limitations. Thus, Defendants' attempts to import other limitations that were explicitly in the claims subject to the prosecution history in question, fail.

Defendants' citation to *Hakim* is not on point. Here, the word "arbiter" was in the claims initially and was distinguished, not based upon the meaning of "arbiter" but based on additional claim limitations explicitly added. That was not the case in *Hakim*. *See Hakim*, 479 F.3d at 1315-18. In context of the particular claim amendments and the Applicants' arguments, the term "arbiter" was not subject to a disclaimer or disavowal. The issued claims included "arbiter" but did not limit the claimed arbiter to a particular configuration. "An argument made to an examiner constitutes a disclaimer only if it is 'clear and unmistakable.'" *Schindler Elevator Corp. v. Otis Elevator Co.*, 593 F.3d 1275, 1285 (Fed. Cir. 2010).

The Court construes "arbiter" / "arbitration circuit" / "memory arbiter" / "arbiter circuit" to mean "circuitry that uses a priority scheme to determine which requesting device will gain access."

6. "control circuit" ('464 Patent claim 1, 2, 7-13, 16-24, 32)

PUMA's Construction	Defendants' Construction
No construction necessary.	"an electronic control device that is separate from the CPU or processor"

The issue is whether the "control circuitry" must be separate from the processor/device. The parties did not provide additional arguments at the hearing.

Positions of the Parties

PUMA asserts that the term is effectively defined by the claim language. PUMA points to claim 1 of the '464 Patent, which states that the "control circuit" is coupled to the decoding circuit, the processor, and the main memory. Furthermore, PUMA notes that the claim states that the "control circuit" is configured to "request continuous use of several portions of the main memory from the operating system" and to "translate the noncontiguous addresses to contiguous addresses of a block memory." '464 Patent claim 1.

PUMA objects to Defendants' construction for multiple reasons. First, PUMA asserts that Defendants' insertion of "device" in place of "circuit" provides no meaningful guidance. (Dkt. No. 78 at 21). Second, PUMA objects to Defendants' requirement that the "control circuit" be "separate."

PUMA asserts that the word "separate" is not defined in by the specification. PUMA also asserts that Defendants require the control circuit to be "separate" from "the CPU." PUMA points out, however, that "CPU" is not used in the claims that include "control circuit." PUMA asserts that the addition of "CPU" would, thus, cause confusion. (Dkt. No. 78 at 21). Furthermore, PUMA asserts that Defendants seek to impose a nineteen-word definition on a two-word term despite the fact that the claim language provides guidance as to the meaning and scope of the term. (*Id*.). PUMA also asserts that Defendants' "separate" requirement conflicts with the specification. PUMA asserts that the '464 Patent explicitly contemplates that multiple components "can be monolithically integrated as a single chip." '464 Patent 5:10-13. PUMA asserts that the claim just requires the "control circuit" to be "coupled" to the processor, which can be the case even if the components are monolithically integrated as a single chip. (Dkt. No. 88 at 8-9).

Defendants assert that the dispute reduces to whether or not the "control circuit": (1) is an electronic device and (2) is separate from the CPU/processor. Defendants assert that support is found in the following passage:

> Broadly stated, the present invention embodies a control circuit for use in a computer system. The computer system is controlled by an operating system and has a main memory. An electronic device is coupled to the processor and the main memory and is configured to request continuous use of several portions of the main memory from the operating system.

'464 Patent 3:37-43. Defendants contend that the figures support its construction. Defendants point to Figures 1 and 2 in the '464 Patent:

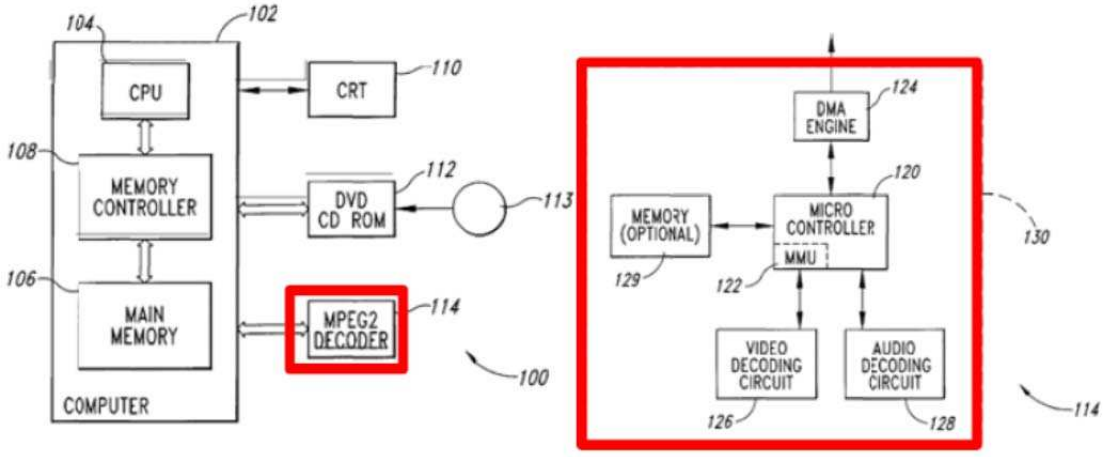


Fig. 1 *Fig. 2*

'464 Patent Figures 1 and 2 (color coding added). Defendants claim that the microcontroller 120, inside the MPEG decoder 114, performs the tasks of the claimed "control circuit." (Dkt. No. 86 at 21 (citing '464 Patent 6:63-7:50)). Defendants assert that the figures confirm that the MPEG decoder 114 is not part of the CPU and is a separate device coupled to the computer 102. Defendants assert that the specification repeatedly identified this divided architecture in context of being "the present invention." For example, Defendants point to the passages: "[t]he present invention relates to the field of electronic systems requiring blocks of memory" ('464 Patent 1:19-20), "the present invention shares the main memory 108 with the computer 102" ('464

Patent 6:60-62) and "[t]he present invention interacts with the Windows 95 operating system 152 to act like a software application" but "actually employs hardware" that "is not a CPU, or other processor, or Intel-based microprocessor" ('464 Patent 9:14-21). (Dkt. No. 86 at 21).

Defendants further assert that during prosecution, the Applicants amended independent claim 25 to include the "control circuit." Defendants assert that when adding "control circuit," the Applicants argued that "[the prior art] does not teach the administration of a memory management method through a separate control circuit . . . ." (*Id*. at 21-22 (quoting Dkt. No. 86 Ex. M at 0506, 509)). Defendants assert that if the Court ignored these repeated and consistent representations by the Applicants to the patent office the Court would improperly award the Applicants claim scope that they had surrendered during prosecution. (*Id*. at 22).

As to the term "device," Defendants contend that the term is used at column 3 line 40 to line 43 of the '464 Patent to describe "control circuit." Defendants assert that their construction, unquestionably, grounds the "control circuit" in the realm of the physical, not mere software. (Dkt. No. 86 at 22).

As to the term "separate," Defendants assert that the Applicants used this term to distinguish the prior art. Defendants assert that the fact that the patent does not provide a special definition for "separate" reinforces the fact that the jury should be well-equipped to understand the word based on common parlance. (Dkt. No. 86 at 22-23).

Defendants assert that the surrounding claim language conforms to their construction. Specifically, Defendants assert the claim language requires the "control circuit" to be "coupled" to the "processor" and "configured to request . . . from the operating system." (*Id*. at 23). Defendants assert that there should, thus, be no dispute. Defendants contend that the Court

should resolve this issue now, rather than allowing the parties to argue this dispute to the jury. (*Id*.).

Analysis

The issues and arguments presented to the Court for "control circuit" are the same as the issues and arguments presented by the parties in *Parthenon I*. *Parthenon I* Order at 41-44. The Court applies the analysis that it applied in *Parthenon I*. For the reasons described in *Parthenon I*, the Court rejects Defendants' proposal that the control circuit be a separate device. *Id.* at 44-45.

The Court finds that "control circuit" has its plain and ordinary meaning and no further construction is necessary.

7. "directly supplied" ('194 Patent claim 15 and '368 Patent claim 3) and "directly supplies" ('368 Patent claim 2, 14, 21; '045 Patent claim 2, 6, 13; '753 Patent claim 3)[4]

PUMA's Construction	Defendants' Construction
a. "supplied without being stored in main memory for purposes of decoding subsequent images"	a. Plain and ordinary meaning. Alternatively: "supplied without intervening components"
b. "supplies without being stored in main memory for purposes of decoding subsequent images"	b. Plain and ordinary meaning. Alternatively: "supplies without intervening components"

The parties dispute whether the term "directly supplied" describes (1) the way in which the components are physically connected or (2) method by which certain frames are not sent to the main memory for use in decoding other frames.

[4] The parties included '194 Patent claim 2 in the Patent Rule 4-5(d) Joint Claim Construction Chart. (Dkt. No. 90-2 at 3). However, the terms at issue are not found in that claim.

Positions of the Parties

PUMA asserts that "directly supplied" concerns the system's use of decompressed frames in the context of video coding. PUMA asserts that the phrase "directly supplied" describes the fact that certain types of frames do not need to be transferred to main memory for use in the subsequent decoding of other frames.

PUMA contends that Defendants seek to restrict the term to a description of a physical architecture of a device with no intervening components. PUMA asserts, however, that the term is not intended to be a limitation on the physical architecture or intended to exclude the use of intervening components. PUMA claims that Defendants' construction would exclude disclosed embodiments which include intervening components. Specifically, PUMA points to Figure 3 of the '194 Patent:

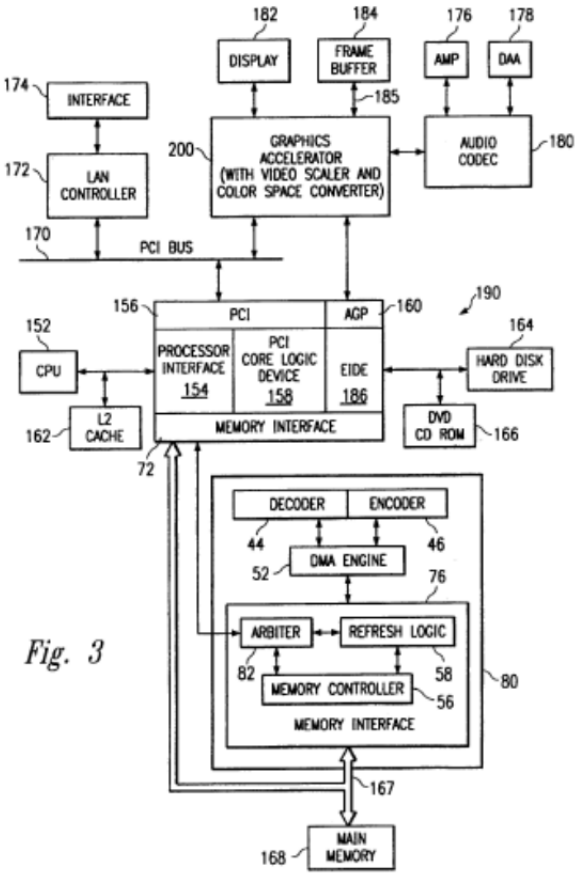


Fig. 3

’194 Patent Figure 3. PUMA states that in Figure 3, the decoder/encoder 80 is connected to the graphics accelerator 200 and the display 182 through the core logic chipset 190. PUMA asserts that Defendants’ construction would not encompass this embodiment due to the intervening core logic chipset 190 and the use of multiple buses. (Dkt. No. 78 at 16-17). PUMA asserts that adding the phrase “with no intervening components” to the construction is directly at odds with the specification.

PUMA contends that the patents do not use “directly supplied” in the context of mandating no intervening components. PUMA asserts that the phrase “directly supplied” reflects the fact that certain types of frames do not need to be transferred to main memory for use in the subsequent decoding of other frames. (*Id*. at 17). PUMA points to claim 14 of the ’194 Patent as illustrative. Claim 14 states that the “decoder directly supplies a display adapter of the display device with an image for use other than decoding a subsequent image.” PUMA also notes that claim 15 of the ’194 Patent states: “the images directly supplied to the display adapter being bidirectional images obtained from two preceding intra and predicted images.” Thus, PUMA asserts that the term “directly supplied” must be viewed in context of MPEG bidirectional decoding of video frames.

PUMA notes that the specification states “[t]he intra and predicted images are likely to be used to reconstruct subsequent predicted and bidirectional images, while bidirectional images are not used again.” ’194 Patent 3:21-25. PUMA asserts the specification, thus, notes that “a buffer associated with bidirectional images is not required, these bidirectional images B being directly supplied to display adapter 120 as they are being decoded.” ’194 Patent 10:39-42. PUMA asserts that “directly supplied” must be viewed in the context of bidirectional frames, which do not need to be stored in main memory for purposes of decoding. (Dkt. No. 78 at 18).

Defendants assert that their construction conforms to the plain meaning of "directly." Defendants assert that their construction indicates that an image that is supplied to any component, including main memory, before reaching the display adapter, is not "directly supplied." (Dkt. No. 86 at 25). Defendants contend that PUMA reads an embodiment into the claim ("without being stored in main memory"). Defendants also contend that PUMA's "for purposes of decoding subsequent images" is redundant to the given claim language. (*Id*. at 23).

Defendants assert that PUMA's sole citation to the '194 Patent is at column 10 line 39 to line 42. Defendants assert that this same section of the patent indicates that this is just "another embodiment." '194 Patent at 10:22. Defendants assert that there is no disclaimer in either the specification or file history. (Dkt. No. 86 at 24). Defendants assert that the passage in question only states that when "B" images are directly supplied to the display adapter 120 as they are being decoded, a buffer associated with these images is not required. Defendants assert that, importantly, the passage does not say that **if** the "B" images are not stored in a buffer, then the images **are** directly supplied. (*Id*.).

Defendants contend that images are directly supplied to a display adapter from a decoder. Defendants state that Figure 4 of the '194 Patent illustrates how bidirectional "B" images are provided from the decoder/encoder 80 to the video controller 120.

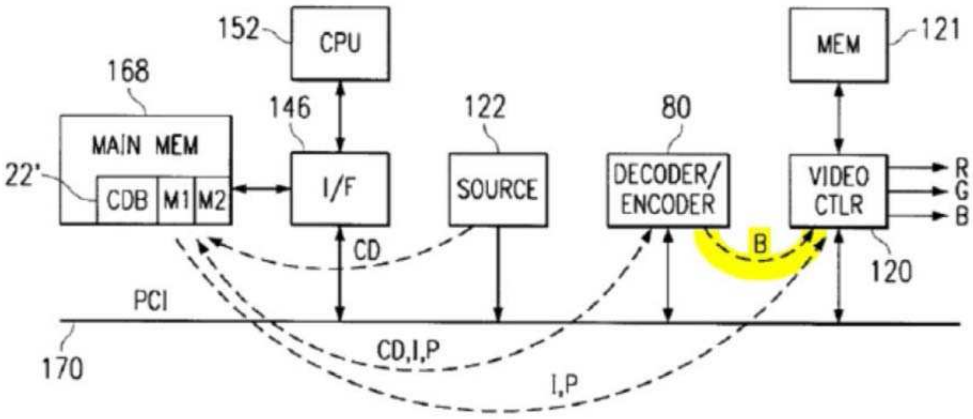


FIG. 4

'194 Patent Figure 4 (color coding adding). Defendants argue that while it is true that "B" images are not supplied to the buffer memory on the path from the decoder to the display adapter (VIDEO CLTR 120), neither are they supplied to any other component (such as I/F 146 or CPU 152). Defendants assert that under PUMA's construction, an image supplied by the decoder to other components (or any memory other than main memory) would still be considered directly supplied. (Dkt. No. 86 at 25). Defendants claim this is directly at odds with the plain meaning of "directly supplied."

Defendants contend that the phrase "for the purposes of decoding subsequent images" is redundant given the surrounding claim language. Defendants cite to claims 2, 14, and 21 of the '368 Patent and claim 3 of the '753 Patent, which include "an image under decoding which is not used to decode a subsequent image." (Dkt. No. 86 at 25). At the oral hearing, Defendants asserted that if Defendants' positions were rejected, PUMA's construction should be altered to remove "for purposes of decoding subsequent images."

Analysis

These terms arise in the context of decoded images. The specification passages in which "directly supplied" is used provides guidance as to the term's meaning in the context of the specification.

> FIG. 4 shows another embodiment of a computer where the decoder/encoder 80 is sharing the main memory 168. In this embodiment, the main memory 168 corresponds to the shared memory 50 of FIG. 2. In FIG. 4, the decoder/encoder 80 according to the present invention is connected as a peripheral to a conventional computer equipped with a fast peripheral bus 170, for example, a PCI bus, although the bus can be VESA Local Bus (VLB), an Accelerated Graphics Port (AGP) bus, or any bus having the required bandwidth. In this embodiment, the fast peripheral bus 170 corresponds to the fast bus 70. **As shown, the decoder/encoder 80 does not have a dedicated memory, but utilizes a region 22' of the main memory 168 of the computer.**
>
> Region 22' includes a Compressed Data Buffer (CDB), into which image source 122 writes the compressed image data, and **two image buffers M1 and M2 associated with intra or predicted images. As will be seen hereafter, a buffer associated with bidirectional images is not required, these bidirectional images B being directly supplied to display adapter 120 as they are being decoded.**
>
> Thus, in the system of FIG. 4, compressed or coded data CD are transferred from image source 122 to buffer CDB of memory 168. **These same compressed data are then transferred to the decoder/encoder 80 which, if they correspond to intra or predicted images, retransmits them in decoded form to buffers M1 and M2 of memory 168. In the case where the compressed data correspond to bidirectional images, the decoder/encoder 80 decodes these data and directly supplies display adapter 120 with the decoded data.** The display adapter then supplies these data to a display device such as a screen. **The intra or predicted images stored in buffers M1 and M2 are transferred to display adapter 120 at the appropriate time and are used in the decoding of subsequent predicted or bidirectional images.**

'194 Patent 10:22-56 (emphasis added). The passages above show that bidirectional images are not decoded by the decoder and then provided to the main memory for later transfer to the display adaptor. Rather, bidirectional images are provided from the decoder to the display

adaptor without being stored in the main memory. The bypassing of the main memory is the context in which "directly supplied" is utilized in the specification.

Defendants' emphasis on "no intervening" components lacks support in the specification. First, in all embodiments, the decoder provides the bidirectional images to the display adaptor through an intervening bus. Second, as noted by PUMA, the Figure 3 embodiment teaches the use of intervening chipset components, the core logic chipset, in addition to multiple intervening buses (the memory bus 167 and PCI bus 170). '194 Patent Figure 3, 9:53-10:21. Though Defendants point to Figure 4, the Court finds that the Figure 3 embodiment is also relevant. Although the movement of the MPEG I, P, and B frames is shown with regard to Figure 4, the context of the specification indicates that Figures 2 and 3 would also be relevant to MPEG frames. For example, an MPEG decoder is described with relation to the prior art Figure 1b embodiment. '194 Patent at 2:35-36. Further, decoder 80 may be found in Figures 2, 3 and 4 of the '194 Patent. The discussion of the applicability of MPEG and intrapicture/interpicture decoding and encoding is made generally with regard to decoder/encoder 80 and is not limited to Figure 4. *Id*. at 8:59-9:52. Further, the description of "directly supplied" images is discussed in the Summary of the Invention without limit to Figure 4. *Id*. at 5:31-41. In context of the overall specification, this understanding of "directly supplying" certain frames would be applicable to Figure 3. *Id*. at 5:31-41, 10:22-56. Defendants' construction would exclude Figure 3. "A claim interpretation that excludes a preferred embodiment from the scope of the claim 'is rarely, if ever, correct.'" *On-Line Techs., Inc. v. Bodenseewerk Perkin-Elmer GmbH*, 386 F.3d 1133, 1138 (Fed. Cir. 2004) (citation omitted).

Finally, as to Defendants' request to remove "for purposes of decoding subsequent images," the Court finds that such concept is central to the passages quoted above and relevant to

the meaning of the terms. Further, such language is not merely duplicative with recited claim language, as some claims do not include such language. *See* '194 Patent Claim 15, '368 Patent Claim 3.

The Court construes "directly supplied" to mean "supplied without being stored in main memory for purposes of decoding subsequent images" and "directly supplies" to mean "supplies without being stored in main memory for purposes of decoding subsequent images." [5]

8. "monolithically integrated into" / "integrated into" ('789 Patent claims 6, 21, 23; '194 Patent claim 19; '368 Patent claims 17, 23; '045 Patent claims 9, 13; '753 Patent claim 12; and '164 Patent claim 12)

PUMA's Construction	Defendants' Construction
"formed on a single semiconductor chip with"	"formed within"

The parties dispute whether the terms require a first component to be formed within a second component or merely on the same semiconductor chip.

Positions of the Parties

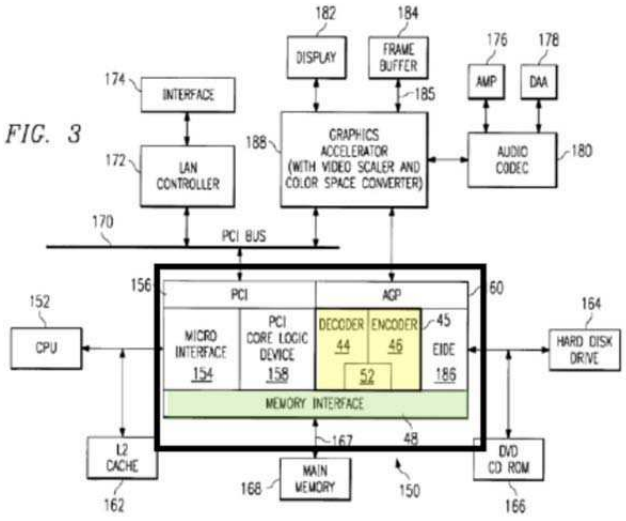
PUMA asserts that the concept of monolithic integration is well understood by a person of skill in the art. PUMA asserts that the term "monolithic" originates from the Greek words *monos* 'single' and *lithos* 'stone.' (Dkt. No. 78 at 21-22). PUMA cites to a number of extrinsic evidence dictionaries indicating that "monolithic" relates to forming structures in a single semiconductor integrated circuit. (*Id*. at 22). PUMA objects that Defendants' construction is

[5] With regard to claims that do not recite "main memory," the term "main memory" is replaced to conform to the usage in each particular claim. Thus, "main memory" is replaced with "the memory" for '194 Patent claim 15, '368 Patent claim 21 and '045 Patent claim 13. "Main memory" is replaced with "system memory" for '368 Patent claim 14 and '045 Patent claim 6.

ambiguous. For example, PUMA asserts that two components can be monolithically integrated into the same semiconductor integrated chip without one component being "formed within" the physical footprint of the other component. PUMA asserts that the purpose of monolithic integration is to reduce costs and promote efficient use of space. PUMA asserts that Defendants' construction ignores these fundamental purposes and would unnecessarily require overlapping of physical layouts. (Dkt. No. 78 at 22).

Defendants assert that PUMA's construction is inconsistent with the claims. Defendants point to the claims of the '164 Patent and note that claim 8 states "the arbiter and second memory interface are **integrated with** the decoder/encoder" while claim 12 states "the refresh logic, the arbiter, and the second memory interface are monolithically **integrated into** the decoder/encoder" (emphasis added). Defendants assert that different claim language should be treated differently, and it would be improper to construe this term in a manner that obliterates the distinction. Defendants argue that PUMA's proposal of construing "integrated into" as "formed . . . with" ignores this difference.

Defendants also assert that PUMA's construction injects a whole new element: "single semiconductor chip" that is not found in the patents. Defendants assert that it is improper to import elements from extrinsic evidence where the patent never discloses that element. (Dkt. No. 86 at 26). Defendants assert that their construction is supported by the specifications. Defendants point to Figure 3 of the '789 Patent:



'789 Patent Figure 3. Defendants assert that the specification equates the Figure 3 placement of the decoder/encoder 45 and the memory interface 48 within the core logic chipset 150 with the integration of components 45 and 48 into component 150: "FIG. 3 shows a computer where the decoder/encoder 45 and the memory interface are integrated into a core logic chipset 150" ('789 Patent at 8:37-40) and "The decoder/encoder 45 is preferably monolithically integrated into the first device as shown in FIG. 3 and FIG. 4. In FIG. 3 the decoder/encoder 45 is integrated into a core logic chipset 150" ('789 Patent at 8:30-34).

In reply, PUMA notes that the '789 Patent states that a video decompression device "can be monolithically integrated into the first device," and that this passage goes on to state integration has the advantage of "producing a better connection between the two devices." '789 Patent at 4:50-51 and 4:56-57. PUMA, thus, asserts that this passage recognizes that two devices can be separate yet still on the same semiconductor chip.

The parties did not provide additional arguments at the oral hearing.

Analysis

PUMA's arguments go to the meaning of "monolithically integrated" or "integrated" in general. However, "[w]hile not an absolute rule, all claim terms are presumed to having meaning

in a claim." *Innova/Pure Water v. Safari Water Filtration*, 381 F.3d 1111, 1119 (Fed. Cir. 2004). The claim terms in question are not just any integration but integrated "into." The parties do not appear to debate that PUMA's construction would conform to what a person skilled in the art would understand to be "monolithically integrated" or "integrated." However, the Court should also give meaning to integrated "into."

The distinction that Defendants point to, with regard to '164 Patent claims 8 and 12, is illustrative. "Integrated with" carries a broad meaning and includes for example, two devices formed on the same chip. However, when one device is claimed to be "integrated into" the second device, the "into" language should be taken into account. PUMA's construction fails to give meaning to "into." PUMA's construction also fails to provide context to the differing claims, some which require not merely integration on the same chip, but integration of one device "into" another. For example, some claims recite "decoder and arbiter circuit are integrated into a single chip." '045 Patent Claim 8; '368 Patent Claim 17. Thus, the decoder and arbiter circuit are formed in the single chip. Similarly, the "decoder is monolithically integrated into the first device" requires the decoder to be formed in the first device. '194 Patent Claim 19. Likewise, "the refresh logic, the arbiter and the second memory interface are monolithically integrated into the decoder/encoder" requires the three claimed elements to be formed in the decoder/encoder. '164 Patent Claim 12. As the parties do not dispute the meaning of "monolithically," construction of the "integrated into" will resolve the parties' dispute.

The Court construes "integrated into" to mean "formed within on a single semiconductor chip."

9. "[first, second, third] onboard memor[y ies]" ('315 Patent claims 1, 8)

PUMA's Construction	Defendants' Construction

No construction necessary	"[first, second, third] memory within the decoder"

The parties dispute whether "onboard" refers to being on the same circuit board as the decoder or being part of the decoder.

Position of the Parties

PUMA asserts that the meaning is straightforward: the memory is onboard. (Dkt. No. 78 at 25). Though the term is not utilized in the '315 Patent specification, PUMA asserts that the specification discusses "motherboard" and "removable boards." '315 Patent at 2:66-67. PUMA asserts that the claims discuss an "image decoder circuit" that includes "onboard memory." PUMA asserts that, in this context, one skilled in the art would understand the term to refer to memory that is on the board with the decoder, as opposed to memory that is on a separate circuit board. (Dkt. No. 78 at 25). PUMA asserts that a memory could be located on the same circuit board as the decoder without being "within" the decoder. (*Id*.).

Defendants assert that the patents generally are directed to devices that share an external memory over a bus. Defendants assert that the patents distinguish this from the use of dedicated memory on a device. (Dkt. No. 86 at 28). Defendants note that claim 1 of the '315 Patent recites both an "image decoder circuit" and a "shared memory." Furthermore, Defendants note that the claim states that the "image decoder circuit including: a first onboard memory; a second onboard memory; a third onboard memory . . . ." Though the term "onboard" is not found in the specification, Defendants note that the specification teaches a decoder that has three first-in first-out (FIFO) memories. In particular, Figure 6 is described as "an embodiment of an MPEG decoder architecture" ('315 Patent 6:22-24) and includes three FIFO memories within the decoder circuit:

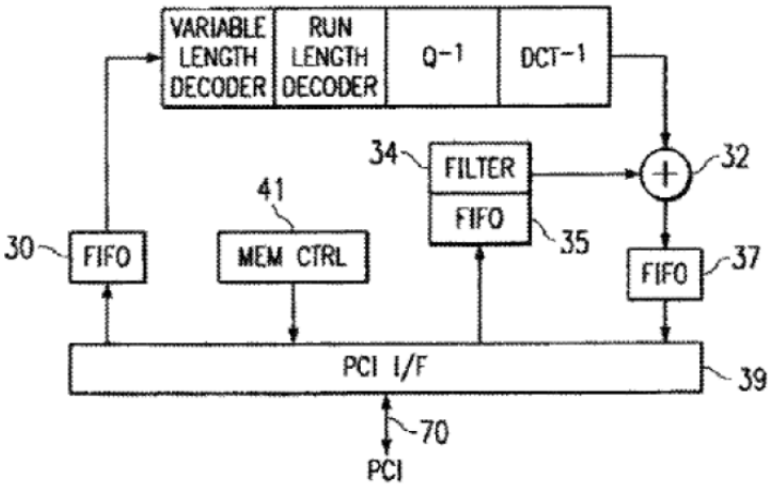


Fig. 6

'315 Patent Figure 6. Defendants assert that PUMA offers no evidence that the term relates to merely being located on the same circuit board as the decoder. (Dkt. No. 86 at 29). Defendants assert that the claims do not recite circuit boards at all, and that the single reference to "motherboards" and "removeable boards" that PUMA identifies is a discussion of the prior art. Defendants further assert that this discussion of the prior art does not relate to where a decoder's memory resides. (*Id.*).

The parties did not provide additional arguments at the oral hearing.

Analysis

PUMA argues that the ordinary meaning of "onboard" merely means on a circuit board. However, PUMA has not pointed to any intrinsic or extrinsic evidence that supports such a construction. The context of the claims is with reference to "the image decoder circuit including: a first onboard memory; a second onboard memory; a third onboard memory . . . ." '315 Patent Claim 1. PUMA's citation to the disclosure in the background describing "motherboard" and

"removable boards" is not relevant to the usage of the term in the claim, specifically a decoder including the claimed elements.

Moreover, the intrinsic record provides a meaning consistent with Defendants' proposal. First, the claims describe an "image decoder circuit **including**: a first onboard memory; a second onboard memory; a third onboard memory." This makes clear that the memories are part of the decoder circuit. Second, the specification description and figures conform to an interpretation of the term as one in which the claimed elements are part of the decoder. '315 Patent 6:22-24, 11:57-6:67, Figure 6.

The Court construes "[first, second, third] onboard memory" and "[first, second, third] onboard memories" to mean "[first, second, third] memor[y, ies] within the decoder."

10. "contiguous" / "noncontiguous" ('464 Patent claims 1, 7, 9-10, 16, 19, 22, 32-36)

PUMA's Construction	Defendants' Construction
No construction necessary	a. "adjacent" b. "non-adjacent"

The parties do not disagree as to the proper meaning of these terms or that one skilled in the art would understand the meaning. The parties merely disagree as to what would be the most helpful presentation of the meaning of these terms to a jury.

Positions of the Parties

PUMA asserts that, in the context of the memory addresses, a person skilled in the art would understand the meaning of the terms. PUMA asserts that Defendants' construction does not add clarity to the meaning of the terms. PUMA claims that by changing the language of the terms, Defendants' construction risks changing the claim scope and causing jury confusion. (Dkt.

No. 78 at 23). PUMA asserts that, as an example, the term "adjacent" may connote a geographic proximity. Thus, PUMA asserts that a jury could conclude that the memory addresses require the corresponding memory cells to be in physical proximity on the memory chip. (*Id*.). PUMA asserts that this would exclude contiguous memory addresses that are not physically adjacent on the chip.

Defendants assert that a jury is not likely to understand the terms in the context of computer memory addresses. (Dkt. No. 86 at 29). Defendants assert that, in memory addresses, a set of contiguous memory addresses could be from address 105 to address 109, including addresses 105, 106, 107, 108 and 109. (*Id*.). Defendants assert that a jury may confuse the term "contiguous" with other meanings of the term, such as when used in with reference to the 48 "contiguous" United States, a meaning related to sharing borders. Defendants assert that "adjacent" will help the jury readily understand that each memory address must immediately follow the prior address. (*Id*. at 29-30). Defendants assert that PUMA conflates addresses with physical locations. Defendants assert that the claims make clear that what is contiguous is the memory addresses, not the physical location of the memory cells. (*Id*. at 30). Defendants assert that not construing the terms runs the risk of the jury applying the usage of such terms from other contexts - contexts that are not appropriate for memory addresses.

In reply, PUMA asserts that the substitution of "adjacent" for "contiguous" runs the very risk that Defendants complain of: that the jury will utilize the term in the manner of other contexts that are not appropriate for memory addresses. PUMA asserts that Defendants' usage of entirely different words as opposed to the claim language would compound the risk of jury misunderstanding. (Dkt. No. 88 at 10).

Analysis

At the oral hearing, it was clear that the parties did not have different understandings with respect to the meaning of the terms. In addition, the parties did not dispute that one skilled in the art would readily understand the meaning of the terms. The parties sought to identify the best approach to conveying the well-understood meaning of the terms to the jury because the jury might accidentally consider the term in a "geographic" sense.

From the perspective of one skilled in the art, the parties have not identified any potential confusion, particularly in light of the specification. Further, Defendants have not identified any possible differing interpretations that one skilled in the art could have, such that construction would be needed. Ultimately, an expert could easily explain the meaning in the context of addresses, such as addresses 105, 106, and 107, as opposed to the geographic common borders example described by Defendants.

The Court finds that "contiguous" and "noncontiguous" have their plain and ordinary meaning and no further construction is necessary.

11. Coupled Terms

"coupled" ('789 Patent claims 1, 5, 15; '368 Patent claims 1, 7, 13, 19, 20; '045 Patent claims 1, 4, 5, 12; '753 Patent claims 1, 7; '315 Patent claim 1, 14, 15 and '164 Patent claims 1, 8, 9, 11; and '464 claims 1, 8, 10, 12, 13, 17, 19-21, 23, 33-35)

"coupleable" ('045 Patent claims 1, 4, 12; '753 Patent claim 7; '315 Patent claim 1 and '164 Patent claim 1)

"coupling" ('789 Patent claim 1 and '194 Patent claims 1, 16, 17)

PUMA's Construction	Defendants' Construction
a. "directly or indirectly connected" b. "directly or indirectly connectable" c. "directly or indirectly connecting"	Plain and ordinary meaning. No construction necessary.

Defendants did not brief the term "coupled" and the parties did not provide oral argument as to this term. However, the parties still list the term as disputed in the parties' final joint claim construction chart. (Dkt. No. 90-2 at 4).

PUMA cites to three Eastern District of Texas cases which have construed "coupled" to mean directly or indirectly connected. (Dkt. No. 78 at 14). PUMA also asserts that the specifications utilize "coupled" to reference elements that are indirectly connected. For example, PUMA cites to '789 Patent Figure 1b which shows a memory interface 18 that connects to an audio decoding circuit 14, and the audio decoding circuit 14 is, in turn, connected to a memory 22. PUMA notes that the specification states that the "memory interface 18 is coupled to memory 22." '789 Patent 2:25. Similarly, PUMA points to '789 Patent Figure 2 which shows a decoder/encoder 45 connected to a memory interface 48, and the memory interface 48 is, in turn, connected to memory 50. PUMA notes that the specification states that "decoder/encoder 45 is coupled to the memory 50 through devices, typically a bus 70." *Id*. 6:29-30. PUMA notes that the '459 Patent has similar passages. (Dkt. No. 78 at 16 (citing '459 Patent 2:28, 7:39-42)). PUMA also notes that the patents use "coupled" to refer to direct connections such as in '789 Patent Figure 2: "DMA engine 60 of the first device is coupled to the arbiter 54 of the memory interface 48." '789 Patent 6:15-17.

PUMA asserts that Defendants do not appear to dispute that the term "coupled" includes both direct and indirect connections. (Dkt. No. 78 at 16). Though the Defendants assert that no

construction is necessary, PUMA notes that the *Parthenon I* defendants disagreed with the plain and ordinary meaning. Thus, PUMA explicitly proposed its construction of "direct and indirect" in *Parthenon I*. PUMA requests that the Court explicitly construe the term "coupled" in both cases.

Analysis

It is unclear as to whether the Defendants assert that the plain and ordinary meaning of the term includes direct and indirect connections. Thus, it is unclear whether a dispute really exists even though the term was presented in the final claim chart without agreement. (Dkt. No. 90-2 at 4). Because the intrinsic evidence shows that "coupled" includes both direct and indirect connections, the Court rejects any argument that states that the Court's construction of coupled requires a "direct" connection. The Court's analysis in *Parthenon I* supports this finding. *Parthenon I* Order at 30-34.

The Court construes "coupled" to mean "directly or indirectly connected," "coupleable" to mean "directly or indirectly connectable," and "coupling" to mean "directly or indirectly connecting."

CONCLUSION

The Court adopts the above constructions. The parties are ordered that they may not refer, directly or indirectly, to each other's claim construction positions in the presence of the jury. Likewise, the parties are ordered to refrain from mentioning any portion of this opinion, other than the actual definitions adopted by the Court, in the presence of the jury. Any reference to claim construction proceedings is limited to informing the jury of the definitions adopted by

the Court.

IT IS SO ORDERED.

SIGNED this 24th day of January, 2016.

ROY S. PAYNE
UNITED STATES MAGISTRATE JUDGE