UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

PARTHENON UNIFIED MEMORY ARCHITECTURE LLC,	§	
	§	
Plaintiff,	§	
	§	
v.	§	Case No. 2:15-cv-00225-JRG-RSP (Lead)
	§	
ZTE CORP., ZTE USA, INC. AND ZTE (TX), INC.,	§	
	§	
Defendants.	§	

MEMORANDUM OPINION AND ORDER

On October 26, 2015, the Court held a hearing to determine the proper construction of the disputed terms in nine Asserted Patents. The Court, having considered the parties' claim construction briefing (Dkt. Nos. 56, 60, and 64) and their arguments at the hearing, issues this Memorandum Opinion and Order construing the disputed terms.

BACKGROUND AND THE ASSERTED PATENTS

Parthenon Unified Memory Architecture LLC ("PUMA") brought this action against ZTE Corp., ZTE USA, Inc., and ZTE (TX), Inc. (collectively, "Defendants") alleging that Defendants infringe U.S. Patent Nos. 5,812,789 ("the '789 Patent"), 6,058,459 ("the '459 Patent"), 6,427,194 ("the '194 Patent"), 7,321,368 ("the '368 Patent"), 7,542,045 ("the '045 Patent"), 7,777,753 ("the '753 Patent"), 8,054,315 ("the '315 Patent"), 8,681,164 ("the '164 Patent") and 5,960,464 ("the '464 Patent") (collectively, "the Asserted Patents"). The '789 Patent and the '459 Patent were filed on the same day, have similar specifications, and incorporate each other by reference. Six patents are based on continuation applications of the '459 Patent: the '194 Patent, the '368 Patent, the '045 Patent, the '753 Patent, the '315 Patent,

and the ’164 Patent.[1] All nine Asserted Patents were subject to claim construction orders issued by this Court in *Parthenon Unified Memory Architecture, LLC v. HTC Corp. et al.*, 2:14-cv-0690-JRG-RSP, Dkt. No. 155 (E.D. Tex. July 30, 2015) (“the *Parthenon I* Order”) and *Parthenon Unified Memory Architecture, LLC v. Samsung Elecs. Co., Ltd. et al.*, 2:14-cv-902-JRG-RSP, Dkt. No. 155 (E.D. Tex. Jan. 24, 2016) (“the *Parthenon II* Order”). Furthermore, one additional Eastern District of Texas claim construction order involved the ’789 Patent. *STMicroelectronics, Inc. v. Motorola, Inc.*, 327 F. Supp. 2d 687 (E.D. Tex. 2004).

In general, the ’789 Patent, the ’459 Patent, the ’194 Patent, the ’368 Patent, the ’045 Patent, the ’753 Patent, the ’315 Patent, and the ’164 Patent relate to systems in which a first device (for example a processor) and a decoder/encoder share a common memory. The ’459 Patent abstract recites:

> An electronic system provides direct access between a first device and a decoder/encoder and a memory. The electronic system can be included in a computer in which case the memory is a main memory. Direct access is accomplished through one or more memory interfaces. Direct access is also accomplished in some embodiments by direct coupling of the memory to a bus, and in other embodiments, by direct coupling of the first device and decoder/encoder to a bus. The electronic system includes an arbiter for determining access for the first device and/or the decoder/encoder to the memory for each access request. The arbiter may be monolithically integrated into a memory interface of the decoder/encoder or the first device. The decoder may be a video decoder configured to decode a bit stream formatted to comply with the MPEG-2 standard. The memory may store predicted images which are obtained from a single preceding image and may also store intra images. Bidirectional images which are directly supplied to a display adapter may be obtained from two preceding intra or predicted images.

’459 Patent Abstract.

[1] The specification of the ’464 Patent is not shared by the other Asserted Patents.

The ’464 Patent relates, generally, to a system whereby a decoder, which requires contiguous blocks of memory, can utilize noncontiguous blocks of the system’s memory. The ’464 patent abstract recites:

> A method and apparatus employing a memory management system that can be used with applications requiring a large contiguous block of memory, such as video decompression techniques (e.g., MPEG 2 decoding). The system operates with a computer and the computer's operating system to request and employ approximately 500 4-kilobyte pages in two or more noncontiguous blocks of the main memory to construct a contiguous 2-megabyte block of memory. The system can employ, on a single chip, a direct memory access engine, a microcontroller, a small block of optional memory, and a video decoder circuit. The microcontroller retains the blocks of multiple pages of the main memory, and the page descriptors of these blocks, so as to lock down these blocks of memory and prohibit the operating system or other applications from using them. The microcontroller requests the page descriptors for each of the blocks, and programs a lookup table or memory mapping system in the on-chip memory to form a contiguous block of memory. As a result, the video decoder circuit can perform operations on a 2-megabyte contiguous block of memory, where the microcontroller employs the lookup table to translate each 2-megabyte contiguous address requested by the video decoder circuit to its appropriate page in the main memory. As soon as the video decoding operations are complete, the microcontroller releases the blocks of multiple pages of memory back for use by the computer.

’464 Patent Abstract.

APPLICABLE LAW

1. Claim Construction

“It is a ‘bedrock principle’ of patent law that ‘the claims of a patent define the invention to which the patentee is entitled the right to exclude.’” *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (quoting *Innova/Pure Water Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)). To determine the meaning of the claims, courts start by considering the intrinsic evidence. *Id.* at 1313; *C.R. Bard, Inc. v. U.S. Surgical Corp.*, 388 F.3d 858, 861 (Fed. Cir. 2004); *Bell Atl. Network Servs., Inc. v. Covad Commc’ns Grp., Inc.*, 262 F.3d 1258, 1267 (Fed. Cir. 2001). The intrinsic evidence includes the claims themselves, the

specification, and the prosecution history. *Phillips*, 415 F.3d at 1314; *C.R. Bard, Inc.*, 388 F.3d at 861. Courts give claim terms their ordinary and accustomed meanings as understood by one of ordinary skill in the art at the time of the invention in the context of the entire patent. *Phillips*, 415 F.3d at 1312–13; *Alloc, Inc. v. International Trade Comm'n*, 342 F.3d 1361, 1368 (Fed. Cir. 2003).

The claims themselves provide substantial guidance in determining the meaning of particular claim terms. *Phillips*, 415 F.3d at 1314. First, a term's context in the asserted claim can be very instructive. *Id*. Other asserted or unasserted claims can also aid in determining the claim's meaning, because claim terms are typically used consistently throughout the patent. *Id*. Differences among the claim terms can also assist in understanding a term's meaning. *Id*. For example, when a dependent claim adds a limitation to an independent claim, it is presumed that the independent claim does not include the limitation. *Id*. at 1314–15.

"[C]laims 'must be read in view of the specification, of which they are a part.'" *Id*. (quoting *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995) (en banc)). "[T]he specification 'is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.'" *Id*. (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)); *Teleflex, Inc. v. Ficosa N. Am. Corp.*, 299 F.3d 1313, 1325 (Fed. Cir. 2002). This is true because a patentee may define his own terms, give a claim term a different meaning than the term would otherwise possess, or disclaim or disavow the claim scope. *Phillips*, 415 F.3d at 1316. In these situations, the inventor's lexicography governs. *Id*. The specification may also resolve ambiguous claim terms "where the ordinary and accustomed meaning of the words used in the claims lack sufficient clarity to permit the scope of the claim to be ascertained from the words alone." *Teleflex, Inc.*, 299 F.3d at

1325. But, "'[a]lthough the specification may aid the court in interpreting the meaning of disputed claim language, particular embodiments and examples appearing in the specification will not generally be read into the claims.'" *Comark Commc'ns, Inc. v. Harris Corp.*, 156 F.3d 1182, 1187 (Fed. Cir. 1998) (quoting *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1560, 1571 (Fed. Cir. 1988)); *see also Phillips*, 415 F.3d at 1323. The prosecution history is another tool to supply the proper context for claim construction because a patent applicant may also define a term in prosecuting the patent. *Home Diagnostics, Inc., v. Lifescan, Inc.*, 381 F.3d 1352, 1356 (Fed. Cir. 2004) ("As in the case of the specification, a patent applicant may define a term in prosecuting a patent.").

Although extrinsic evidence can be useful, it is "'less significant than the intrinsic record in determining the legally operative meaning of claim language.'" *Phillips*, 415 F.3d at 1317 (quoting *C.R. Bard, Inc.*, 388 F.3d at 862). Technical dictionaries and treatises may help a court understand the underlying technology and the manner in which one skilled in the art might use claim terms, but technical dictionaries and treatises may provide definitions that are too broad or may not be indicative of how the term is used in the patent. *Id*. at 1318. Similarly, expert testimony may aid a court in understanding the underlying technology and determining the particular meaning of a term in the pertinent field, but an expert's conclusory, unsupported assertions as to a term's definition are entirely unhelpful to a court. *Id*. Generally, extrinsic evidence is "less reliable than the patent and its prosecution history in determining how to read claim terms." *Id*.

2. Claim Indefiniteness

Patent claims must particularly point out and distinctly claim the subject matter regarded as the invention. 35 U.S.C. § 112, ¶ 2. "[I]ndefiniteness is a question of law and in effect part of

claim construction." *ePlus, Inc. v. Lawson Software, Inc.*, 700 F.3d 509, 517 (Fed. Cir. 2012). A party challenging the definiteness of a claim must show it is invalid by clear and convincing evidence. *Young v. Lumenis, Inc.*, 492 F.3d 1336, 1345 (Fed. Cir. 2007).

The definiteness standard of 35 U.S.C. § 112, ¶ 2 requires that:

> [A] patent's claims, viewed in light of the specification and prosecution history, inform those skilled in the art about the scope of the invention with reasonable certainty. The definiteness requirement, so understood, mandates clarity, while recognizing that absolute precision is unattainable. The standard we adopt accords with opinions of this Court stating that "the certainty which the law requires in patents is not greater than is reasonable, having regard to their subject-matter."

Nautilus, Inc. v. Biosig Instruments, Inc., 134 S. Ct. 2120, 2129–30 (2014) (internal citations omitted).

3. Construing Claim Terms that Have Previously Been Construed by This Court or Other Courts

This is not the first time a Court in this District has construed some of the disputed terms. The *Parthenon I* Order and *Parthenon II* Order construed a number of the presently disputed terms, and in *STMicroelectronics, Inc. v. Motorola, Inc.*, 327 F. Supp. 2d 687 (E.D. Tex. 2004) the Court construed the '789 Patent. These previous constructions are not controlling here but can be instructive and will, at times, provide part of the basis for the Court's analysis. *See Burns, Morris & Stewart Ltd. P'ship v. Masonite Int'l Corp.*, 401 F. Supp. 2d 692, 697 (E.D. Tex. 2005) (while a previous construction may be instructive and provide the basis of the analysis, the previous construction is not binding on the Court, particularly when there are new parties and those parties have presented new arguments).

AGREED TERMS

The parties agreed to the following constructions in their joint claim construction chart:

Term	Agreed Construction
"simultaneously accesses the bus" ('789 Patent claim 1)	"accesses the bus at the same time"
"display device" ('194 Patent claims 1, 3, 7, 11, 16-17; '368 Patent claims 1, 7, 13, 14, 20, 21; '045 Patent claims 1, 4-6, 12, 13; and '753 Patent claims 1, 7)	"screen and its circuitry"
"display adapter" ('368 Patent claims 2, 3; '045 Patent claim 2; and '753 Patent claim 3)	"an adapter that processes images for a display device"

(Dkt. No. 65-2 at 4-5.)

DISPUTED TERMS

1. **"bus" ('789 Patent claims 1, 13, 15, 28; '459 Patent claims 1, 2, 7, 11, 13; '194 Patent claims 1, 2, 9, 11, 16-18, 23; '368 Patent claims 1, 5, 7, 13, 19, 20, 23; '045 Patent claims 1, 4, 5, 12, 15; '753 Patent claims 1, 7; '315 Patent claim 1 and '164 Patent claims 1, 6, 7)**

PUMA's Construction	Defendants' Construction
No construction necessary. Alternatively: "a signal line or a set of associated signal lines to which a number of devices are coupled and over which information may be transferred between them"	"a signal line or set of associated signal lines to which a number of devices are connected and over which information may be transferred by only one device at a time"

The parties dispute (1) whether devices must be "connected" verses "coupled" to a bus and (2) whether a bus may only transfer information one device at a time.

Positions of the Parties

PUMA asserts that the term "bus" is known in the art and does not need construction. Its alternative construction comes from *STMicroelectronics*. In *STMicroelectronics*, the parties agreed to "a signal or set of signal lines to which a number of devices are coupled and over which information may be transferred between them." *STMicroelectronics*, 327 F. Supp. 2d at

711. PUMA asserts its construction is consistent with an IEEE extrinsic evidence dictionary. (Dkt. No. 56 at 6.)

PUMA objects to Defendants' construction with regard to the "one device at a time" limitation. PUMA asserts that such limitation would read out common bus technologies such as split-transaction buses and other buses that can transfer information between multiple devices at the same time. PUMA points to the prior art described in U.S. Patent No. 4,785,394 (the '394 Patent) which shows a split-transaction bus where multiple devices use the bus at the same time: For example, the '394 Patent states: "During the time period which elapses between the read address signal and the response from the memory, the other processors in the computer system are communicating other signals to other components of the system over the bus." (Dkt. No. 56 at 6-7 (quoting Dkt. No. 56 Ex. L at 1:58–62).)

PUMA also points to the prior art Mercury RACEway bus as a bus that allows multiple devices to send information at the same time. (*Id*. at 7.) PUMA asserts that Defendants' construction would exclude this prior art bus. PUMA notes that the defendants in *Parthenon II* characterized the Mercury RACEway bus as a "fabric" but that PUMA identified documents associated with the chips in the *Parthenon II* defendants' products that characterized the "fabric" as a bus. (*Id*.) In its reply, PUMA notes that Defendants removed the word "directly" from their proposed construction. Based on such removal, PUMA asserts that the only issue in dispute is the "one device at a time" limitation. (Dkt. No. 64 at 1.)

Defendants incorporate by reference the evidence and arguments of the defendants from *Parthenon II*. (Dkt. No. 60 at 3.)[2] Defendants summarized the *Parthenon II* arguments that it adopted as follows:

> • The construction of "bus" from the *Parthenon I* Order is incomplete because it does not provide sufficient guidance on where one bus ends and another bus begins.
>
> • The limitation "by only one device at a time" clarifies that, if two devices may transmit at the same time on different signal lines, those lines are not part of a single "bus."
>
> • Using the term "coupled" to define a "bus" makes it impossible to differentiate between one bus and two buses.

(*Id*.).

Defendants assert that the *Parthenon I* Order made clear that the PCI bus, ISA bus and memory bus lines are separate buses. Defendants state, however, that the *Parthenon I* Order left room for mischief and confusion at trial. (*Id*. at 4.) Specifically, Defendants assert that the construction in that Order did not provide a method for determining whether one set of lines is part of a bus. (*Id*.)

Furthermore, Defendants state that the lines of a bus are a shared transmission medium and that a "one device at a time" limitation is fundamental to a shared medium. (*Id*.) Defendants assert that if more than one device could simultaneously transmit data over a "set of associated signal lines," then that set of signal lines is not a bus within the meaning of the patents-in-suit. (*Id*. at 4–5.) Defendants assert that there would be collisions if more than one device transmitted

[2] Defendants' responsive brief did not provide substantive argument for six of the nine disputed term groupings. Rather, Defendants merely incorporated by reference arguments, exhibits and even expert reports/testimony from the *Parthenon I* or *II* cases. The Court does not approve of such techniques. Though the Court has considered such arguments here, in circumstances in which the Court views such briefing techniques as skirting this District's local rules regarding disclosures, page limits, expert testimony, evidence, etc. the Court may decide otherwise.

at a time. Defendants assert that mechanisms such as the "arbiter" in the patents prevent or deal with these collisions. (*Id*. at 5–6.)

Defendants counter PUMA's assertions in three ways. First, Defendants assert that every bus described in the Asserted Patents has a shared medium in which only one device at a time can transmit. (*Id*. at 6.) Second, Defendants contend that "one device at a time" does not exclude split-transaction bus protocols. Defendants assert that a split-transaction bus does not allow two devices to transmit at once. Defendants claim that even in a split-transaction bus any particular transaction is split into a request and a response. (*Id*.) Defendants assert that while one device's transaction is being worked on (for example the request is worked on), other devices can transmit on the bus. However, Defendants assert only one device is transmitting at a time. (*Id*. 6-7, n. 10.) Third, Defendants disagree with PUMA's statements on the Mercury RACEway. Defendants agree that their construction would exclude the Mercury RACEway. Defendants assert, however, that the Mercury RACEway is not a bus (*id*. at 7) and that even if it were an exotic species of bus, it would be very different from the buses in the specification.

Defendants assert that the intrinsic record does not show that the inventors considered a "bus" to be anything other than the type of bus discussed in the specification. Defendants state that the specification and file history do not mention fabrics or crossbars. Therefore, Defendants assert that PUMA is not entitled to a construction that is divorced from the context of the intrinsic record. (*Id*.) Defendants further assert that the RACEway is not a bus but rather a crossbar extension to a VMEbus. Defendants cite to an explanation provided by Mercury Systems:

> As a backward-compatible upgrade, Interlink modules transform the topology of an existing VMEbus chassis from a single transaction bus to a scalable real-time fabric . . . .

(Dkt. No. 60 at 8 (quoting Dkt. 56 Ex. O at 1).) Defendants assert that Mercury System's literature describes the product as something that works with ordinary buses:

> The RACEway interconnect fabric provides a uniform communications medium that connects processors, I/O devices, and standard bus interfaces, such as VME and VSB, in a consistent way throughout the system.

(*Id*. (quoting Dkt. 56 Ex. O at 3-4).) Defendants assert that the term "bus" is never used to refer to the RACEway system, except insofar as a "bus" is something that RACEway connects to and transforms. (*Id*.) Defendants assert that in context of the patents, the RACEway creates additional connections between the devices through the RACEway crossbar, so that the devices do not need to use the actual bus. Defendants assert that because the RACEway allows multiple devices to transmit at once, it is not a shared medium that each connected device uses to transmit.

Defendants assert that the additional documents that PUMA cites to regarding the RACEway are third party non-Mercury Systems documents. Defendants assert that third party descriptions of the RACEway are not relevant and not probative. Defendants contend that any evidentiary value they may possess is far outweighed by the relevant intrinsic record. (*Id*. at 9.) Defendants point out that the first additional document PUMA cites (PUMA's Exhibit N) relates to military digital signal processor architectures. Defendants assert that the document references different types of buses including control buses, data buses (Defendants consider RACEway a data bus), test buses, input/output buses, local/wide area network buses, and PC buses. Defendants assert that all the examples of buses in the patent fall within the PC bus category. (*Id*. at 10.) Defendants assert that though other examples of buses are listed, such examples are not useful in the context of the patents-in-suit which are about personal computer or system-on-chip architectures. (*Id*.) As to PUMA's Exhibit M, Defendants assert that this document relates to

military radar systems and on one page refers to Mercury RACEway Bus. (*Id*.) Defendants assert that the description is inaccurate. Further, Defendants assert the field (radars) is not relevant to the technology and audience of the patents-in-suit. (*Id*.)

As to PUMA's Exhibit X (which appears to use "fabric" interchangeably with "bus"), Defendants assert the document is not relevant. Defendants note that the document is dated 2011, and, thus, assert that it is not probative on the use of the term "bus" fifteen years earlier. Defendants further assert that the document contains no technical disclosure as to the meaning of the term "fabric." Defendants assert that "fabric" could mean a "bus" like those disclosed in the patent (one device at a time) or could mean a type of switched network of buses. Defendants contend that would not be a "bus" as used in the patent but rather a collection of multiple buses. (*Id*. at 11.) Finally, Defendants state that the removal of "direct" from Defendants' construction has rendered the arguments over "direct" moot. (*Id*.)

In reply, PUMA reiterates that split-transaction buses and the Mercury RACEway bus would be excluded by Defendants' construction. As to the split-transaction bus, PUMA asserts that Defendants admit that, in a split-transaction bus, while the request from one device "is being worked on, other devices can transmit on the bus." (Dkt. No. 64 at 2 (quoting Dkt. No. 60 at 6-7).) PUMA asserts that Defendants' construction, thus, excludes split-transaction buses. PUMA state that Defendants attempt to avoid this problem by differentiating between requests and responses and by suggesting that a bus can handle only one of each type of transaction at a time. PUMA asserts that Defendants' construction does not reflect this distinction. PUMA notes that "request" and "response" transactions are not mentioned in the patents. (*Id*.) PUMA asserts this would create jury confusion.

PUMA contends that Defendants admit that their construction excludes the Mercury RACEway. (*See id*. ("PUMA is correct that the term 'bus' as used in the patents-in-suit would not read on Mercury RACEway.") (quoting Dkt. No. 60 at 7).) PUMA asserts that the patents use the term "bus" generally without disclaimer. PUMA asserts that, as a result, Defendants' attempt to carve out some buses from the construction should be rejected.

PUMA responds to Defendants' argument that the Mercury RACEway is not a bus. PUMA asserts that persons of ordinary skill in the art disagree with Defendants. PUMA asserts that the exhibits cited by PUMA repeatedly refer to the Mercury RACEway as a bus. (*Id*. (citing Dkt. No. 56 Ex. N at 203 and Ex. M at 31).) PUMA notes that Exhibit N states that "some currently available choices for a data bus" include "RACEway (Mercury Computer)." (Dkt. No. 56 Ex. N at 203.) PUMA also notes prior art that states "[t]he Mercury Raceway bus is an important part of the IFB architecture" and "[t]he P2 connector is also used to propagate the Raceway bus from board to board." (Dkt. No. 56 Ex. M at 31.) As to Defendants' quote from Exhibit O, PUMA asserts that it supports PUMA's position. PUMA asserts that the document states that the Mercury Interlink modules transform the topology from "a single transaction bus to a scalable real-time fabric." PUMA asserts that the document distinguishes between two types of buses: "single transaction buses" and "real-time fabrics." PUMA asserts that under Defendants' argument, the phrase "single transaction" would be entirely redundant because all buses under Defendants' construction would presumably be "single transaction" buses.

PUMA asserts that the Qualcomm technical documents that are central to this case refer to the fabric as a type of bus. (Dkt. No. 64 at 3 (noting that Dkt. 56 Ex. X at 67 states that there are "three buses that span the entire MSM device" and lists the "system fabric," "applications fabric" and "system fast peripheral bus.").) PUMA cautions that it has raised this evidence for

the simple purpose of assuring the Court that persons of ordinary skill in the art have always understood the term "bus" to be broad and inclusive. PUMA asserts that based on the evidence associated with the Mercury RACEway bus and the Qualcomm fabrics, persons of skill in the art have not restricted the term "bus" in the manner urged by Defendants. (*Id*.)

At the oral hearing, Defendants acknowledged that the *Parthenon I* and *Parthenon II* constructions were technically correct but did not provide adequate jury guidance as to where one bus begins and another bus ends. (Dkt. No. 69 at 7 (hereinafter "Oral Hearing Tr.").) Defendants also asserted that "connected" vs. "coupled" was not a primary dispute as that dispute is better addressed with regard to the "coupled" claim term dispute. (*See id.* at 12.) Defendants also acknowledge that they rely on the expert testimony from the *Parthenon II* case and that the expert from the *Parthenon II* case never stated that a structure that could handle two or more devices at the same time was not a bus. (*Id.* at 15-17.) At the Oral Hearing, Defendants emphasized that any given wire can only transmit voltages from one device at any particular time. (*Id*. at 17.)

Analysis

The analysis from *Parthenon I* and *Parthenon II* applies to the arguments raised by the parties. *Parthenon I* Order at 14-17; *Parthenon II* Order at 13-16. As to the phrase "one device at a time," Defendants are, in effect, seeking a negative limitation that bars multiple devices. The inclusion of a negative limitation within a claim construction generally requires support from the intrinsic evidence. *See Santarus, Inc. v. Par Pharms., Inc.*, 694 F.3d 1344, 1351 (Fed. Cir. 2012) ("Negative claim limitations are adequately supported when the specification describes a reason to exclude the relevant limitation."); *Omega Eng'g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1322-23 (Fed. Cir. 2003) (declining to add a negative limitation when there was no "express disclaimer or

independent lexicography in the written description that would justify adding that negative limitation"). As to the intrinsic evidence, Defendants only cite to an embodiment. Defendants do not cite to any disclaimer or disavowal. Even if only a single embodiment exists, the preferred embodiment is not required to be read into the claims. *See Arlington Indus., Inc. v. Bridgeport Fittings, Inc.*, 632 F.3d 1246, 1254 (Fed. Cir. 2011) ("Even where a patent describes only a single embodiment, claims will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using words or expressions of manifest exclusion or restriction.") (internal citations omitted). Moreover, Defendants' construction, in essence, reads the arbiter concept into the "bus" term. However, as described in the patents, the arbiter is a separate structure that has a separate function. '459 Patent Figure 7, 12:49-13:36; '789 Patent Figure 2, 4:4-11, 9:42-57. The fact that the specification discloses a separate arbiter and arbitration function shows that the structure and function are not inherent in the term "bus." As PUMA points out, the claims also confirm that the arbiter function is not inherently part of the claimed bus. Some claims recite the arbiter and arbitration limitaions and some claims do not. *See, e.g.,* '789 Patent Claims 15 and 19. The intrinsic record does not teach that buses that allow multiple devices to access at the same time are excluded from the term "bus."

Most of the parties' briefing and oral argument focuses on whether the extrinsic evidence established that "bus," at the time of the invention, was thought of by those skilled in the art to require a "one device at a time" limitation. On balance, the Court finds that the extrinsic evidence does not support including a negative limitation on the term "bus."

First, the Court notes that Defendants arguments mix concepts that relate to two distinct structures: a single wire and a bus. None of the parties appears to dispute that a single wire a can

transmit information for only one device at a time. However, "bus" contains a collection of wires, not just a single wire.

As for Defendants' reliance upon the expert declaration of Dr. Stone from *Parthenon II*, it is telling that Dr. Stone does not affirmatively state that a bus cannot carry information from more than one device at a time. *See Parthenon II* Dkt. No. 86-1 at 10-16. Defendants acknowledged this issue with Dr. Stone's testimony at the oral hearing. (Oral Hearing Tr. at 15-17.) Indeed, the Court notes that Dr. Stone's testimony was likely directed to a signal line and not to a "bus":

> 36. A wire or "signal line," can carry only one symbol at any one time because a wire is only at one voltage level or carries only one current at any given time.
>
> 37. Because a wire can carry only one symbol at any one time, a "bus" composed of one or more wires can carry only one bus transaction at any one time over the wires. This concept . . . .

Parthenon II Dkt. No. 86-1 at 11. The declaration does not state that any multi-line structure that carries information from more than one device cannot be a "bus."

With respect to Defendants claim that a split-transaction bus still transfers information "one device at a time," it is clear that Defendants acknowledge that a split-transaction bus provides for overlapping transactions. (Dkt. No. 60 at 6-7.) PUMA asserts that in the split-transaction process both devices use the bus at the same time (i.e., two operations are being performed concurrently). Defendants assert that only one device uses the bus at a time because at any particular time only data from one device is on the signal lines. The question reduces to whether "one device at a time" should be construed to mean the usage of the bus in an "operation" timeframe or a particular instance in time on one wire. Defendants' construction creates ambiguity that could be interpreted to exclude split-transaction buses.

As to the Mercury RACEway, the weight of the evidence shows that those skilled in the art called the Mercury RACEway a bus. (Dkt. No. 56 Ex. N at 203 and Ex. M at 31.) Mercury's own statements show that the term "bus" does not always mean "one device at a time" as Mercury referred to certain buses as "a single transaction bus" implying that "bus" itself is not limited to "one device at a time." (*See* Dkt. No. 56 Ex. O at 1.) Defendants' agreed that the Mercury RACEway operated with more than one device at a time and that their construction would exclude the Mercury RACEway. (Dkt. No. 60 at 7.) Balancing the competing extrinsic evidence, the Court finds that the extrinsic evidence does not support the exclusion sought by Defendants.

Finally, the Court notes that at the Oral Hearing, a question arose as to whether Defendants' construction would exclude aspects of the PCI and ISA buses, the buses disclosed as the preferred embodiments in the Asserted Patents. Though not explicitly mentioned in the specification, Defendants acknowledged that clocks transmit clock information on the PCI and ISA buses, while other devices transmit other information at the same time on the bus. (Oral Hearing Tr. at 19.) Thus, Defendants' construction could be interpreted to exclude the buses disclosed in the specification. '789 Patent Figures 3-4, 8:38-62, 9:5-41. A construction that excludes the preferred embodiment "is rarely, if ever, correct." *Accent Packaging, Inc. v. Leggett & Platt, Inc.*, 707 F.3d 1318, 1326 (Fed. Cir. 2013).

The Court construes "bus" to mean "a signal line or a set of associated signal lines to which a number of devices are coupled and over which information may be transferred between them."

2. "memory bus" ('164 Patent claims 1, 6, 7)

PUMA's Construction	Defendants' Construction

No construction necessary. Alternatively: "a signal line or a set of associated signal lines to which a number of devices, including a memory, are coupled and over which information may be transferred"	"bus that connects directly with a memory"

The primary issue in dispute between the parties is whether a memory bus requires a direct connection.

Positions of the Parties

PUMA asserts that a person skilled in the art would understand that a memory bus is a bus that is coupled to a memory. (Dkt. No. 56 at 9.) PUMA asserts that Defendants' use of "connects directly" would read out common buses that include intervening components or interfaces, such as the MBus. PUMA claims that nothing in the specification suggests that the patentee intended to restrict the generic term "memory bus" in such a narrow fashion. (Dkt. No. 78 at 9.)

Defendants incorporate by reference the arguments raised by the defendants in *Parthenon II*. (Dkt. No. 60 at 11-12.) Defendants summarize the *Parthenon II* arguments that they have adopted as follows:

- A construction requiring a "direct connection" between a bus and a memory is supported by the intrinsic record, including the figures in the specification.
- PUMA's proposed construction is overly broad because under it, any bus is a memory bus.

(*Id*. at 12.)

Defendants assert that the parties' fundamental disagreement here is on the degree or relevance of the connection. (*Id*.). Defendants object to the use of "indirectly." Defendants assert

that every device in a computer is either directly or indirectly connected. Defendants assert that PUMA's construction, thus, reads out the term "memory" and destroys the differentiation between "bus" and "memory bus." (*Id*.) Defendants assert that no person of ordinary skill in the art would believe that every bus in a computer system is a memory bus.

Defendants assert that the only objection PUMA has identified with regard to Defendants' construction is that a tri-state buffer would prevent a memory from being "directly" connected to a bus (the MBus approach). (*Id*. at 13.) Defendants assert that a tri-state buffer merely connects or disconnects one device from another. Defendants assert that at times the devices are connected and transmitting, and at other times the devices are disconnected and not transmitting. Defendants assert that this conforms to Dr. Stone's expert testimony:

> [Y]ou have a clock cycle or you have a time, a period, when the drivers to the bus are in tri-state mode. That means they're physical disconnected, there's no electrical connection. Actually, it's through a transistor that's open. Then you connect them to the bus by closing that transistor, closing a switched. So whatever you're driving will be passed to the bus. When it says active high or active low, that means that you're putting a zero or a one on the bus. When you're done driving and you reach the time that you're at the end of that clock period, you go back to tri-state, which means you disconnect the driver from the bus.

(Dkt. No. 56 Ex. Q, at 41-42.) Defendants assert that the tri-state buffer periodically connects the memory to the bus and thus, the buffer does not exclude such arrangements from being "directly" connected. Rather, sometimes the device is connected (and meets the limitation) and sometimes it is not connected (and does not meet the limitation). Defendants assert that "sometimes a limitation would not be met" is not a reasoned objection to a proposed construction. (Dkt. No. 60 at 14.)

In reply, PUMA asserts that Defendants have falsely suggested that PUMA is arguing that every bus in a computer is a "memory bus." PUMA asserts that if a bus is not used to send data to and from the memory, it would logically not be a memory bus. (Dkt. 64 at 4.) PUMA

contends that Defendants' position that an intervening switch or interface renders a bus used to send data to a memory not a "memory bus" is improper. (*Id*.)

Analysis

The dispute regarding "directly" connected raises issues that were previously raised as to the terms "bus" and "coupled." The Court relies on its reasoning for those terms and finds that a "direct" connection is not required. The Court rejects Defendants argument that its proposed construction does not exclude an "MBus"-like bus with switches and interfaces. Defendants' proposed construction suggests that an "MBus"-like bus that "directly" connects to a memory would not be a "memory bus" until it is in-use and transmitting data. However, the nature of a bus structure should not change based on whether the system that contains the bus is active and in-use. Furthermore, even when the bus is active, interfaces and switches will serve as intervening structures through which the bus may be accessed. Therefore, a construction that uses the word "coupled" more properly describes the relationship between the "bus" and the memory because a construction that allows only a "direct" connection could be interpreted as excluding interfaces and switches. As to the general style of the construction, the Court finds that Defendants' approach is clearer.

The Court construes "memory bus" to mean "bus [as construed] that is coupled with memory."

3. "in real time" ('789 Patent claims 1, 13, 15, 28; '315 Patent claim 1 and '164 Patent claims 1, 6)

PUMA's Construction	Defendants' Construction
"fast enough to keep up with an input data stream"	Indefinite

The fundamental dispute between the parties relates to the question of whether certain prosecution history statements limit "real time" to a bus latency concept which would conflict with the specification and render the term indefinite.

Positions of the Parties

PUMA notes that, in *STMicroelectronics*, the Court construed "real time" to mean "processing fast enough to keep up with an input data stream." *STMicroelectronics*, 327 F. Supp. 2d at 693, 710. PUMA asserts that this construction comports with the intrinsic and extrinsic evidence.

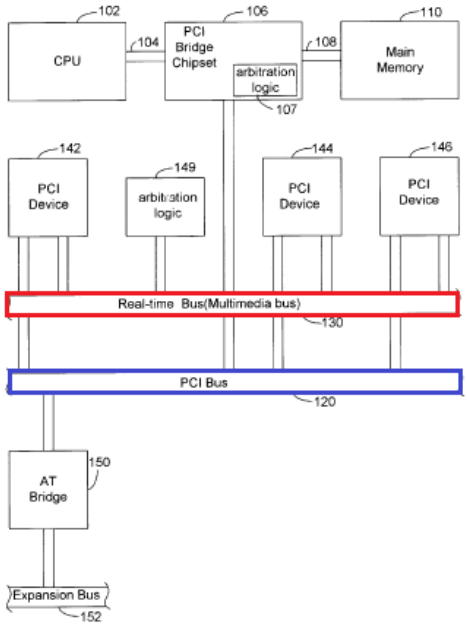
PUMA asserts that the patent specification states that "[i]f the decoder does not operate in real time the decoded movie would stop periodically between images until the decoder can get access to the memory." '789 Patent 3:21-24. Elsewhere, the specification similarly states:

> A goal is to have the decoder/encoder 45 operate in real time without dropping so many frames that it becomes noticeable to the human viewer of the movie. To operate in real time the decoder/encoder 45 should decoder [sic] and/or encode images fast enough so that any delay in decoding and/or encoding cannot be detected by a human viewer. This means that the decoder/encoder 45 has a required bandwidth that allows the decoder/encoder 45 to operate fast enough to decode the entire image in the time between screen refreshes, which is typically 1/30 of a second, with the human viewer not being able to detect any delay in the decoding and/or encoding.

Id. at 6:41-52. PUMA also cites to an IEEE dictionary and to *STMicroelectronics* in which the Court said: "The relevant dictionary definition indicates that real time concerns the processor's ability to 'keep up with' the data input." (Dkt. No. 56 at 10 (quoting *STMicroelectronics*, 327 F. Supp. 2d at 693).)

PUMA asserts that Defendants' proposed construction should be rejected for the reasons that PUMA argued in *Parthenon I* and *Parthenon II* which is that Defendants have misread the prosecution history. PUMA asserts that in the prosecution, PUMA did not distinguish Gulick on

the basis of using a PCI bus and did not distinguish Gulick by narrowing the ordinary meaning of "real time." Rather, PUMA asserts that the Applicants distinguished Gulick on the basis that its PCI bus was insufficient for real time performance. (Dkt. No. 56 at 10-11 (citing Dkt. No. 56 Ex. J (Mangione-Smith Decl.) at ¶25-27).) PUMA emphasizes that Figure 1 of Gulick shows that the Gulick PCI bus was used in addition to a "real time" bus. PUMA asserts that Gulick represents that its PCI bus was not sufficient to guarantee real time performance. (*Id.* at 11.) PUMA points to Figure 1 of Gulick as illustrative:



(Dkt. No. 56 at 11 (color coding added).) PUMA notes that Gulick included a real time bus 130 and a PCI bus 120. PUMA asserts that Gulick itself represented that its PCI bus was insufficient to guarantee real time performance. PUMA contends that it was the Gulick reference which raised the issue of latency in the context of the specific system of Gulick. PUMA asserts that the Applicants did not generally characterize "PCI bus" in the prosecution but characterized its specific use in Gulick. (*Id.* at 11-12.) PUMA asserts the representation in Gulick that its PCI bus was not a real time bus did not have anything to do with the parameters of PCI buses in general.

Rather, PUMA contends that the representation shows that in the specific context of Gulick the PCI bus was not a real time bus. (*Id*. at 12.)

Defendants incorporate by reference the arguments of the defendants from *Parthenon II*. (Dkt. No. 60 at 14.) Defendants explicitly do not, however, adopt the alternative construction proposed by the defendants in *Parthenon II*. (*Id*.) Defendants summarize the *Parthenon II* arguments that it adopted as follows:

- The intrinsic evidence is inconsistent as to the meaning of "real time."
- The specification indicates that the PCI bus is a real time bus.
- The prosecution history distinguishes the invention over the PCI bus when cited in a rejection, because the PCI bus is not a real time.
- The patent's notice function is not served, because a person of ordinary skill in the art, reading the specification and claims, receives conflicting information and has no way to know whether a PCI bus does or does not meet the "real time" limitation in the claims.

(*Id*.)

In reply, PUMA asserts that Defendants' arguments should be rejected for the same reasons that PUMA articulated in *Parthenon II*. PUMA asserts that the *Parthenon II* defendants main complaint focused on the impact of latency. (Dkt. No. 64 at 5.) PUMA asserts that "fast enough to keep up with an input data stream" already subsumes concepts like bandwidth, latency, and any other issue that would negatively impact the amount of data that can be transmitted. (*Id*.) PUMA also asserts that the *Parthenon II* defendants misread the prosecution history. PUMA asserts that the patentees did not distinguish Gulick by narrowing the ordinary meaning of "real time." Rather, PUMA asserts that Gulick was distinguished on the grounds that the PCI bus—as used in the specific context of Gulick—was insufficient for real time

performance. (*Id*. at 5-6 (noting Figure 1 of Gulick includes both a PCI bus and real time bus).) The parties did not provide additional argument at the oral hearing.

Analysis

The issues and arguments presented to the Court for "real time" are the same as presented by the parties in *Parthenon II* for this term. *Parthenon II* Order at 18-25. The Court's analysis in *Parthenon II* is applicable here and provides the basis for the Court's construction. *Id*.

The Court construes "real time" to mean "fast enough to keep up with an input data stream."

4. "fast bus" ('368 Patent claim 7 and '045 Patent claim 4)

PUMA's Construction	Defendants' Construction
"bus with a bandwidth equal to or greater than the required bandwidth to operate in real time"	"bus with a bandwidth greater than the bandwidth required for the decoder to operate in real time"

The parties dispute whether the bandwidth is limited to "greater than" or includes "bandwidth equal to or greater than."

Positions of the Parties

PUMA asserts that two passages in the specification are definitional: "a fast bus 70 is any bus whose bandwidth is equal to or greater than the required bandwidth" ('459 Patent 8:1-2) and "two devices are coupled to the memory through a fast bus having a bandwidth of at least the minimum bandwidth needed for the video and/or audio decompression and/or compression device to operate in real time" ('459 Patent 4:59-62.) PUMA asserts that Defendants' construction is similar to PUMA's but eliminates the "equal to" language from the patentee's definition. (Dkt. No. 56 at 13.) PUMA asserts that if a fast bus has "at least the minimum

bandwidth" then, as a matter of logic, it has a bandwidth equal to or greater than the requirement. (*Id*.)

Defendants incorporate by reference the arguments of the defendants from *Parthenon I*. (Dkt. No. 60 at 15.) The parties did not provide additional argument at the oral hearing.

Analysis

The issues and arguments presented to the Court for "fast bus" are the same as presented by the parties in *Parthenon I* for this term. *Parthenon I* Order at 23-24. The Court's analysis in *Parthenon I* is applicable here and provides the basis for the Court's construction. *Id*.

The Court construes "fast bus" to mean "bus with a bandwidth equal to or greater than the bandwidth required to operate in real time."

5. "arbiter" / "arbitration circuit" / "memory arbiter" / "arbiter circuit" ('789 Patent claims 1, 19; '459 Patent claims 1-3, 7, 9, 11, 13; '194 Patent claims 1-3, 7, 9, 11, 16-18, 22, 23; '368 Patent claims 1, 5, 7, 13, 17, 19, 20, 23; '045 Patent claims 1, 4, 5, 12, 15; '753 Patent claims 1, 4, 7-10, 12; and '164 Patent claims 1, 8, 12)

PUMA's Construction	Defendants' Construction
"circuitry that uses a priority scheme to determine which requesting device will gain access"	"circuitry that uses a priority scheme to determine which requesting device will gain direct access"

The sole difference between the parties' construction is Defendants' inclusion of "direct" in their construction.

Positions of the Parties

PUMA notes that the agreed construction in *STMicroelectronics* conforms to PUMA's construction. *STMicroelectronics*, 327 F. Supp. 2d at 710. PUMA asserts that Defendants' construction relies on the prosecution history for the '459 Patent. PUMA notes that in the prosecution of the '459 Patent, the patentees amended the claims to add language concerning

"direct access." PUMA states that the amendment, for example, made the following changes: "an arbiter coupled to the decoder, the arbiter configured to determine which of at least the first device and the decoder receives direct access [for selectively providing access for the first device and the decoder] to the first memory . . . ." (Dkt. No. 56 Ex. S at 2) (underlined and bracketed language in original). PUMA asserts that the patentee did not redefine "arbiter" but rather added other surrounding language to traverse the prior art. (Dkt. No. 56 at 19.) PUMA asserts that the Applicants traversed the prior art by describing a specific configuration of the arbiter. (*Id*. at 19.) PUMA further notes that the claims at issue were never allowed and were subsequently cancelled and replaced with other claims. PUMA asserts that such claims did not use "direct access" but used "without also requiring a second bus." (*Id*.) PUMA asserts that Defendants, thus, seek to import a limitation into the claims that would improperly change the scope of the issued claims.

Defendants incorporate by reference the arguments of the defendants from *Parthenon II*. (Dkt. No. 60 at 19.) Defendants assert that eliminating the "direct" requirement broadens the meaning of "arbiter" beyond the specification. Defendants assert that a device is not an arbiter with respect to two devices and a bus, if the data may traverse several other buses. (*Id*.) Defendants claim that, without the use of "direct," the term "arbiter" is not being used in a meaning that one skilled in the art would use the term.

PUMA claims that Defendants' are arguing that a circuit is not an "arbiter" if the data controlled by the arbiter must traverse several other buses. PUMA argues that this is not mentioned in the intrinsic record. (Dkt. No. 64 at 9.) The parties did not provide additional argument at the oral hearing.

Analysis

The issues and arguments presented to the Court for the arbiter terms are the same as those presented by the parties in *Parthenon II*. *Parthenon II* Order at 26-29. The Court's analysis in *Parthenon II* applies. Furthermore, as to Defendants' argument that an arbiter must be limited to a single bus, the Court notes that Defendants' proposed construction does not include this limitation. Defendants also do not point to support in the intrinsic record that warrants including this negative limitation.

The Court construes "arbiter" / "arbitration circuit" / "memory arbiter" / "arbiter circuit" to mean "circuitry that uses a priority scheme to determine which requesting device will gain access."

6. "control circuit" ('464 Patent claims 1, 2, 7-13, 16-24, 32)

PUMA's Construction	Defendants' Construction
No construction necessary.	"an electronic control device that is separate from the CPU or processor and that interacts with the operating system"

The primary issue raised in the briefing is whether the "control circuitry" must be separate from the processor/device.

Positions of the Parties

PUMA asserts that the term is effectively defined by the surrounding claim language. PUMA points to claim 1 of the '464 Patent which specifies that the "control circuit" is coupled to the decoding circuit, the processor, and the main memory. Furthermore, PUMA notes that the claim states that the "control circuit" is configured to "request continuous use of several portions of the main memory from the operating system" and "translate the noncontiguous addresses to contiguous addresses of a block memory." '464 Patent claim 1.

PUMA objects to Defendants' construction for multiple reasons. First, PUMA asserts that Defendants' insertion of "device" in place of "circuit" provides no additional guidance. (Dkt. No. 56 at 20.) Second, PUMA objects to Defendants' requirement that the "control circuit" be "separate." PUMA asserts that the specification does not define what "separate" means. PUMA also asserts that Defendants require the control circuit to be "separate" from "the CPU." PUMA argues, however, that "CPU" is not used in the claims that include "control circuit." PUMA contends that the addition of "CPU" would, thus, cause confusion. (*Id*.) PUMA contends that the specification states that multiple components "can be monolithically integrated as a single chip." '464 Patent 5:10-13. PUMA asserts that the claim merely requires the control circuit to be "coupled" to the processor, which can be the case even if the components are monolithically integrated as a single chip. (Dkt. No. 64 at 9.) Furthermore, PUMA asserts that Defendants' construction ignores the fact that the surrounding claim language provides guidance as to the meaning and scope of the term. (*Id*.)

Defendants incorporate by reference the arguments of the defendants from *Parthenon II*. (Dkt. No. 60 at 20.) The parties did not provide additional argument at the oral hearing.

Analysis

The issues and arguments presented to the Court for "control circuit" are the same as presented by in *Parthenon I* and *Parthenon II*. *Parthenon I* Order at 41-44; *Parthenon II* Order at 29-33. The Court's analysis in *Parthenon I* applies. For the reasons described in the *Parthenon I* Order, the Court rejects Defendants' proposition that the control circuit must be a separate device. *Parthenon I* Order at 44-45.

The Court finds that "control circuit" has its plain and ordinary meaning and no further construction is necessary.

7. "directly supplied" ('194 Patent claim 15; '368 Patent claim 3) and "directly supplies" ('368 Patent claims 2, 14, 21; '045 Patent claims 2, 6, 13; '753 Patent claim 3)[3]

PUMA's Construction	Defendants' Construction
a. "supplied without being stored in main memory for purposes of decoding subsequent images"	a. "supplied without intervening components"
b. "supplies without being stored in main memory for purposes of decoding subsequent images"	b. "supplies without intervening components"

The dispute between the parties relates to whether the term "directly supplied" describes the physical connection of the components or the decoding method by which some frames are not sent to the main memory for subsequent use in decoding other frames.

Positions of the Parties

PUMA asserts that "directly supplied" concerns the system's use of decompressed frames in the context of video coding. PUMA states that the phrase describes the fact that certain types

[3] The parties included '194 Patent claim 2 in the Patent Rule 4-5(d) Joint Claim Construction Chart. (Dkt. No. 65-2 at 3.) However, the terms at issue are not found in that claim.

of frames do not need to be transferred to main memory for use in the subsequent decoding of other frames.

PUMA asserts that Defendants seek to improperly restrict the term to a description of a structural arrangement that includes no intervening components. PUMA asserts, however, that the term is not intended to be a limitation on the physical architecture or to exclude the use of intervening components. PUMA asserts that Defendants' construction would exclude disclosed embodiments which include intervening components. Specifically, PUMA points to Figure 3 of the '194 Patent:

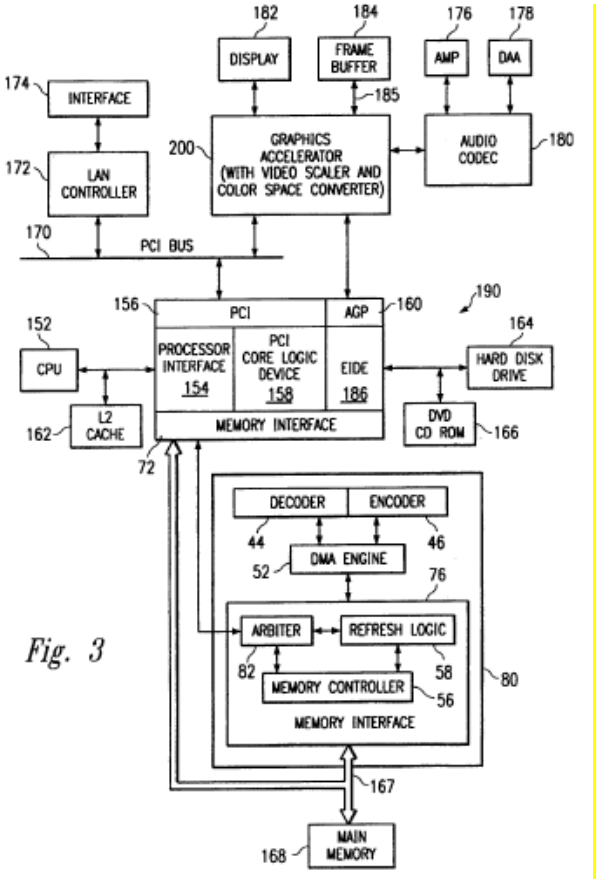


Fig. 3

'194 Patent Figure 3. PUMA asserts that in Figure 3, the decoder/encoder 80 is connected to the graphics accelerator 200 and the display 182 through the core logic chipset 190. PUMA asserts that Defendants' construction would not encompass this embodiment due to the intervening core

logic chipset 190 and the use of multiple buses. (Dkt. No. 56 at 16-17.) PUMA contends that any frames supplied from the decoder/encoder 80 to the display 182 would necessarily pass through the intervening core logic chipset 190. PUMA states that Defendants' added phrase "without intervening components" is directly at odds with the specification.

PUMA contends that the patents do not use the term "directly supplied" to mandate that there be no intervening components. PUMA asserts that the phrase "directly supplied" reflects the fact that certain types of frames do not need to be transferred to main memory for use in the subsequent decoding of other frames. (*Id*. at 17.) PUMA points to claim 14 of the '194 Patent as illustrative. The Claim states that the "decoder directly supplies a display adapter of the display device with an image for use other than decoding a subsequent image." PUMA also notes that claim 15 of the '194 Patent states: "the images directly supplied to the display adapter being bidirectional images obtained from two preceding intra and predicted images." Thus, PUMA asserts that the term "directly supplied" must be viewed in context of MPEG bidirectional decoding of video frames.

PUMA notes that the specification states "[t]he intra and predicted images are likely to be used to reconstruct subsequent predicted and bidirectional images, while bidirectional images are not used again." '194 Patent 3:21-25. PUMA asserts that the specification, thus, notes that "a buffer associated with bidirectional images is not required, these bidirectional images B being directly supplied to display adapter 120 as they are being decoded." '194 Patent 10:39-42. PUMA asserts that these passages show that "directly supplied" must be viewed in the context of bidirectional frames, which do not need to be stored in main memory for purposes of decoding. (Dkt. No. 56 at 18.)

Defendants incorporate by reference the arguments of the defendants from *Parthenon II*. (Dkt. No. 60 at 18.) The parties did not provide additional argument at the oral hearing.

Analysis

The issues and arguments presented to the Court for "directly supplied/supplies" are the same as those presented by the parties in *Parthenon II*. *Parthenon II* Order at 33-40. The Court's analysis in *Parthenon II* applies.

The Court construes "directly supplied" to mean "supplied without being stored in main memory for purposes of decoding subsequent images" and "directly supplies" to mean "supplies without being stored in main memory for purposes of decoding subsequent images." [4]

8. "monolithically integrated into" / "integrated into" ('789 Patent claims 6, 21, 23; '194 Patent claim 19; '368 Patent claims 17, 23; '045 Patent claims 9, 15; '753 Patent claim 12; and '164 Patent claim 12); "monolithically integrated with" / "integrated with" ('459 Patent claims 2, 3; '194 Patent claims 2, 3; '164 Patent claim 8)

PUMA's Construction	Defendants' Construction
"formed on a single semiconductor chip with"	"formed within"

The parties dispute whether the terms require a first component to be formed within a second component or merely formed with the second component on the same semiconductor chip.

Positions of the Parties

PUMA asserts that the concept of monolithic integration is well understood by a person of skill in the art. PUMA asserts that the term "monolithic" originates from the Greek words

[4] With regard to claims that do not recite "main memory," the term "main memory" is replaced to conform to the usage in each particular claim. Thus, "main memory" is replaced with "the memory" for '194 Patent claim 15, '368 Patent claim 21 and '045 Patent claim 13. "Main memory" is replaced with "system memory" for '368 Patent claim 14 and '045 Patent claim 6.

monos ‘single’ and *lithos* ‘stone.’ (Dkt. No. 56 at 21.) PUMA cites to a number of extrinsic evidence dictionaries which indicate that “monolithic” relates to forming structures in a single semiconductor integrated circuit. (*Id*.) PUMA argues that Defendants’ construction is ambiguous. For example, PUMA asserts that two components can be monolithically integrated into the same semiconductor integrated chip without one component being “formed within” the physical footprint of the other. PUMA asserts that the purpose of monolithic integration is to reduce costs and promote efficient use of space. PUMA asserts that Defendants’ construction ignores these fundamental purposes and would unnecessarily require the overlapping of physical layouts. (*Id*. at 22.)

PUMA asserts that there are two terms “integrated into” and “integrated with.” PUMA asserts that its construction is proper, at a minimum, for “integrated with.” (*Id*.) PUMA asserts that device A “integrated with” device B does not require device A to be “within” device B or vice-versa. (*Id*. at 22-23.)

Defendants incorporate by reference the arguments of the defendants from *Parthenon II*. (Dkt. No. 60 at 20.) Defendants further assert that to the extent PUMA draws a distinction between the terms using “into” and “with,” Defendants assert that such distinction is without merit and that Defendants’ arguments apply equally to “integrated into” and “integrated with.”

In reply, PUMA notes that although Defendants adopt the *Parthenon II* defendants’ positions, Defendants do not differentiate between claims using “with” and “into.” PUMA notes that the *Parthenon II* defendants made such a distinction because they stated that the claims “explicitly differentiate between integrating components **with** the decoder/encoder, and integrating components **into** the decoder/encoder.” (Dkt. No. 64 at 10 (quoting *Parthenon II* Dkt. No. 86 at 31 (emphasis in original)).) PUMA asserts that, at a minimum, PUMA’s construction is

proper for the terms "monolithically integrated with" and "integrated with." (*Id*.) The parties did not provide additional argument at the oral hearing.

Analysis

PUMA's arguments go to the meaning of "monolithically integrated" or "integrated" in general. However, "[w]hile not an absolute rule, all claim terms are presumed to having meaning in a claim." *Innova/Pure Water v. Safari Water Filtration*, 381 F.3d 1111, 1119 (Fed. Cir. 2004). The terms "monolithically integrated into" and "integrated into" describe not just any integration but describe integrated "into." The parties do not appear to debate that PUMA's construction would conform to what a person skilled in the art would understand to be "monolithically integrated" or "integrated." However, the Court should give meaning to integrated "into."

The distinction between claim 8 and claim 12 of the '164 Patent is illustrative. Claim 8 of the '164 Patent states that "the arbiter and second memory interface are **integrated with** the decoder/encoder" while claim 12 states "the refresh logic, the arbiter, and the second memory interface are monolithically **integrated into** the decoder/encoder" (emphasis added). "Integrated with" carries a broader and more general meaning than "integrated into." Two devices formed "with" each other can be, for example, just formed on the same chip. However, when one device is "integrated into" a second device, the "into" language should be given effect. PUMA's construction fails to give meaning to "into." PUMA's construction also fails to provide context for the differing claims, some which require more than mere integration on the same chip, but require integration of one structure "into" another.

For example, some claims state that the "decoder and arbiter circuit are integrated into a single chip." '368 Patent Claim 17. Thus, for those claims, the decoder and arbiter circuit are formed in the single chip. Similarly, the claims which state that the "decoder is monolithically

integrated into the first device" require the decoder to be formed in the first device. '194 Patent Claim 19. The same principle applies to the claims which recite that "the refresh logic, the arbiter and the second memory interface are monolithically integrated into the decoder/encoder." '164 Patent Claim 12.

As noted, for the claims that utilize "integrated with." The plain meaning of those claims do not require forming one structure into or within another. Rather, the claims just require the two structures to be formed with each other. As the parties do not dispute the meaning of "monolithically," construction of the "integrated into" and "integrated with" will resolve the parties' dispute.

T**he Court construes "integrated into" to mean "formed within on a single semiconductor chip." The Court construes "integrated with" to mean "formed on a single semiconductor chip."**

9. Coupled Terms

"coupled" ('789 Patent claims 1, 5, 15; '464 Patent claims 1, 8, 10, 12, 13, 17, 19, 20, 21, 23, 33, 34, 35; '368 Patent claims 1, 7, 13, 19, 20; '045 Patent claims 1, 4, 5, 12; '753 Patent claims 1, 7; '315 Patent claims 1, 14, 15 and '164 Patent claims 1, 8, 9, 11)

"coupleable" ('045 Patent claims 1, 4, 12; '753 Patent claim 7; '315 Patent claim 1 and '164 Patent claim 1)

"coupling" ('789 Patent claim 1 and '194 Patent claims 1, 16, 17)

PUMA's Construction	Defendants' Construction
a. "directly or indirectly connected" b. "directly or indirectly connectable" c. "directly or indirectly connecting"	"attached, resulting in an arrangement that includes no more than one bus" Alternatively: Indefinite

Positions of the Parties

PUMA cites three Eastern District of Texas cases which have construed "coupled" to mean directly or indirectly connected. (Dkt. No. 56 at 13.) PUMA also asserts that the specification utilizes "coupled" to reference elements that are indirectly connected. For example, PUMA cites to Figure 1b of the '789 Patent which shows a memory interface 18 that connects to an audio decoding circuit 14 with the audio decoding circuit 14 in turn connected to a memory 22. PUMA notes that the specification states that the "memory interface 18 is coupled to memory 22." '789 Patent 2:25. Similarly, PUMA points to Figure 2 of the '789 Patent which shows a decoder/encoder 45 connected to a memory interface 48 with the memory interface 48 in turn, connected to memory 50. PUMA notes that the specification states that the "decoder/encoder 45 is coupled to the memory 50 through devices, typically a bus 70." *Id*. 6:29-30. PUMA notes that the '459 Patent has similar passages. (Dkt. No. 56 at 15 (citing '459 Patent 2:28, 7:39-42).) PUMA further notes that the patents use "coupled" to refer to direct connections such as in Figure 2 of the '789 Patent: "DMA engine 60 of the first device is coupled to the arbiter 54 of the memory interface 48." '789 Patent 6:15-17.

Defendants previously stated that there should be "no construction" as to this term. (Dkt. No. 56 at 13.) Defendants now assert that it should be construed as "attached, resulting in an arrangement that includes no more than one bus." Defendants incorporate by reference and adopt the arguments and evidence presented by the defendants in *Parthenon I*. (Dkt. No. 60 at 15 (citing *Parthenon I* Dkt. No. 121 at 15-23).)

Defendants, despite advancing this new construction, continue to assert that the term should require no construction. (Dkt. No. 60 at 16.) Defendants argue that because a person of skill in the art would understand that if "coupled" were to have any limiting effect the term must

indicate the quality or relevance of the connection between the things that are coupled. (*Id*. at 16.) Defendants assert that without some "relevance" in the connection, absurd results are obtained.

Defendants point to Figure 4 of the '789 Patent as an example that illustrates "coupled:"

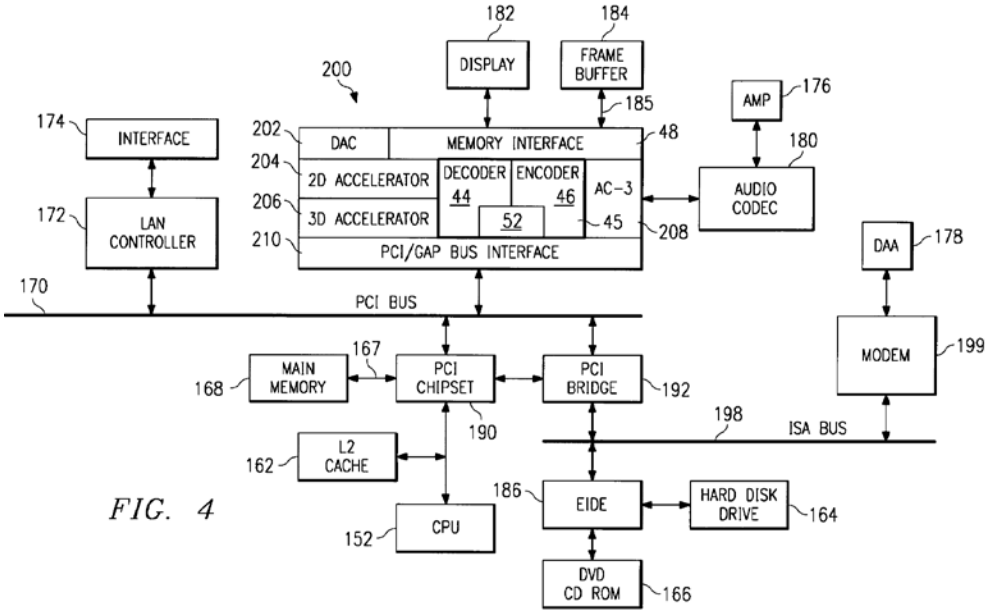


FIG. 4

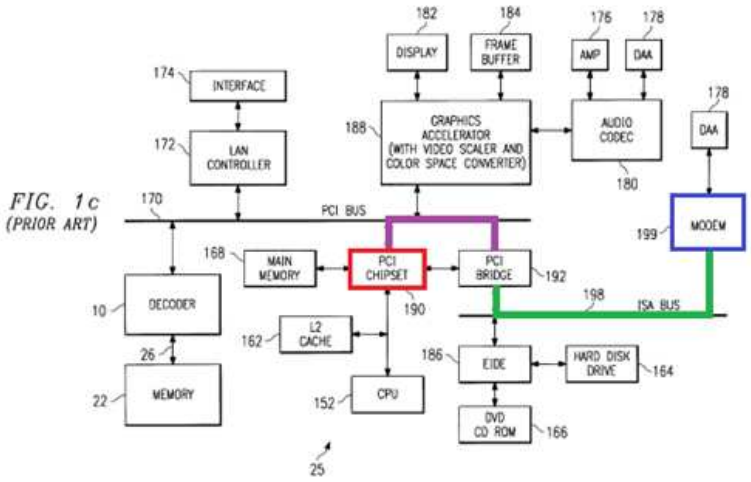
Defendants assert that the figure clearly shows that the Hard Disk Drive 164 is coupled to the EIDE 186 and the EIDE 186 is coupled to the ISA Bus 198. Defendants assert that an engineer might casually say that the Hard Disk Drive 164 is "coupled" to the ISA Bus 198, but would understand that the Hard Disk Drive is "connected to the EIDE 186 and through that to the ISA Bus 198." (Dkt. No. 60 at 17.) Defendants assert that, thus, "coupled" is not precise and not useful to one in the art.

Defendants claim that it is inconceivable that an engineer would ever state that "the LAN controller 172 is coupled to the ISA Bus 198." (*Id*.) Defendants assert that such language would be worse than inaccurate and would actively mislead because no engineer would find that statement to mean that the "LAN Controller 172 is connected to the PCI Bus 170, and through

that to the PCI Bridge 192, and through that to the ISA Bus 198." (*Id*.)

Defendants contend that in engineering, a term with such a low level of precision would not be used at all. (*Id*. at 18.) Defendants assert it would be more accurate to say that the LAN Controller 172 and the Modem 199 are "in the box with the other parts" than it would be to say they are "coupled to the PCI Bus." (*Id*.) Defendants assert that the use of the term is analogous to stating that the hard drive of one's home computer is "coupled" to the hard drive of a neighbor's computer. (*Id*.) Defendants assert that if the Court adopts PUMA's constructions the terms are indefinite under *Nautilus*. (*Id*.) At the oral hearing, Defendants emphasized that when the specifications use "coupled," the term is used in the context of devices that are coupled through, at most, one bus.

In reply, PUMA asserts that Defendants' new construction directly conflicts with the examples and figures of the asserted patents. PUMA points to Figure 1c of the '789 Patent which is described as "Fig. 1c shows a computer 25 containing a decoder 10, a main memory 168 and other typical components such as a modem 199, and graphics accelerator 188. The decoder 10 and the rest of the components are coupled to the core logic chipset 190 through a bus 170." '789 Patent 2:49-53. PUMA asserts that the figure shows that the modem 199 is "coupled" to the core logic chipset 190 through ISA bus 198 and PCI bus 170, resulting in an arrangement that includes two buses. (Dkt. No. 64 at 7.) Figure 1c is replicated below.



’789 Patent Figure 1c (color coding added). As to Defendants’ indefiniteness argument, PUMA states that Defendants have not provided any support. PUMA asserts that this term is commonly used by those skilled in the art and that Defendants have not shown that it would not be understood with “reasonably certainty.” (Dkt. No. 64 at 7, n. 2.)

Analysis

Defendants re-assert the positions taken by the defendants in *Parthenon I.* In addition, they argue that “coupled” inherently does not have precision and does not have meaning to one skilled in the art. The specifications, however, use the term repeatedly, and suggest that the term allows for both direct and indirect connections. Furthermore, Defendants’ construction uses “attached” but does not explain if “attached” includes direct attachment or indirect attachment. However, Defendants’ incorporation by reference of the *Parthenon I* arguments (where “directly connected” was utilized), implies that Defendants assert that “attached” means “directly connected.” For the reasons stated in *Parthenon I*, Defendants position is rejected. *Parthenon I* Order at 30-34.

Defendants do not contest that the well-known meaning of “coupled” includes devices that are both directly and indirectly connected. In fact, Defendants explicitly admit that those in

the art refer to "coupled" in the context of indirect connections. (Dkt. No. 60 at 17.) Defendants argue that the well-known meaning of "coupled" does not apply because all the disclosed embodiments show connections with only one bus. However, even if the specification discloses embodiments with only one bus, incorporating that limitation into the Court's construction is not mandated. *See Arlington Indus., Inc. v. Bridgeport Fittings, Inc.*, 632 F.3d 1246, 1254 (Fed. Cir. 2011) ("[E]ven where a patent describes only a single embodiment claims will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using words of expressions of manifest exclusion or restriction" (citation omitted)). Moreover, Defendants' attempt to include a negative limitation must be supported by the intrinsic record. *See Santarus, Inc. v. Par Pharms., Inc.*, 694 F.3d 1344, 1351 (Fed. Cir. 2012). Defendants' have not adequately pointed to intrinsic evidence that shows that the Court should include a negative limitation.

Indeed, the Applicants repeatedly use the term "coupled" in a manner consistent with its well-known meaning. For example, in the '789 Patent, the memory interface 18 of Figure 1b is described as "coupled" to memory 22. Yet, the path between the memory interface and the memory includes at least the audio decoding circuit and a bus between the audio decoding circuit and the memory. '789 Patent 2:25, Figure 1b.

Likewise, in the '789 Patent Figure 2, the decoder/encoder 45 is "coupled" to the memory 50 despite multiple intervening "devices" such as the memory interface 48 and bus 70. *Id*. Figure 2, 6:29-32. Similarly, the '789 Patent describes the modem 199 as "coupled" to the core logic chipset 190, despite the two components being linked through two buses: the ISA bus and the PCI bus. '789 Patent Figure 1c, 2:49-53. Although, at the oral hearing, the parties disputed the proper interpretation of '789 Patent Figure 1c, the Court finds that the specification directly

supports PUMA's interpretation. *See* '789 Patent Figure 1c, Figure 4, 2:49-53, 9:33-34.

Finally, the Court notes that the '368 Patent describes an alternative embodiment for Figure 7 in which peripherals such as the modem 199, disk drive 164 and DVD CD-ROM 166 are "coupled directly" to the PCI chipset. '368 Patent at 12:65-13:5, Figure 7. "Direct coupling" is achieved by incorporating the EIDE interface 186 into the PCI chipset 190 and eliminating the PCI bridge 192 and ISA bus 198. *Id.* This passage implies that absent the modifier "directly," the word "coupled" has a broader meaning than the phrase "directly coupled." Defendants asserted that PUMA's construction, which lacks a degree or relevance of the coupling, would provide no limits to coupling. Defendants thus assert that PUMA's construction effectively allows for all the devices shown in all the figures to be "coupled." The Court rejects Defendants' assertions. The evidence submitted does not indicate that an interpretation by one skilled in the art would reach this conclusion.

Although not explicitly briefed or argued at the oral hearing, Defendants incorporated by reference the file history arguments presented in *Parthenon I*. As the Court noted in prior Orders, these arguments do not support incorporating a negative limitation in the Court's construction. *Parthenon I* Order at 30-34. In fact, some of these file history arguments emphasize that "coupling" is not limited to one bus.

As to the arguments directed at the '459 Patent and '194 Patent prosecution history, the Applicants discussed "direct access" in the '459 Patent prosecution because they added "direct" access and "without also requiring a second bus" limitations to some claims. (*Parthenon I* Dkt. No. 121 Ex. 5 at PUMA 0756, 0762-64); '459 Patent claim 1. The fact that a claim explicitly requires "without also requiring a second bus" shows that the Applicants included the limitations when they were necessary. With regard to the Applicants' use of "directly coupled" in the '368

patent's prosecution history, the cited response indicates that the Applicants used the phrase to describe the arbiter's ability to directly control access to memory by the decoder and other devices. (*Parthenon I* Dkt. No. 121 Ex. 14 at 01256.) It is accurate to state that the Applicants describe the devices in an embodiment of the figures as "directly coupled" to the fast bus. But the Court finds that this statement does not create a global disclaimer to the well-known meaning of "coupled." Rather, the Court finds that it is an example of the Applicants describing a particular embodiment of the figure to the Examiner. Moreover, the example is not limiting because the Applicants' use of "direct" coupling again implies that "coupled" means more than "directly" coupling. *See Phillips*, 415 F.3d at 1314 ("[T]he claim term in this case refers to 'steel baffles,' which strongly implies that the term 'baffles' does not inherently mean objects made of steel.").

In the context of the overall intrinsic record, including the specifications and various file history statements, a clear disclaimer of the term "coupled" was not made.

The court construes "coupled" to mean "directly or indirectly connected," "coupleable" to mean "directly or indirectly connectable," and "coupling" to mean "directly or indirectly connecting."

CONCLUSION

The Court adopts the reasoning and constructions above. The parties should ensure that all testimony that relates to a term addressed in this Order is constrained by both the Court's reasoning and its constructions. In the presence of the jury, however, the parties should not expressly or implicitly refer to each other's claim construction positions and should not expressly refer to any portion of this Order that is not an actual construction adopted by the Court. The references to the claim construction process should be limited to informing the jury

of the constructions adopted by the Court.

IT IS SO ORDERED.

SIGNED this 25th day of January, 2016.

ROY S. PAYNE
UNITED STATES MAGISTRATE JUDGE