UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

PARTHENON UNIFIED MEMORY ARCHITECTURE LLC,	§	
Plaintiff,	§	
v.	§	Case No. 2:15-cv-00621-JRG-RSP
APPLE INC.,	§	
Defendant.	§	

MEMORANDUM OPINION AND ORDER

On April 19, 2016, the Court held a hearing to determine the proper construction of the disputed terms in five Asserted Patents. The Court has considered the briefs and arguments. (Dkt. Nos. 106, 110, and 111.) Based on the intrinsic and extrinsic evidence, the Court construes the disputed terms in this Memorandum Opinion and Order. *See Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005); *Teva Pharm. USA, Inc. v. Sandoz, Inc.*, 135 S. Ct. 831 (2015).

BACKGROUND AND THE ASSERTED PATENTS

Parthenon Unified Memory Architecture LLC ("PUMA") brought this action against Apple Inc. ("Apple") alleging that Apple infringes U.S. Patent Nos. 5,812,789 ("the '789 Patent"), 7,321,368 ("the '368 Patent"), 7,542,045 ("the '045 Patent"), 7,777,753 ("the '753 Patent"), and 5,960,464 ("the '464 Patent") (collectively, "the Asserted Patents"). The '789 and another patent, U.S. Patent No. 6,058,459 ("the '459 Patent"), were filed on the same day, have similar specifications, and incorporate each other by reference. A number of patents resulted from continuation applications of the '459 Patent, including the'368 Patent, the '045 Patent, and

the ’753 Patent.[1] All five Asserted Patents were subject to claim construction orders issued by this Court in (1) *Parthenon Unified Memory Architecture, LLC v. HTC Corp.*, 2:14-cv-0690-JRG-RSP, Dkt. No. 155 (E.D. Tex. July 30, 2015) (the “*Parthenon I* Order”), (2) *Parthenon Unified Memory Architecture, LLC v. Samsung Elecs. Co., Ltd.*, 2:14-cv-902-JRG-RSP, Dkt. No. 155 (E.D. Tex. Jan. 24, 2016) (the “*Parthenon II* Order”), and (3) *Parthenon Unified Memory Architecture, LLC v. ZTE Corp.*, 2:15-cv-0225-JRG-RSP, Dkt. No. 80 (E.D. Tex. Jan. 25, 2016) (the “*Parthenon III* Order”) Furthermore, one additional Eastern District of Texas claim construction order involved the ’789 Patent. *STMicroelectronics, Inc. v. Motorola, Inc.*, 327 F. Supp. 2d 687 (E.D. Tex. 2004).

In general, the ’789 Patent, the ’368 Patent, the ’045 Patent, and the ’753 Patent relate to systems in which a first device (for example a processor) and a decoder/encoder share a common memory. The ’789 Patent abstract recites:

> An electronic system that contains a first device that requires a memory interface and video and/or audio decompression and/or compression device that shares a memory interface and memory with the first device while still permitting the video and/or audio decompression and/or compression device to operate in real time is disclosed.

’789 Patent Abstract. The ’368 Patent abstract recites:

> An electronic system, an integrated circuit and a method for display are disclosed. The electronic system contains a first device, a memory and a video/audio compression/decompression device such as a decoder/encoder. The electronic system is configured to allow the first device and the video/audio compression/decompression device to share the memory. The electronic system may be included in a computer in which case the memory is a main memory. Memory access is accomplished by one or more memory interfaces, direct coupling of the memory to a bus, or direct coupling of the first device and decoder/encoder to a bus. An arbiter selectively provides access for the first device and/or the decoder/encoder to the memory. The arbiter may be monolithically integrated into a memory interface. The decoder may be a video

[1] The specification of the ’464 Patent is not shared by the other Asserted Patents.

> decoder configured to comply with the MPEG-2 standard. The memory may store predicted images obtained from a preceding image.

'368 Patent Abstract.

The '464 Patent relates, generally, to a system whereby a decoder, which requires contiguous blocks of memory, can utilize noncontiguous blocks of the system's memory. The '464 patent abstract recites:

> A method and apparatus employing a memory management system that can be used with applications requiring a large contiguous block of memory, such as video decompression techniques (e.g., MPEG 2 decoding). The system operates with a computer and the computer's operating system to request and employ approximately 500 4-kilobyte pages in two or more noncontiguous blocks of the main memory to construct a contiguous 2-megabyte block of memory. The system can employ, on a single chip, a direct memory access engine, a microcontroller, a small block of optional memory, and a video decoder circuit. The microcontroller retains the blocks of multiple pages of the main memory, and the page descriptors of these blocks, so as to lock down these blocks of memory and prohibit the operating system or other applications from using them. The microcontroller requests the page descriptors for each of the blocks, and programs a lookup table or memory mapping system in the on-chip memory to form a contiguous block of memory. As a result, the video decoder circuit can perform operations on a 2-megabyte contiguous block of memory, where the microcontroller employs the lookup table to translate each 2-megabyte contiguous address requested by the video decoder circuit to its appropriate page in the main memory. As soon as the video decoding operations are complete, the microcontroller releases the blocks of multiple pages of memory back for use by the computer.

'464 Patent Abstract.

APPLICABLE LAW

1. Claim Construction

"It is a 'bedrock principle' of patent law that 'the claims of a patent define the invention to which the patentee is entitled the right to exclude.'" *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (quoting *Innova/Pure Water Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)). To determine the meaning of the claims, courts start

by considering the intrinsic evidence. *Id.* at 1313; *C.R. Bard, Inc. v. U.S. Surgical Corp.*, 388 F.3d 858, 861 (Fed. Cir. 2004); *Bell Atl. Network Servs., Inc. v. Covad Commc'ns Grp., Inc.*, 262 F.3d 1258, 1267 (Fed. Cir. 2001). The intrinsic evidence includes the claims themselves, the specification, and the prosecution history. *Phillips*, 415 F.3d at 1314; *C.R. Bard, Inc.*, 388 F.3d at 861. Courts give claim terms their ordinary and accustomed meanings as understood by one of ordinary skill in the art at the time of the invention in the context of the entire patent. *Phillips*, 415 F.3d at 1312–13; *Alloc, Inc. v. International Trade Comm'n*, 342 F.3d 1361, 1368 (Fed. Cir. 2003).

The claims themselves provide substantial guidance in determining the meaning of particular claim terms. *Phillips*, 415 F.3d at 1314. First, a term's context in the asserted claim can be very instructive. *Id*. Other asserted or unasserted claims can also aid in determining the claim's meaning, because claim terms are typically used consistently throughout the patent. *Id.* Differences among the claim terms can also assist in understanding a term's meaning. *Id*. For example, when a dependent claim adds a limitation to an independent claim, it is presumed that the independent claim does not include the limitation. *Id*. at 1314–15.

"[C]laims 'must be read in view of the specification, of which they are a part.'" *Id*. (quoting *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995) (en banc)). "[T]he specification 'is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.'" *Id*. (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)); *Teleflex, Inc. v. Ficosa N. Am. Corp.*, 299 F.3d 1313, 1325 (Fed. Cir. 2002). This is true because a patentee may define his own terms, give a claim term a different meaning than the term would otherwise possess, or disclaim or disavow the claim scope. *Phillips*, 415 F.3d at 1316. In these situations, the inventor's

lexicography governs. *Id*. The specification may also resolve ambiguous claim terms "where the ordinary and accustomed meaning of the words used in the claims lack sufficient clarity to permit the scope of the claim to be ascertained from the words alone." *Teleflex, Inc.*, 299 F.3d at 1325. But, "'[a]lthough the specification may aid the court in interpreting the meaning of disputed claim language, particular embodiments and examples appearing in the specification will not generally be read into the claims.'" *Comark Commc'ns, Inc. v. Harris Corp.*, 156 F.3d 1182, 1187 (Fed. Cir. 1998) (quoting *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1560, 1571 (Fed. Cir. 1988)); *see also Phillips*, 415 F.3d at 1323. The prosecution history is another tool to supply the proper context for claim construction because a patent applicant may also define a term in prosecuting the patent. *Home Diagnostics, Inc., v. Lifescan, Inc.*, 381 F.3d 1352, 1356 (Fed. Cir. 2004) ("As in the case of the specification, a patent applicant may define a term in prosecuting a patent.").

Although extrinsic evidence can be useful, it is "'less significant than the intrinsic record in determining the legally operative meaning of claim language.'" *Phillips*, 415 F.3d at 1317 (quoting *C.R. Bard, Inc.*, 388 F.3d at 862). Technical dictionaries and treatises may help a court understand the underlying technology and the manner in which one skilled in the art might use claim terms, but technical dictionaries and treatises may provide definitions that are too broad or may not be indicative of how the term is used in the patent. *Id*. at 1318. Similarly, expert testimony may aid a court in understanding the underlying technology and determining the particular meaning of a term in the pertinent field, but an expert's conclusory, unsupported assertions as to a term's definition are entirely unhelpful to a court. *Id*. Generally, extrinsic evidence is "less reliable than the patent and its prosecution history in determining how to read claim terms." *Id*.

2. Claim Indefiniteness

Patent claims must particularly point out and distinctly claim the subject matter regarded as the invention. 35 U.S.C. § 112, ¶ 2. "[I]ndefiniteness is a question of law and in effect part of claim construction." *ePlus, Inc. v. Lawson Software, Inc.*, 700 F.3d 509, 517 (Fed. Cir. 2012). A party challenging the definiteness of a claim must show it is invalid by clear and convincing evidence. *Young v. Lumenis, Inc.*, 492 F.3d 1336, 1345 (Fed. Cir. 2007).

The definiteness standard of 35 U.S.C. § 112, ¶ 2 requires that:

> [A] patent's claims, viewed in light of the specification and prosecution history, inform those skilled in the art about the scope of the invention with reasonable certainty. The definiteness requirement, so understood, mandates clarity, while recognizing that absolute precision is unattainable. The standard we adopt accords with opinions of this Court stating that "the certainty which the law requires in patents is not greater than is reasonable, having regard to their subject-matter."

Nautilus, Inc. v. Biosig Instruments, Inc., 134 S. Ct. 2120, 2129–30 (2014) (internal citations omitted).

3. Construing Claim Terms that Have Previously Been Construed by This Court or Other Courts

This is not the first time a Court in this District has construed some of the disputed terms. The *Parthenon I*, *II*, and *III* Orders construed a number of the presently disputed terms and in *STMicroelectronics, Inc. v. Motorola, Inc.*, 327 F. Supp. 2d 687 (E.D. Tex. 2004) the Court construed the '789 Patent. These previous constructions do not control but can be instructive and will, at times, provide part of the basis for the Court's analysis. *See Burns, Morris & Stewart Ltd. P'ship v. Masonite Int'l Corp.*, 401 F. Supp. 2d 692, 697 (E.D. Tex. 2005) (holding a previous construction may be instructive and provide the basis for the analysis, but is not binding, particularly when there are new parties and arguments).

AGREED TERMS

The parties agreed to the following constructions. (Dkt. No. 94 at 1–2; Dkt. No. 106 at 6).

Term	Agreed Construction
"bus" '789 Patent claims 1, 13 '368 Patent claims 1, 5, 7, 13, 19, 20, 23 '045 Patent claims 1, 4, 5, 12, 15 '753 Patent claims 1, 7	"a signal line or set of associated signal lines to which a number of devices are coupled and over which information may be transferred between them"
"algorithmically translate the noncontiguous addresses to the contiguous addresses" '464 Patent claims 7, 22	"convert the noncontiguous addresses to the contiguous addresses according to at least one mathematical operation"
"display device" '368 Patent claims 1, 7, 13, 14, 20, 21 '045 Patent claims 1, 4-6, 12, 13 '753 Patent claims 1, 7	"screen and its circuitry"
"display adapter" '368 Patent claims 2, 3 '045 Patent claim 2 '753 Patent claim 3	"an adapter that processes images for a display device"
"arbiter" "arbitration circuit" "memory arbiter" "arbiter circuit" '789 patent: claims 1, 19 '368 patent: claims 1, 7, 13, 17, 19, 20, 23 '045 patent: claims 1, 4, 5, 9, 12, 15 '753 patent: claims 1, 7	"circuitry that uses a priority scheme to determine which requesting device will gain access"

DISPUTED TERMS

1. Access Terms

"selectively providing access for the first device and the decoder to the memory" ('789 Patent claim 1)

"controlling the access to said main memory" ('368 Patent claim 1; '045 Patent claim 1)

"control access to the main memory" / "control access to the memory" ('753 Patent claims 1, 7)

“controlling the access to the system memory” / “control access to the system memory” (’368 Patent claim 13; ’045 Patent claim 5)

PUMA’s Construction	Apple’s Construction
No construction necessary in view of parties’ agreed construction of “arbiter.”	“allowing/allow only one device to access the [main/system] memory at a time”

The primary dispute between the parties relates to whether the arbiter permits only one device to access memory at a time.

Positions of the Parties

PUMA notes that all of the disputed terms relate to functions of the “arbiter,” which the parties have agreed should be construed as “circuitry that uses a priority scheme to determine which requesting device will gain access.” For example, claim 1 of the ’789 Patent recites “an arbiter for selectively providing access for the first device and the decoder to the memory” and claim 1 of the ’368 Patent recites “an arbiter . . . for controlling the access to the system memory.”

PUMA contends the priority scheme of the “arbiter” is not restricted to allowing only one device to access the memory at a time. Rather, PUMA contends that, as agreed by the parties, “arbitration” is only a “priority scheme to determine which requesting device will gain access.” PUMA cites to a prior art patent and contends that a dual-port memory which includes two independent addresses and data paths for allowing two devices to access the memory at the same time was known in the art. PUMA contends the patentee did not disclaim the use of this type of memory. (*See* Dkt. No. 106 at 24.)

Apple contends that the full term must be considered and points to claim 1 of the ’368 Patent as an example. It recites: “an arbiter circuit coupled to both the microprocessor system and the decoder for controlling access to said main memory by the decoder and the

microprocessor." Apple contends that, as claimed, the "arbiter" is coupled to two devices and controls the access of those devices to the memory. Apple contends that the only plausible reading of the claim is that both devices cannot access memory at the same time. (Dkt. No. 110 at 4.)

Apple contends that in four IPR proceedings, PUMA disclaimed "arbiters" that allowed more than one device at a time to access the memory to overcome the Rathnam and Bowes references. As an example, Apple points to the arguments made in the '368 Patent IPR proceeding in which PUMA stated "Rathnam does not disclose an arbiter that controls access to the SDRAM (i.e., the alleged main/system memory)." (Dkt. No. 110 Ex. M at 31.) Apple contends PUMA specifically argued that the '368 Patent embodiments "allow multiple devices to use the bus even while only one device, e.g. the decoder, has access to main memory." (*Id*. at 32.) The full passage in question is:

> Controlling access to a bus that connects multiple system components **is not** the same as controlling access to the SDRAM (i.e., the alleged main/system memory). The distinction between accessing the bus and accessing the main/system memory is evident from the disclosure of the '368 Patent which allows, for example, the video decoder to use part of the available bandwidth of the bus to access the shared memory while the remaining bus bandwidth remains available to other components. The '368 patent specification recognizes benefit of controlling access to the memory as opposed to the memory bus. *See, e.g.*, '368 Pat. [Ex. 1001], 8:47-59 ("In the preferred embodiment, even during decoding and encoding, the decoder/encoder 80 does not always use the entire required bandwidth. Since the fast bus 70 has a bandwidth a little less than twice the size of the required bandwidth, the decoder/encoder 80 uses at most 60% of the bandwidth of the fast bus 70 . . . . In the preferred embodiment the decoder/encoder typically will be using less than 40% of the bandwidth of the fast bus 70. This frees up the remaining bandwidth to be used by the other devices with which the decoder/encoder 80 is sharing the memory 50"). By controlling access to the main memory, rather than the memory bus, embodiments of the '368 patent allow multiple devices to use the bus even while only one device, e.g. the decoder, has access to the main memory.

(*Id*. at 31–32 (emphasis in original).) Apple contends this statement disclaims more than one device at a time from accessing the memory and contends this is what is meant by "controlling access." (Dkt. No. 110 at 5–6.)

Apple also contends the prosecution of the '368 Patent contains a disclaimer:

> The arbiter 82 sends out control signals to determine **which of the devices is permitted to access the memory** via the fast bus 70, Page 20, lines 17-28. Thus while both of the devices are coupled to the memory 50, the control signal which gives them access to the memory 50 comes via the arbiter 82 which grants permission to any devices attempting to access the memory 50 **and blocks permission to the other devices**.

(Dkt. 110 Ex. X, Appellant's Brief at 4 (emphasis added).) Apple contends this makes clear that the "arbiter" determines which of the devices gets access to the memory and blocks access by the other devices.

Apple further contends that the plain language of the claims conforms to its construction of the disputed terms. Apple contends that if both the microprocessor and the decoder could access the memory at the same time, there would be no need for the limitation "controlling the access to said main memory by the decoder and the microprocessor." Apple contends in such a case no arbitration would occur.

Apple also asserts that in the specification, every disclosure regarding the "arbiter" only allows one device to access the memory at a time. Apple cites to the '368 Patent specification in support.

> Referring to FIG. 2, the operation of the arbiter 82 during a memory request will now be described. During the operation the decoder/encoder 80, the first device 42, and the refresh logic 58, if it is present, request access to memory through the arbiter 82. There may be other devices that request access to the memory 50 through the arbiter. **The arbiter 82 determines which of the devices gets access to the memory**.
> …

> It is also determined if two requests are issued simultaneously. This can be performed either before or after determining the state of the arbiter. Access to the memory is determined according to the following chart.

Arbiter state	Simultaneous requests	Action
Idle	Yes	One of the requests gets access to the memory based on the priority scheme, and the other request is queued.
Busy	Yes	Both requests are queued in an order based on the priority scheme.
Queue	Yes	Both requests are queued in an order based on the priority scheme.
Idle	No	The device gets access to the memory.
Busy	No	The request is queued.
Queue	No	The requests are queued in an order based on the priority scheme.

’368 patent 13:6–3 (emphasis added). Apple also points to the ’789 Patent specification in support.

> In the preferred embodiment of the invention the shared memory interface contains an arbiter. The arbiter and DMA engines of the video and/or audio decompression and/or compression device and of the first device are configured to arbitrate between the two devices when one of them is requesting access to the memory. This allows the use of one memory interface to control the access of both the video and/or audio decompression and/or compression device and the first device to the memory.

’789 patent, 4:2–11. Apple states that PUMA fails to point to a single portion of the specification that indicates that the “arbiter” permits multiple devices to access memory at the same time. (Dkt. No. 110 at 8.)

Apple finally contends that extrinsic evidence also supports its position. In particular, Apple points to dictionaries which define “arbiter” as “[a] functional module that accepts bus requests from requester modules and grants control of the data transfer bus (DTB) to one requester at a time.” Dictionaries also define “arbitration” as “[t]he process of determining which requesting device will gain access to a resource.” (Dkt. No. 110 Ex. Q at 43.)

Apple contends PUMA's extrinsic evidence relating to dual-port memories is irrelevant as it does not relate to "arbiters." Furthermore, Apple states that the claims relate to a single memory bus, not multiple data and address buses coupled to a dual ported memory. (Dkt. No. 110 at 8.)

Apple further objects to PUMA's contention that the agreed construction of "arbiter" controls on the issue. Apple contends the issue is not what an "arbiter" is, but what the "arbiter" does, specifically scope of the claim language that describes the function of the "arbiter." Furthermore, Apple contends its proposed construction of the limitations following "arbiter" conforms to the parties' agreed construction of "arbiter" as they agreed an "arbiter" includes a "priority scheme to determine **which requesting device** will gain access."

In reply, PUMA contends the IPR responses do not support Apple's position. PUMA contends that in the IPR responses, the distinction made between the claimed invention and the prior art was not between single devices accessing memory and multiple devices accessing memory. Rather, PUMA contends the IPR responses focused on the fact that prior art "arbiter" controlled access to the bus, while the claims required the "arbiter" to control access to the memory. (Dkt. No. 111 at 9.)

As to the primary sentence relied on by Apple, the last sentence in the IPR response above, PUMA contends that the language quoted by Apple just illustrates one difference between accessing the bus and accessing the main memory. That is, in the claimed invention, unlike in the prior art, multiple devices can access the bus while one device is accessing the memory. PUMA further contends it never characterized Rathnam as allowing multiple devices to access the main memory at the same time or took any position on that issue. (Dkt. No. 111 at 10.)

As to the quote from the ’368 Patent prosecution, PUMA contends that it is not an unequivocal disclaimer. PUMA contends the quote comes from a general background discussion of the technology and was not made with regard to any cited reference. In addition, PUMA contends none of the cited references had anything to do with whether or not multiple devices could access memory at the same time. PUMA contends that, in contrast, the applicant distinguished Wasserman by noting it failed to teach “a memory arbiter coupled to both a microprocessor system and decoder for controlling access to the main memory.” (Dkt. No. 110 Ex. X at 7.)

Analysis

At the hearing, the Court proposed a construction for “selectively providing access for the first device and the decoder to memory.” The Court proposed construing that term to mean “allowing access for only one of the first device or the decoder to the memory.” Apple agreed with the proposed construction. (Dkt. No. 120 at 6–7.) PUMA disagreed with the proposed construction. For the “controlling access” terms, the Court proposed “no construction necessary.” Apple disagreed with the proposed construction. (*Id*.)

Controlling access terms

The Court disagrees with Apple’s argument that its proposed constructions are supported by the IPR responses. The IPR responses when read in context show the distinction identified by Apple in its briefs is not the distinction the patent owner identified between the claimed invention and the prior art.

For example, the Patent Owner’s Preliminary Response for the ’368 Patent (Dkt. No. 110 Ex. M) discusses the differences between the claimed invention and Rathnam. The IPR response states that the distinction between the claimed invention and Rathnam is that “Rathnam controls

access to the internal bus, **not** access to the SDRAM (i.e., the alleged main/system memory)." (Dkt. No. 110 Ex. M at 30 (emphasis in original).) Disassembled, this statement shows the patent owner distinguished the claimed invention from Rathnam by pointing out that the "arbiter" in Rantham "control[led] access to the internal bus" while the "arbiter" in the claimed invention "control[led] . . . access to the SDRAM."

> The second paragraph also illustrates this distinction. The second paragraph states:
>
> > Therefore, Rathnam does not disclose an arbiter that controls access to the SDRAM (i.e., the alleged main/system memory). Instead, the central arbiter of Rathnam controls access to the internal bus that connects many different components, including peripherals and the PCI bus together.

(*Id*. at 31.)

> Likewise, the third paragraph draws the same distinction:
>
> > Controlling access to a bus that connects multiple system components **is not** the same as controlling access to the SDRAM (i.e., the alleged main/system memory). The distinction between accessing the bus and accessing the main/system memory is evident from the disclosure of the '368 Patent which allows, for example, the video decoder to use part of the available bandwidth of the bus to access the shared memory while the remaining bus bandwidth remains available to other components. The '368 patent specification recognizes benefit of controlling access to the memory as opposed to the memory bus.

(*Id*. (emphasis in original).)

The fourth paragraph makes the same distinction as the three paragraphs above. It also emphasizes the patent owner's position that Rathnam does not disclose a limitation that requires the arbiter to "control[] access to the main/system memory."

> The distinction between controlling access to the memory and controlling access to the bus is also evident from the claims of the '368 Patent. Specifically, independent claims 1, 5, and 13 recite an arbiter that controls access to the "main/system memory." In contrast, independent claims 7 and 20 recite an arbiter that controls access to the bus.
> . . .

> Therefore, Rathnam's alleged disclosure of a central arbiter that controls access to an internal bus **does not** satisfy the limitation of independent claims 1, 5, and 13 which recite an arbiter that controls access to the main/system memory.

(*Id*. 31–31 (emphasis added).)

In addition to the IPR responses, Apple points to the intrinsic record to support its proposed construction. The Court finds the intrinsic record does not support Apple's narrow construction.

The plain meaning of "arbiter" does not provide that an "arbiter" allows only one device at a time to access a memory. The plain meaning provides that an "arbiter" is a device that can execute "any" priority scheme for determining access. ('368 Patent 13:54–55.) The scheme must ensure, however, that the "decoder/encoder 80 gets access to the memory 50 often enough and for enough of a burst length to operate properly, yet not [so often as to] starve the other devices sharing the memory." ('368 Patent 13:55–60.) Based on this disclosure, the Court finds that an "arbiter" falls within the plain meaning of the term if the "arbiter" possesses "any" priority scheme that allows a "decoder" to gain access to a memory without "starving" the other devices in the system. This plain meaning includes an "arbiter" with a scheme that allows more than one device to access the memory. An "arbiter" can possess this scheme if the memory being accessed can support access by more than one device.

Apple has not identified any definition or disclaimer that excludes an "arbiter" with a priority scheme that allows more than one device at a time to access the memory. Apple notes the specification discloses embodiments of "arbiters" that allow one device at a time to access the memory. But Apple fails to note that the specification also teaches "arbiters" can have "any priority scheme."

The Court finds that its construction of the "controlling access" terms should focus on the idea that an "arbiter" can have "any priority scheme" that achieves the "controlling" function. The Court finds that its construction should not focus on the function of the memory and should not assume that a memory only allows access by one device at a time because the specification potentially discloses only this type of memory. Because the Court does not assume that a memory can only allow access by one device at a time, the Court does construe the disputed terms to exclude an "arbiter" with a priority scheme that can determine access to a memory that allows access by more than one device at a time. *See Interactive Gift Exp., Inc. v. Compuserve Inc.*, 256 F.3d 1323, 1331–32 (Fed. Cir. 2001) (noting a "fine line" between reading a limitation in from the specification and reading a term in context of the specification); *Arlington Indus., Inc. v. Bridgeport Fittings, Inc.*, 632 F.3d 1246, 1254 (Fed. Cir. 2011) ("[E]ven where a patent describes only a single embodiment claims will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using words of expressions of manifest exclusion or restriction.") (citation omitted).

Finally, the Court finds the intrinsic record supports the Court's construction. For example, the applicant's appeal brief states:

> The arbiter 82 sends out control signals to determine which of the devices is permitted to access the memory via the fast bus 70, Page 20, lines 17-28. Thus while both of the devices are coupled to the memory 50, the control signal which gives them access to the memory 50 comes via the arbiter 82 which grants permission to any devices attempting to access the memory 50 and blocks permission to the other devices.

(Dkt. 110 Ex. X at 4.) The appeal brief shows that an "arbiter" can allow more than one device at a time to access the memory. The appeal brief uses the word "devices" when stating "the arbiter 82 [] grants permission to any devices attempting to access the memory 50." Accordingly, the Court rejects Apple's proposed constructions and resolves the dispute as to the "controlling

access" terms. *See O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co.*, 521 F.3d 1351, 1362 (Fed. Cir. 2008) ("[D]istrict courts are not (and should not be) required to construe every limitation present in a patent's asserted claims."); *Finjan, Inc. v. Secure Computing Corp.*, 626 F.3d 1197, 1207 (Fed. Cir. 2010) ("Unlike *O2 Micro*, where the court failed to resolve the parties' quarrel, the district court rejected Defendants' construction.")

Selectively providing access terms

The Court finds the word "selectively" supports Apple's proposed construction and limits access to the memory to either the "decoder" or the "first device." Claim 1 of the '789 Patent states the "arbiter" "selectively provid[es] access for the first device and the decoder to the memory." The plainest reading of that phrase teaches that the "arbiter" "selects" between the "first device" and the "decoder" when determining access. That means the "first device" and the "decoder" cannot "access" the memory at the same time. *See Seachange Int'l, Inc. v. C-Cor Inc.*, 413 F.3d 1361, 1368–69 (Fed. Cir. 2005) (noting that different words or phrases may indicate different meanings and scope).

The Court construes **"selectively providing access for the first device and the decoder to the memory"** ('789 Patent claim 1) to mean **"allowing access for only one of the first device or the decoder to the memory."** The Court finds that **"controlling the access to said main memory," "control access to the main memory," "control access to the memory," "controlling the access to the system memory," and "control access to the system memory" need no further construction.**

2. Interface Terms

"bus interfaces coupled to the fast bus" ('368 Patent claim 7; '045 Patent claim 4)

“memory interface” (’789 Patent claim 1 ;’753 Patent claim 7)

PUMA’s Construction	Apple’s Construction
No construction necessary. Alternative construction: “hardware or software that forms a link between devices and allows them to communicate with each other”	“a device or boundary that attaches to the bus to communicate information” “a device or boundary that attaches to a memory bus to communicate information”

The parties dispute whether the use of “attached” in the constructions is proper and whether the terms may be software alone.

Positions of the Parties

PUMA contends that the term is commonly used by those skilled in the art and that the surrounding claim language provides guidance as to what the claim element means. PUMA points to claim 1 of the ’789 Patent which recites “a memory interface for coupling to the memory, and coupled to the first device and the decoder, the memory interface having an arbiter for selectively providing access for the first device and the decoder to the memory.” PUMA contends no further construction is needed. PUMA similarly points to claim 7 of the ’368 Patent which states “a plurality of bus interfaces coupled to the fast bus,” “a decoder coupled to the main memory via a first bus interface,” and “a central processing circuit coupled to the main memory via a second bus interface.”

PUMA contends that Apple’s construction ignores the claim language and would require the interface to be “attached” to the memory or the bus. PUMA contends, however, that the surrounding claim language uses “coupled.” (Dkt. No. 106 at 18.) PUMA notes that the parties agree “coupled” includes both direct and indirect connections. PUMA asserts that contradicts Apple’s use of “attached” for the bus terms. PUMA also contends the figures contradict Apple’s use of “attached.” PUMA points to Figures 1a and 1b of the ’368 Patent which show that the

memory interface 18 is not "attached" to either the memory 22 or the memory bus but rather indirectly coupled through the audio decoding circuit 14:

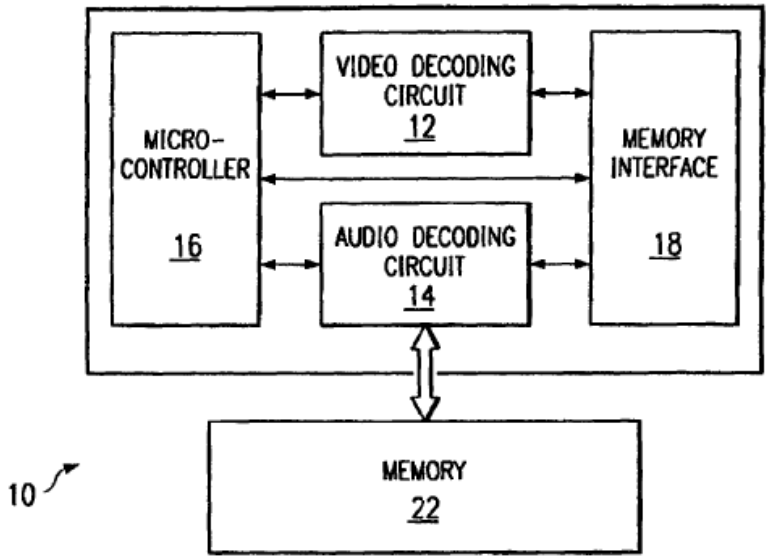

Fig. 1a
(Prior Art)

'368 Patent Figure 1a. PUMA contends if any construction is needed, PUMA's alternative construction is consistent with the term's general use in the specification and extrinsic dictionary sources. (Dkt. No. 106 at 19 (citing extrinsic definitions).)

Apple contends that the gravamen of the dispute is whether "interface" must include at least some hardware that attaches to a bus or if the "interface" may consist entirely of software with no hardware (PUMA's use of "or"). (Dkt. No. 110 at 10.) Apple contends that the plain language of the claims, the specification, and the terms all require a hardware structure.

Apple contends that the terms are used in the context of interfaces that couple to other hardware structures (e.g., bus interface "coupled to the fast bus" and "a memory interface for coupling to the memory, and coupled to the first device and to the decoder, the memory interface having an arbiter."). Apple contends hardware couples to other hardware. Apple contends it would be nonsensical to describe pure software coupled to a bus. For bus interface, Apple also

points to Figures 3 and 7 of the '368 Patent which depict interfaces 156 and 210 as part of the hardware (i.e., a device or boundary). Apple notes that interface 156 is part of the PCI core logic chipset 190, and interface 210 is part of the graphics accelerator. (*Id.* at 11.) As to "memory interface," Apple similarly asserts that the specification always references a physical connection to the bus or device. (Dkt. No. 110 at 12 (citing specification passages).)

Apple also cites to extrinsic definitions for interface. They define interface as "the place at which independent and often unrelated systems meet and act on or communicate with each other" or "a shared boundary between modules or agents of a computer system, through which information is conveyed." (*Id.* (quoting Dkt. 110 Ex. S & T).) Apple further contends that even if a device is indirectly connected to a bus, at some point there must be a physical attachment. Apple contends that the "interface" is the attachment point.

Apple contends that PUMA's first dictionary definition establishes that an interface is an "electronic device that enables one piece of gear to communicate or control another" and "a shared boundary" that "may be a piece of hardware," "a portion of computer storage accessed by two or more programs, or a surface that forms the boundary between two types of materials." (Dkt. No. 110 at 12 (quoting Dkt. No. 106 Ex. G).) Apple contends all of these structures are physical and not purely software. Apple acknowledges that PUMA's second dictionary definition does state "hardware or software that forms a link . . . ." However, Apple contends "or software" is not applicable here because, in the claims, the devices to which the interface couples are hardware (memory and buses). (*Id.* at 13.) Apple agrees software interfaces exist (for example, a web browser) but states that the claim terms are not referring to software interfaces. (*Id.*) As to Figures 1a and 1b, Apple notes that those figures are hardware figures and the figures do not support a purely software interface.

In reply, PUMA contends that the "software" issue is a red herring. PUMA asserts one skilled in the art knows that software runs on at least some hardware. PUMA contends its alternative construction comes from technical dictionaries that are meant to broadly include all types of interfaces, regardless of whether they are based in hardware or software. (Dkt. No. 111 at 8.) PUMA contends that no construction is needed, but if construed, the term should be construed to conform to technical dictionaries.

At the hearing, the Court proposed a construction for "interface" to mean "hardware, or hardware with software, that forms a link between devices and allows them to communicate with each other." PUMA agreed to this construction. Apple agreed to this construction if "link" was replaced with "that forms a physical attachment between the devices" or replaced with "physical link." (Dkt. No. 120 at 36, 40–42.)

Analysis

The Court's proposed construction addresses the pure "software" dispute by construing the term as "hardware, or hardware with software." The parties agreed on that part of the Court's construction. (*Id*. at 36, 42.) The remaining dispute centers on whether the Court should include "attachment" or "physical." Apple argued at the hearing that the language was necessary to show the "direct" nature of the connection. (*Id*. at 40–41.) However, the claims are broader than "direct" connections because the claims use the word "coupled," which the parties agree can include both direct and indirect connections.

For example, the claims in the '368 Patent and '045 Patent recite "bus interfaces coupled to the fast bus" and the claims in '789 Patent recites "memory interface for coupling to the memory, and coupled to the first device and to the decoder." Likewise, the claims in the '753 Patent recite a "central processing unit coupled to the bus for accessing the memory, the central

processing unit having a memory interface circuit." Furthermore, the specification teaches in Figures 1a and 1b of the '368 Patent, that the memory interface may be indirectly connected to the memory through other circuitry. In light of the claim language itself, the specification and the parties' positions regarding the coupling terms, the Court rejects the concept that a direct physical attachment is required.

The Court construes "interface" to mean "hardware, or hardware with software, that forms a link between devices and allows them to communicate with each other."

3. "the second bus interface of the central processing circuit" and "the first bus interface of the central processing circuit" ('368 Patent claim 7; '045 Patent claim 4)

PUMA's Construction	Apple's Construction
"the second bus interface of the central processing circuit"	Indefinite

The parties acknowledge that the term "first bus interface" located in the final clause of several claims is a drafting error. The dispute centers on if the Court can correct the clause to say "second bus interface." Claim 7 of the '368 Patent is illustrative:

> 7. An electronic system comprising:
> . . .
> a plurality of bus interfaces coupled to the fast bus;
> a decoder coupled to the main memory via **a first bus interface** . . .
> a central processor circuit coupled to the main memory via **a second bus interface** . . . and
> an arbiter circuit coupled to the decoder and to **the second bus interface of the central processing circuit** for controlling access to the bus via the respective bus interfaces of data to and from **the <u>first</u> bus interface of the central processing circuit** and the decoder.

'368 Patent claim 7 (emphasis added).

Positions of the Parties

PUMA asserts that it is clear from the claim language that the drafter mistakenly wrote "first bus interface of the central processing circuit" instead of "second" bus interface. (Dkt. No. 106 at 20.) PUMA contends that Apple ignores the fact that there is no "first" bus interface of the central processing unit and that the "first" bus interface is associated only with the decoder. In contrast, PUMA contends only the "second" bus interface is associated with the central processing unit. (*Id*.) PUMA contends there is, thus, no antecedent basis for any "first" bus interface of the central processing unit. PUMA contends that this is clear from the claim.

PUMA further contends that the broader claim element in question references "an arbiter circuit coupled to the decoder and to the second bus interface of the central processing circuit." PUMA contends this context reinforces that the "first" in the "first bus interface" should be a "second" bus interface.

Finally, PUMA cites to the other claims which contain parallel language to claim 7 of the '368 Patent but do not contain the error. For example, PUMA points to claim 1 of the '368 Patent. PUMA notes claim 1 states the "arbiter" is coupled to two elements: the "microprocessor system" and the "decoder." PUMA points out that the end of the arbiter claim limitation recites these same elements again. PUMA contends that the other claims are also similar in this fashion. (*Id*. at 21.)

Apple contends there is no antecedent basis for "the first bus interface of the central processing circuit." Apple contends it is not clear if this limitation is referring to one of the prior disclosed bus interfaces or something different all together. (*See* Dkt. No. 110 at 24.) Apple contends the error cannot be corrected by the Court because PUMA's correction does not make sense and the proper correction is subject to debate.

Apple asserts that "'[when claim language] might mean several different things and no informed and confident choice is available among the contending definitions,' the claim is invalid for indefiniteness." *Interval Licensing LLC v. AOL Inc.*, 766 F.3d 1364, 1371 (Fed. Cir. 2014) (quoting *Nautilus, Inc. v. Biosig Instruments, Inc.*, 134 S.Ct. 2120, 2130 (2014)). Apple notes: "a district court can correct a patent only if (1) the correction is not subject to reasonable debate based on consideration of the claim language and the specification and (2) the prosecution history does not suggest a different interpretation of the claims." *Smith v. ORBCOMM, Inc.*, No. 2:14-cv-666-JRG, 2015 WL 5302815, at **12–13 (E.D. Tex. Sept. 10, 2015) (citing *Novo Indus., L.P. v. Micro Molds Corp.*, 350 F.3d 1348 (Fed. Cir. 2003)).

Apple also notes: "a term does not have proper antecedent basis where such basis is not otherwise present by implication or the meaning is not reasonably ascertainable." *Halliburton Energy Servs., Inc. v. M-I LLC*, 514 F.3d 1244, 1249–50 (Fed. Cir. 2008). Apple contends that the "no reasonable debate" standard is "difficult to overcome" and generally reserved for obvious clerical errors that are evident on the face of the patent. *ORBCOMM, Inc.*, 2015 WL 5302815, at *13; *STMicroelectronics, Inc. v. Motorola, Inc.*, 327 F. Supp. 2d 687, 702 (E.D. Tex. 2004).

Apple also asserts that PUMA originally stated that no construction of these terms was needed and only when PUMA filed its brief did PUMA propose "fixing" the claims. Apple contends there must be a reasonable debate as to whether the claims should be corrected (and how), since PUMA originally proposed no construction and now PUMA proposes to change the claims. (Dkt. No. 110 at 26 (citing Dkt. No. 94-1 at 3).) Apple points to *ORBCOMM* as finding there was no obvious error that could be corrected when the plaintiff argued for an alternative construction. (*Id*. at 26–27.)

Finally, Apple contends that there is a reasonable debate as to how the claims should be corrected. Apple contends potential corrections include:

- "~~the~~ a first bus interface of the central processing circuit and the decoder;" or
- "the first bus interface of the ~~central processing circuit~~ decoder and the ~~decoder~~ central processing circuit."

Apple contends the first correction is more plausible than PUMA's proposed correction because the central processing unit would have a "first" and "second" bus interface. Apple suggests the central processing unit would have a "first" bus interface because the claim already recites a "second bus interface of the central processing circuit." Apple also contends that the second correction is more plausible than PUMA's proposed correction because it provides the recited bus interface with an antecedent basis. Apple contends these are equally plausible constructions and that PUMA has even taken the position that no construction was necessary. Apple contends that because there are several plausible and reasonable corrections, the Court cannot correct the claim.

In reply, PUMA cites the "not subject to reasonable debate" standard of *Novo Industries*. PUMA contends its correction satisfies this standard and that Apple's arguments are unreasonable. (*See* Dkt. No. 111 at 8.) PUMA contends the patentee obviously meant to refer to the "first" interface with reference to the decoder and the "second" interface with reference to the central processing circuit. PUMA further asserts that the beginning of the claim element makes clear what is meant to be referenced later in the claim: "an arbiter circuit coupled to the decoder and to the second bus interface of the central processing circuit." PUMA contends no other interpretation makes sense.

The parties elected not to provide further arguments as to this term at the hearing.

Analysis

The Federal Circuit applies a strict standard to judicial correction of claim terms:

> This case presents the question whether a district court can act to correct an error in a patent by interpretation of the patent where no certificate of correction has been issued. We hold that a district court can do so only if (1) the correction is not subject to reasonable debate based on consideration of the claim language and the specification and (2) the prosecution history does not suggest a different interpretation of the claims.

Novo, 350 F.3d at 1354. PUMA has proposed one correction to the claim—changing "second" to "first." However, Apple has proposed at least one other correction that the Court finds is subject to reasonable debate—"the first bus interface of the ~~central processing circuit~~ decoder and the ~~decoder~~ central processing circuit."

The claim states the "arbiter" is "coupled to the decoder and the second bus interface of the central processing circuit." PUMA contends this claim language renders Apple's alternative implausible because it shows that the "second bus interface" is associated with the "central processing circuit." However, the Court finds that Apple's proposed construction is likewise reasonable. The "arbiter" could be coupled to the "first bus interface" of the "decoder" and the "second bus interface" of the "central processing circuit" and still satisfy the limitations of the claim by "controlling access to the bus . . . of data to and from the central processing circuit and the decoder" Furthermore, Apple's alternative construction would not conflict with the specification. The Federal Circuit's standard does not ask the Court to decide which proposed construction is most plausible. Rather the standard only asks the Court to decide if reasonable debate exists based on the claim language and the specification. *See id.* at 1354–58. The Court finds that reasonable debate exists.

Finding that the term cannot be corrected, the Court must decide if the claim meets the "reasonable certainty" test of *Nautilus*. *See Nautilus*, 134 S. Ct. at 2129–30. Both parties

acknowledge there was a drafting error. The claim, as written, requires both a first and second bus interface of the central processing circuit. The claim does not provide an antecedent basis for the "first bus interface of the central processing circuit." The Court finds the terms in question, which are in claim 7 of the '368 Patent claim 7 and claim 4 of the '045 Patent, indefinite.

The Court finds that "the first bus interface of the central processing circuit" is indefinite.

4. Real Time and Fast Bus Terms

"in real time" / "real time operation" / "operate in real time" ('789 Patent claims 1, 13)

"the bus having a sufficient bandwidth to enable the decoder to access the memory and operate in real time when the first device simultaneously accesses the bus"('789 Patent claim 1)

"wherein the bus has a bandwidth of at least twice the bandwidth required for the decoder to operate in real time" ('789 Patent claim 13)

PUMA's Construction	Apple's Construction
"[processing] fast enough to keep up with an input data stream"	Indefinite

"fast bus" ('368 Patent claim 7; '045 Patent claim 4)

PUMA's Construction	Apple's Construction
"bus with a bandwidth equal to or greater than the required bandwidth to operate in real time"	Indefinite

The parties incorporate the arguments presented in *Parthenon I*, *II*, and *III* for "real time" and "fast bus." Those arguments center on whether the prosecution history distinguished the PCI bus of Gulick as not being real time.

Positions of the Parties

In *STMicroelectronics* the Court construed "real time" as "processing fast enough to keep up with an input data stream." *STMicroelectronics*, 327 F. Supp. 2d at 693, 710. PUMA contends that its proposed construction, which is also the *STMicroelectronics* construction, comports with the intrinsic and extrinsic evidence. PUMA asserts that the patent specification states that "[i]f the decoder does not operate in real time the decoded movie would stop periodically between images until the decoder can get access to the memory." '789 Patent 3:21–24. Elsewhere, the specification states:

> A goal is to have the decoder/encoder 45 operate in real time without dropping so many frames that it becomes noticeable to the human viewer of the movie. To operate in real time the decoder/encoder 45 should decoder [sic] and/or encode images fast enough so that any delay in decoding and/or encoding cannot be detected by a human viewer. This means that the decoder/encoder 45 has a required bandwidth that allows the decoder/encoder 45 to operate fast enough to decode the entire image in the time between screen refreshes, which is typically 1/30 of a second, with the human viewer not being able to detect any delay in the decoding and/or encoding.

Id. at 6:41-52. PUMA also cites to an IEEE dictionary and to *STMicroelectronics* in which the Court said: "The relevant dictionary definition indicates that real time concerns the processor's ability to 'keep up with' the data input." (Dkt. No. 106 at 8 (quoting *STMicroelectronics*, 327 F. Supp. 2d at 693).) PUMA notes that an expert for the defendants in the prior cases used the term "real time" in his own publications. (*Id*. at 9.)

As to "fast bus," PUMA asserts that two passages in the specification are definitional: "a fast bus 70 is any bus whose bandwidth is equal to or greater than the required bandwidth" ('368 Patent 8:27-28) and "two devices are coupled to the memory through a fast bus having a bandwidth of at least the minimum bandwidth needed for the video and/or audio decompression and/or compression device to operate in real time" ('368 Patent 5:15–18.)

Apple incorporates by reference the arguments made by the defendants in *Parthenon I, II*, and *III*. (Dkt. No. 110 at 28.) Apple presents additional evidence from the expert declaration of Donald Alpert. Apple asserts the PUMA construction is inconsistent with the patent specifications. (*Id*. at 28-29 (citing Alpert Declaration).) Apple contends the specifications indicate that the decoder can stop or drop frames when the decoder fails to keep up with the input data stream. '789 Patent 3:26–28, 11:27–40; '368 Patent 4:29–31, 8:10–12, 14:61–64. Apple contends PUMA's construction does not allow a decoder to stop or drop frames, thus excluding a preferred embodiment.

Apple further contends that the terms are vague and subjective (citing the Alpert Declaration). Apple notes that the specification states that operating the decoder in real time "reduces stops between images and the dropping of a significant number of frames to a point where both are practically eliminated" ('789 Patent 11:36–39) and "reduces stops between images and the dropping of a significant number of frames to a point where both are practically eliminated" ('368 Patent 14:61–64.) Apple contends that one skilled in the art would not know whether stops are "practically eliminated" if the stops occurred once per minute, or whether more or less frequent stops are allowed. Apple similarly contends that what particular number of dropped frames is a "significant number" or "practically eliminated" would not be known. (Dkt. No. 110 at 29–30 (citing Alpert Declaration).) Apple further contends that the specification disclosure which states that the dropped frames are not "noticeable to the human viewer" and "cannot be detected by a human viewer" ('789 Patent 6:41–52) is merely a subjective criteria and thus ambiguous.

As to fast bus, Apple contends that the inclusion of "real time" in PUMA's construction for "fast bus" similarly renders "fast bus" indefinite. Apple contends that the specification and

file history are inconsistent with regard to the prosecution and the Gulick reference. (Dkt. No. 110 at 30.)

In reply, PUMA incorporates by reference its earlier arguments from the *Parthenon I, II*, and *III* cases. (Dkt. No. 111 at 1.) PUMA also contends Apple's assertion that the terms in question do not allow a decoder to stop or drop frames conflicts with the specification:

> A goal is to have the decoder/encoder 45 operate in real time without dropping so many frames that it becomes noticeable to the human viewer of the movie. To operate in real time the decoder/encoder 45 should decoder and/or encode images fast enough so that any delay in decoding and/or encoding cannot be detected by a human viewer. This means that the decoder/encoder 45 has a required bandwidth that allows the decoder/encoder 45 to operate fast enough to decode the entire image in the time between screen refreshes, which is typically 1/30 of a second, with the human viewer not being able to detect any delay in the decoding and/or encoding.

'789 Patent 6:41–52. PUMA contends this case is not like *Interval Licensing* where the term was "purely subjective" and based on the preferences of a particular user. (Dkt. No. 111 at 2 (citing *Interval Licensing LLC v. AOL, Inc.*, 766 F.3d 1364, 1368 (Fed. Cir. 2014)).) PUMA contends that the term here relates to objective processes that are performed in accordance with standards, such as MPEG, that are known to those skilled in the art. PUMA contends that the disclosure quoted above and the understanding of those in the art provide meaning to the terms. As to whether an exact number of dropped frames must be disclosed, PUMA contends that is not the proper legal standard. (*Id*. at 3.)

The parties elected not to provide further arguments as to these terms at the hearing.

Analysis

To the extent Apple relies upon the arguments presented in the prior cases, the analysis presented in the *Parthenon I* Order at 17-24, *Parthenon II* Order at 18-26, and *Parthenon III* Order at 20-24 is applicable here and provides a basis for the Court's construction. That analysis

also provides guidance that the construction is not purely subjective as argued by Apple. Such conclusion is further supported by the specification passages cited by PUMA which provide guidance as to the meaning of the terms. ’789 Patent 3:21-24, 6:41-52; ’368 Patent 5:15-18, 8:27-28, 5:15-18. As to Apple’s argument regarding the exact number of drops, these specification passages provide sufficient objective guidance to one skilled in the art to meet the reasonable certainty standard. *See Nautilus* 134 S. Ct. at 2129 (“absolute precision” is not required); *Enzo Biochem, Inc. v. Applera Corp.*, 599 F.3d 1325, 1335 (Fed.Cir.2010) (holding that the claim phrase "not interfering substantially" was not indefinite even though the construction "define[d] the term without reference to a precise numerical measurement"). Further, the prior art (intrinsic and extrinsic) relied on by the parties provides additional evidence that the term has a non-subjective meaning to those skilled in the art.

The Court construes “real time” to mean “fast enough to keep up with an input data stream.”

The Court construes “fast bus” to mean “bus with a bandwidth equal to or greater than the bandwidth required to operate in real time.”

5. Coupled Terms

"coupleable to a main memory" / "coupleable to a memory" ('045 Patent claims 1, 4, 12; '753 Patent claims 7)

"coupled to a memory" / "coupled to the memory" / "coupled to main memory" / "coupled to system memory" ('789 Patent claim 1; '368 Patent claims 1, 7, 13, 20; '045 Patent claims 1, 4, 5; '753 Patent claim 1)

"coupling to the memory" ('789 Patent claim 1)

PUMA's Construction	Apple's Construction
a. "directly or indirectly connectable to a memory/main memory" b. "directly or indirectly connected to a memory/main memory" c. "directly or indirectly connecting to a memory/main memory"	a. "directly or indirectly connectable to the memory/main memory/system memory using no more than one bus" b. "directly or indirectly connected to the memory/main memory/system memory using no more than one bus" c. "directly or indirectly connecting to the memory using no more than one bus"

The primary issue disputed by the parties is Apple's inclusion of "no more than one bus," language that was also at issue in *Parthenon I* and *III.*

Positions of the Parties

PUMA cites three Eastern District of Texas cases which have construed "coupled" to mean directly or indirectly connected. (Dkt. No. 106 at 11.) PUMA asserts that the specification uses "coupled" to reference elements that are indirectly connected to other elements. For example, PUMA cites to Figure 1b of the '789 Patent which shows the memory interface 18 connected to an audio decoding circuit 14 and the audio decoding circuit 14 connected to the memory 22. PUMA notes the specification describes the "memory interface 18 [as] coupled to memory 22." '789 Patent 2:25. PUMA also points to Figure 2 of the '789 Patent which shows a decoder/encoder 45 connected to a memory interface 48 and the memory interface 48 connected to memory 50. PUMA notes the specification likewise states the "decoder/encoder 45 is coupled

to the memory 50 through devices, typically a bus 70." *Id*. 6:29–30. PUMA notes the '368 Patent has similar passages. (*See* Dkt. No. 106 at 12 (citing '368 Patent 2:51, 7:65–8:1).) PUMA further notes the patents use "coupled" to refer to direct connections such as in Figure 2 of the '789 Patent: "DMA engine 60 of the first device is coupled to the arbiter 54 of the memory interface 48." '789 Patent 6:15–17.

PUMA asserts that Apple's use of "no more than one bus" undercuts the commonly recognized meaning of coupled (to allow indirect connections) and conflicts with the examples and figures of the asserted patents. PUMA points to Figure 1c of the '789 Patent which is described as "show[ing] a computer 25 containing a decoder 10, a main memory 168 and other typical components such as a modem 199, and graphics accelerator 188. The decoder 10 and the rest of the components are coupled to the core logic chipset 190 through a bus 170." '789 Patent 2:49–53. PUMA asserts the figure shows that the modem 199 is "coupled" to the core logic chipset 190 through ISA bus 198 and PCI bus 170, resulting in a "coupling" arrangement that includes two buses. (Dkt. No. 106 at 12.)

PUMA also points to Figure 7 of the '368 Patent, an alternative embodiment. As to Figure 7, the specification says that "if the peripherals are compatible to the PCI bus, the EIDE interface 186 can be integrated into the PCI chipset 190 and the peripherals 164 and 166 can be coupled directly to the PCI chipset, eliminating PCI bridge 192 and ISA bus 198." '368 Patent 12:65–13:5. PUMA notes that in the *Parthenon I* Order, the Court found "[t]his passage implies that absent the modifier 'directly,' the word 'coupled' has a broader meaning than the phrase 'directly coupled.'" *Parthenon I* Order at 32.

Apple contends that under PUMA's construction, every component of a computer system is "coupled to" memory. (Dkt. No. 110 at 22.) Apple contends every description of "coupling" in

the specification, with regard to coupling to a memory, involves an attachment that includes no more than one bus. (Dkt. No. 110 at 22.)

Apple further contends that the prosecution history supports its construction. Apple contends Lambrecht, which was discussed during the prosecution of the '459 Patent, disclosed a CPU and Multimedia device attached to main memory via two buses. Apple contends the applicant distinguished Lambrecht on this basis—that the claimed invention had one bus and Lambrecht had two buses. (*See* Dkt. No. 110 at 22 (citing Dkt. No. 110 Ex. V (stating Lambrecht uses a PCI bridge chipset for access between other first devices or decoders and a main memory and this was not direct access for a first device and decoder to a first memory)).) Apple further contends that during the '368 Patent prosecution, the applicant characterized the "present invention" as having "both the decoder and the device 42 . . . directly coupled to the fast bus 70, which in turn is coupled to the memory 50." (*Id*. at 23 (quoting Dkt. No. 110 Ex. W at 10).) Apple notes that in an appeal brief, the applicant again argued that "since the same bus is concurrently coupled to both of the devices, both of them have the ability to place data on and retrieve data from the bus 70, each of them having direct access to the fast bus 70." (*Id*. (quoting Dkt. No. 110 Ex. X at 4).)

As to PUMA's reliance on Figure 1c of the '789 Patent, Apple contends the figure and related discussion do not apply to coupling components to memory. (*Id*.) Apple further contends the surrounding paragraphs make clear that Figure 1c is not a preferred embodiment because "the addition of each bus is very expensive." '789 Patent at 2:45–3:12. Apple contends that Figure 1c was the problem the patentees sought to overcome. (Dkt. No. 110 at 23.)

As to the Court's prior distinction of "directly coupled" and "coupled," Apple contends that unlike prior defendants, Apple's construction includes "directly" and "indirectly." Apple

contends what Apple is seeking for construction is not "coupled" but "coupled *to main memory*." (*Id*. at 23–24.)

In reply, PUMA contends that it is clear "coupled" includes indirect connections including two buses. PUMA contends, again, that the Figure 1c discussion describes the modem 199 as being coupled to the core logic chipset, yet Figure 1c shows the coupling through bus 170 and 190. (Dkt. No. 111 at 3.) PUMA contends the mere fact that Figure 1c is prior art does not negate that the specification clearly contemplates "coupling" through two buses.

As to the prosecution history of the '459 Patent, PUMA contends that Apple's reliance is misplaced. PUMA contends the language in question relates to the addition of "direct access" language and the configuration of the arbiter. (*Id*. at 4.) PUMA further contends the claim in the '459 patent stated the decoder was "coupled" to the memory and that the decoder had "direct access" to the memory. PUMA asserts that shows the patentees did not intend to narrow the commonly used term "coupled" as argued by Apple. PUMA further notes that the amended claims in the prosecution history of the '459 Patent were canceled and that the issued claims did not use the "direct access" language or the "without also requiring a second bus" language found in the other patents. (*Id*.)

PUMA contends Apple's reliance on the prosecution history of the '368 Patent is similarly misplaced. PUMA contends that the key difference between the claimed invention and Cheney and Wasserman is that these prior art references did not disclose an arbiter that controlled access to the main memory by both the decoder and the microprocessor. (*Id*. at 5 (citing Dkt. No. 110 Ex. W at 8–10).) PUMA notes the applicant stated "the present invention discloses an arbiter as a component of the decoder that is not only responsible for arbitrating between the decoder and the devices external to the decoder, but also able to directly control the

other devices' access to memory." (Dkt. No. 110 Ex. W at 10.) PUMA contends that to highlight this concept, the applicant pointed to Figure 2 of the '368 Patent which shows "both the decoder 80 and the device 42 [] directly coupled to the fast bus 70, which in turn couple to the memory 50." (*Id*.) PUMA contends the patentee pointed out Figure 2 to assist the Examiner in recognizing why Wasserman did not disclose an arbiter that controlled the access of the decoder and the CPU to the memory. The applicant further said that unlike in Figure 2, "Wasserman shows the decoder core is coupled to the memory controller 106. The memory controller 106 is coupled to the bus unit 104 and the system memory controller 110. The bus unit, in turn is coupled to the CPU." (Dkt. No. 111 at 5 (quoting Dkt. No. 110 Ex. W at 10).) PUMA contends that in Wasserman memory controller 106 did not control access by the CPU because "requests to access system memory from the CPU must first pass through the memory controller 106 of the decoder." (Dkt. No. 110 Ex. W at 10) PUMA contends the patentees raised this same argument on appeal and ultimately prevailed, without the PTO requiring any change to the claims' use of "coupled." (Dkt. No. 111 at 6.)

The parties elected not to provide further arguments as to these terms at the hearing.

Analysis

Apple acknowledges that "coupling" includes direct and indirect connections. However, Apple contends that "coupling," when used to describe memory, requires the use of no more than one bus. Apple does not contend this is the plain meaning of "coupled." But it does contend that the specification and the prosecution history support its construction. The Court disagrees for the reasons below.

In the intrinsic record, the applicant uses the term "coupled" in a way that is consistent with its plain meaning. As both parties agree, the plain meaning allows both direct and indirect

connections. For example, the specification of the ’789 Patent describes the memory interface 18 of Figure 1b as “coupled” to memory 22. It describes the components as “coupled” despite the presence of at least the audio decoding circuit and the bus between the components. ’789 Patent 2:25, Figure 1b. The specification further contains similar disclosures as to Figure 2 of the ’789 Patent. The specification says that the decoder/encoder 45 is “coupled” to the memory 50 but recognizes that “devices” such as the memory interface 48 and bus 70 can sit in-between the two components. *Id*. Figure 2, 6:29–32. Finally, the specification of the ’789 Patent describes the modem 199 as “coupled” to the core logic chipset 190 even though the components are linked through the ISA bus and the PCI bus. ’789 Patent Figure 1c, 2:49–53.

As shown above, the plain meaning of “coupled” includes indirect connections. Thus, components that are associated through more than one bus can be “coupled” because they are indirectly connected. Given the plain meaning of “coupled,” even if the specification discloses embodiments where memory components are associated through only one bus, the Court should not read those embodiments into its construction. *See Arlington*, 632 F.3d at 1254 (“[E]ven where a patent describes only a single embodiment claims will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using words of expressions of manifest exclusion or restriction.”) (citation omitted). Furthermore, Apple’s one bus construction imposes a negative limitation on the plain meaning of “coupled” because it excludes components indirectly connected through more than one bus. Apple has not pointed to intrinsic evidence that shows the negative limitation is warranted. *See Santarus, Inc. v. Par Pharms., Inc.*, 694 F.3d 1344, 1351 (Fed. Cir. 2012). Indeed, in contrast to Apple’s position, Figure 1c of the ’789 Patent shows that the modem and core logic chipset are “coupled” despite being connected across two busses.

Apple contends that PUMA's construction would provide no limits to coupling and include all devices in a computer. Apple, thus, asserts that PUMA's construction effectively allows for all the devices shown in all the figures to be "coupled." The Court rejects Apple's assertions. The evidence submitted does not indicate that one skilled in the art would reach this conclusion.

Apple further relies on various prosecution histories, including the related '459 Patent. As the Court noted in prior Orders, these arguments do not support imposing a negative limitation on the plain meaning of a term. *Parthenon I* Order at 32–34. In fact, some of these file history arguments emphasize that "coupling" is not limited to one bus.

As to the arguments directed at the '459 Patent, the applicant discussed "direct" access in the prosecution history because the applicant added "direct" access and the claims issued with a "without also requiring a second bus" limitation. (Dkt. No. 110 Ex. V at 2–6); '459 Patent claim 1. That some claims explicitly require "without also requiring a second bus" shows that the applicant included the limitation when it was intended. That undercuts Apple's assertion that a "direct" limitation should be in all claims with "coupled."

With regard to the applicant's use of "directly coupled" in the prosecution history of the '368 Patent, the cited response indicates that the applicant used the phrase to describe the arbiter's ability to directly control access to memory by the decoder and other devices. (Dkt. No. 110 Ex. W at 10.) It is accurate to state the applicant described the devices in an embodiment of the figures as "directly coupled" to the fast bus. But the Court finds that this statement does not create a disclaimer to the plain meaning of "coupled." Rather, the Court finds the statement relates to an example of the applicant describing a particular embodiment to the Examiner. Moreover, the example is not limiting because the applicant's use of "direct" implies that

"coupled" means more than "directly" coupling. *See Phillips*, 415 F.3d at 1314 ("[T]he claim term in this case refers to 'steel baffles,' which strongly implies that the term 'baffles' does not inherently mean objects made of steel.").

As to the "present invention" language in the prosecution history of the '368 Patent, the Court finds that it does not define "coupled." The first use of the term emphasizes that arbitration is "decoupled" from bus access. It does not state that all devices that are "coupled" must be "directly coupled" on the same bus. Specifically, the passage in question states "[i]n the present invention, arbitration is decoupled from bus access." (Dkt. No. 110 Ex. W at 10.) It then goes on to describe devices that are both "directly coupled" and "coupled" to the bus. (*Id*. ("decoder 80 and the device 42 are directly coupled to the fast bus, which in turn is coupled to the memory 50").) Nowhere in this passage does the applicant adopt a one bus limitation to "coupled."

As to the statement in the appeal brief of the '368 Patent, the Court finds that the applicant's statement was made in the course of explaining Figure 2. The applicant expressly states that Figure 2 "provides one example of the inventive features." (Dkt. No. 110 Ex. X at 2.) Figure 2 is just an "example" of the claimed invention, thus, on the whole, the applicant's statement in the appeal brief does not show its intent to disavow or disclaim the plain meaning of "coupled." (*Id*. at 2–4; *see also Pacing Techs., LLC v. Garmin Int'l, Inc.*, 778 F.3d 1021, 1025 (Fed. Cir. 2015) (finding disclaimer when the applicant states that one embodiment accomplishes all of the objects of the invention)).

Apple finally points to a discussion about the devices having direct access to the fast bus, but similarly, the Court finds this does not limit the claim to "no more than one bus." The discussion did not focus on "no more than one bus." In the context of the overall intrinsic record, the patentee did not make a clear disclaimer of the term "coupled." As the Federal Circuit has

said, "[w]hen the prosecution history is used solely to support a conclusion of patentee disclaimer, the standard for justifying the conclusion is a high one." *Avid Tech., Inc. v. Harmonic, Inc.*, 812 F.3d 1040, 1045 (Fed. Cir. 2016).

The court construes "coupled" to mean "directly or indirectly connected," "coupleable" to mean "directly or indirectly connectable," and "coupling" to mean "directly or indirectly connecting."

6. "control circuit" ('464 Patent claims 1, 2, 7-13, 16-24, 32)

PUMA's Construction	Apple's Construction
No construction necessary.	"an electronic control device that is not a CPU or other processor"

The parties dispute whether the control circuit must be something other than a processor.

Positions of the Parties

PUMA asserts that the term is defined by the surrounding claim language. PUMA points out that claim 1 of the '464 Patent specifies the arrangement of the "control circuit" by stating it is coupled to the decoding circuit, the processor, and the main memory. PUMA then notes the "control circuit" is configured to "request continuous use of several portions of the main memory from the operating system" and to "translate the noncontiguous addresses to contiguous addresses of a block memory." '464 Patent claim 1.

PUMA objects to Apple's construction for at least two reasons. First, PUMA asserts that replacing "circuit" with "device" provides no additional guidance. (Dkt. No. 106 at 16.) Second, PUMA contends that saying the "control device [] is not a CPU or other processor" reads out embodiments described in the specification such as Figure 2 of the '464 Patent.

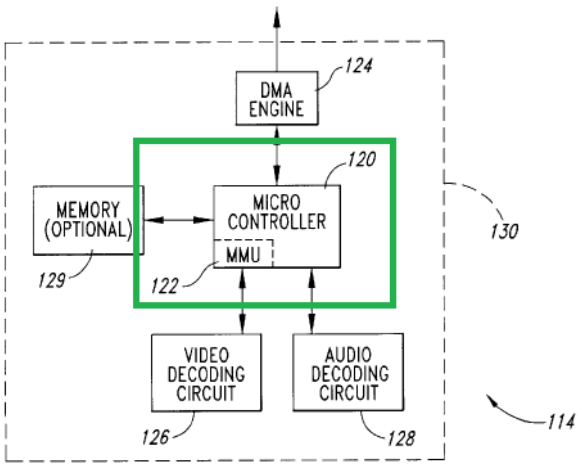

Fig. 2

'464 Patent Figure 2 (color added).

For example, PUMA states that in Figure 2, the memory management 122 is part of the microcontroller. It "algorithmically maps a contiguous address to a noncontiguous address in the main memory 106." ('464 Patent 8:21–23.) PUMA notes that dependent claim 16 explicitly recites the "control circuit includes a memory management unit that is configured to translate the noncontiguous addresses to the contiguous addresses." ('464 Patent 10:61–64.) PUMA contends Apple's construction would read out these embodiments and contradicts the claim language. (*See* Dkt. No. 106 at 17.)

In response, Apple contends that PUMA has conceded that "control circuit" has no accepted meaning because PUMA has argued its meaning is supplied by the surrounding claim language. Apple notes its expert states that the term has no accepted meaning. Apple further contends when a term has no accepted meaning, the term can only be construed as broadly as provided in the specification. (*See* Dkt. No. 110 at 14 (citing *Irdetro Access, Inc. v. Echostar Satellite Corp.*, 383 F.3d 1295, 1300 (Fed. Cir. 2004)).)

Apple notes "control circuit" appears in all independent claims of the '464 Patent. Apple asserts claim 10 is representative of how the term is used in the '464 Patent. Claim 10 provides:

"a control circuit coupled to the processor and the main memory, the control circuit being configured to request continuous use of several portions of the main memory from the operating system." ('464 Patent 10:38–47.) The claims separately recite the "control circuit" as "coupled to the . . . processor." Apple contends this shows that the "control circuit" is not the "processor" which supports its proposed construction. (Dkt. No. 110 at 14-15.)

Apple further contends the specification consistently distinguishes the "control circuit" from a processor. Apple asserts this use in the specification must govern because the claim term has no accepted meaning in the art. (*Id*. at 15.) Apple notes that the Summary of the Invention states that "an electronic device is coupled to the processor and the main memory . . . to request continuous use of several portions of the main memory." '464 Patent at 3:40–43. Apple suggest that this shows the "control circuit" is an electronic device "coupled to the processor" and not the processor itself. Apple also notes that the specification states "[t]he MPEG2 decoder 114, including the video decoding circuit 126 and microcontroller 120, is not a CPU, or other processor, or Intel-based microprocessor." '464 Patent at 9:19–21. Apple contends this paragraph characterizes the decoder as "the present invention." (Dkt. No. 110 at 15–16 (citing '464 Patent at 9:14-16).) Finally, as to the specification, Apple says the figures show that the MPEG decoder 114, which includes the "control circuit," is distinct from CPU 104. Apple contends the specification teaches that the microcontroller 120 of the decoder 114 performs the claimed "control circuit" functions, not the system CPU or processor. (*Id*. at 16 (citing '464 Patent 7:1-50, 8:36–44).) Apple contends these teachings from the specification must control in the absence of an accepted meaning.

Apple finally contends that the prosecution history supports its construction. Apple contends that in response to a rejection over Harrell, the applicant added a "control element"

limitation to the claims. Apple contends the applicant distinguished Harrell on the basis that Harrell "does not teach the administration of a memory management method through a separate control circuit that requests continuous use of several portions of main memory." (*Id*. at 17 (quoting Dkt. 110 Ex. R at 5).) Apple asserts the applicant, thus, argued that claim 25 was different because, as amended, it "further recites a control circuit used in combination with a decoding circuit, the processor and the main memory." (*Id*. (quoting Dkt. 110 Ex. R at 5).) Apple contends the applicant unambiguously limited the "control circuit" to an element that was not the processor or CPU. Apple contends PUMA's construction directly conflicts with the claims, specification, and prosecution history. (*Id*. at 18.)

In reply, PUMA again points to Figure 2 and asserts Apple's construction reads out the embodiment which shows the memory management unit can be part of the microcontroller. PUMA contends the patent explicitly characterizes the microcontroller as a "control circuit." (*See* Dkt. No. 111 at 7.) PUMA further contends the specification explicitly uses "microcontroller" but never once uses the phrase "specialized electronic device." (*Id*.)

The parties elected not to provide further arguments as to this term at the hearing.

Analysis

The arguments in the prior cases focused on whether the "control circuit" and the processor could be circuits formed on the same device. *See Parthenon I* Order at 44; *Parthenon III* Order at 29. Apple shifts the argument. Apple seeks a construction that excludes the "control circuit" from being "any other processor."

The specification of the '464 Patent discloses an embodiment of the decoder where the "control circuit" is in the microcontroller. A microcontroller falls within the scope of "any other processor." Thus, the Court rejects Apple's construction. The specification does not show that a

construction that excludes an embodiment is supported by the intrinsic record. (*See* Dkt. No. 110 at 17 (citing Alpert Declaration).)

Apple, however, correctly states that the "control circuit" is distinct from the system's processor or CPU. The claims state the "control circuit" is "coupled" to the processor and the specification shows that the system processor and the "control circuit" are separate components of the claimed invention. This conforms to the prosecution history statements on Harrell which note that the claimed invention has a separate "control circuit." The full intrinsic record teaches that the "control circuit" and the system processor are not the same device. With such clarification, the Court finds that no further construction is necessary.

The Court finds that "control circuit" needs no further construction other than that the "control circuit" is not the same circuit as the claimed "processor."

7. Supply Terms

"directly supplied" ('368 Patent claim 3)

"directly supplies" ('368 Patent claims 14, 21; '045 Patent claims 2, 6, 13; '753 Patent claim 3)

PUMA's Construction	Apple's Construction
a. "supplied without being stored in main memory for purposes of decoding subsequent images" b. "supplies without being stored in main memory for purposes of decoding subsequent images"	a. "the images directly supplied to the display adapter" means "images that are provided from the decoder to the display adaptor without being stored in the main memory" b. "the decoder directly supplies a display adapter [device] with an image" means "an image is provided from the decoder to the display adaptor [device] without being stored in the main memory"

The dispute in the prior *Parthenon* cases focused on construing the term to mean images could be supplied without the use of any "intervening components." The dispute in this case focuses on Apple's claim that including the phrase "for purposes of decoding subsequent

images" allows images to be stored in the memory (albeit only for other purposes) and then indirectly supplied to the display adapter (from the decoder to the memory to the display adapter).

Positions of the Parties

PUMA contends that "directly supplied" concerns the system's use of decompressed frames in the context of video coding. PUMA contends the phrase "directly supplied" reflects the fact that certain types of MPEG frames do not need to be transferred to main memory for use in the subsequent decoding of other frames. PUMA notes I-frames (intra-coded frames) do not require data from other frames in order to be decompressed, P-frames (predicted frames) use data from previous images, and B-frames (bidirectional frames) use data from both previous and forward frames. (Dkt. No. 106 at 14.) PUMA notes the patent states that "intra and predicted images are likely to be used to reconstruct subsequent predicted and bidirectional images, while the bidirectional images are not used again." '753 Patent 3:28-30. PUMA further contends that "[i]n the case where the compressed data correspond to bidirectional images, the decoder/encoder 80 decodes these data and directly supplies display adapter 120 with the decoded data." *Id.* at 10:39-42.

PUMA objects to Apple's construction as suggesting that data corresponding to bidirectional images never gets stored in the memory. PUMA contends the patent contemplates that bidirectional images may be stored in the memory because "compressed or coded data CD are transferred from image source 122 to buffer CDB of memory 168 . . . . In the case where the compressed data correspond to bidirectional images, the decoder/encoder 80 decodes these data and directly supplies display adapter 120 with the decoded data." *Id.* at 10:34–42. PUMA states

this is in contrast to the I-frames and P-frames which are stored in memory for subsequent use in decoding other images.

Apple objects to the "for purposes of decoding subsequent images" as negating the "directly supplies" limitation. Apple contends PUMA's construction would allow images to be indirectly supplied to the display adaptor and stored in memory as long as the storage was for purposes other than "decoding subsequent images." (Dkt. No. 110 at 19.) Apple contends that representative claim language includes: "the images directly supplied to the display adapter being bidirectional images obtained from two preceding intra or predicted images" ('368 Patent claim 3) and "the video circuit directly supplies a display adapter with an image under decoding which is not used to decode a subsequent image" ('753 Patent claim 3). Apple contends there is nothing that states the image is directly supplied only when the image is supplied "for purposes of decoding subsequent images."

For example, Apple contends that the patent makes clear what "directly supplied" means in Figure 4.

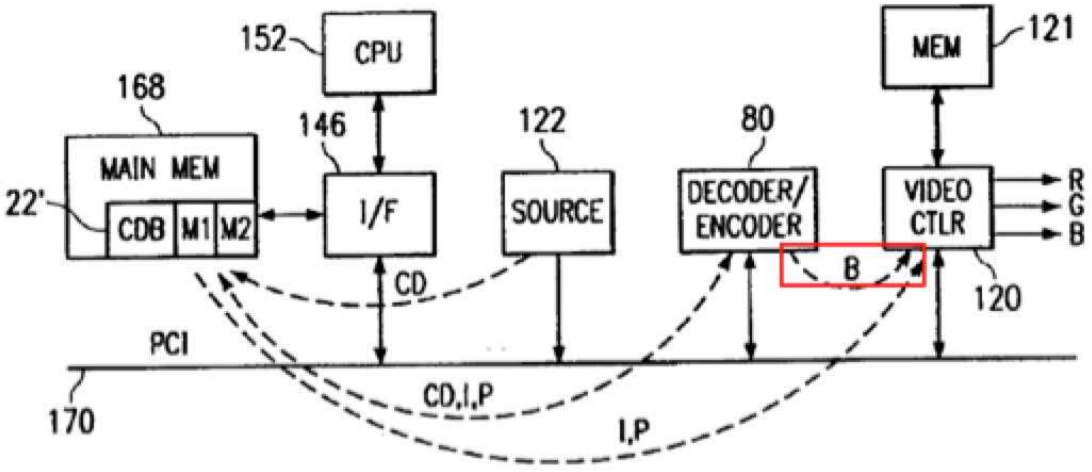

Fig. 4

‘

’368 Patent Figure 4 (color added). Figure 4 of the ’368 Patent shows a “direct supply” of the B-frames from the decoder/encoder to the video controller without the B-frames being supplied to memory. (Dkt. No. 110 at 19-20.) Apple contends this excludes PUMA’s construction which would allow images to go back to the memory as long as it was for a purpose other than decoding. Apple contends that the patent touts the benefits of “direct supply” and those benefits would be lost if there were an intervening step of accessing the memory. The patent states: “a buffer associated with bidirectional images is not required” and the bus rate “is substantially decreased due to the bidirectional images not being stored in main memory 168.” ’368 Patent 10:52–11:8. Apple contends that allowing the images to be stored in memory for any purpose would defeat these benefits.

Apple contends PUMA cites only a short specification passage in support of its construction. ’753 Patent 10:34–42. Apple asserts the passage in full does not show the images may go to the main memory on their way to the display adapter:

> Thus, in the system of FIG. 4, compressed or coded data CD are transferred from image source 122 to buffer CDB of memory 168. These same compressed data are then transferred to the decoder/encoder 80 which, if they correspond to intra or predicted images, retransmits them in decoded form to buffers M1 and M2 of memory 168. In the case where the compressed data correspond to bidirectional images, the decoder/encoder 80 decodes these data and directly supplies display adapter 120 with the decoded data.

’753 Patent 10:34–42. Apple contends the last sentence makes clear that directly supplying an image from the decoder to the display adapter does not include accessing the memory. (Dkt. No. 110 at 21.)

In reply, PUMA contends that it is clear from the specification that “directly supplied” must be viewed from the context of bidirectional decoding frames. The specification says: “video circuit directly supplies a display adapter with an image under decoding which is not used to

decode a subsequent image." '753 Patent claim 3. PUMA contends Apple's construction is flawed in that Apple's construction implies that bidirectional images never get stored in memory. PUMA notes the patent explicitly states however that "compressed or coded data CD are transferred from image source 122 to buffer CDB of memory 168 . . . . In the case where the compressed data correspond to bidirectional images, the decoder/encoder 80 decodes these data and directly supplies display adapter 120 with the decoded data." '753 Patent 10:34–42. PUMA contends the patent explicitly contemplates that bidirectional images are stored in memory. PUMA contends that its construction captures the concept that the images are not stored in memory for subsequent decoding.

The parties elected not to provide further arguments as to these terms at the hearing.

Analysis

Apple contends the construction from *Parthenon I*, *II*, and *III* can be interpreted as allowing data to be transferred from the decoder to the main memory before the data is supplied to the display adaptor. Apple contends the Court's previous construction allows this whenever the data transferred to the memory is not used for decoding subsequent images.

The Court addresses this concern by concluding that data that is "directly suppled" must be supplied without first being stored in the main memory. The Court found in *Parthenon I* and *II* that:

> The[] passages above show that bidirectional images are not decoded by the decoder and then provided to the main memory for later transfer to the display adaptor. Rather, bidirectional images are provided from the decoder to the display adaptor without storage in the main memory. The bypassing of the main memory is the context in which "directly supplied" is utilized in the specification.
> . . .
>
> Defendants' emphasis of "no intervening" components lacks support in the specification. First, in all embodiments, the decoder provides the bidirectional images to the display adaptor through an intervening bus. Thus, Defendants'

> "directly supplied" architecture approach needs the qualification contained in Defendants' proposed construction ("via a single bus").

Parthenon I Order at 39; *See Parthenon II* Order at 38-39. As stated in those Orders, "bypassing [] the main memory is the context in which 'directly supplied' is utilized in the specification." *Parthenon I* Order at 40. That means the data "directly supplied" to the display adapter cannot first be stored in the memory because it must "bypass" the main memory.

PUMA argues the clarification proposed in Apple's construction would conflict with the specification of the '753 Patent. *See* '753 Patent 10:34-42. However, the specification, when read in context, clearly states that the storage in memory occurs before the data is sent to the decoder. The storage does not occur after the data has been sent to the decoder but before it is sent to the display adapter.

> [I]n the system of Figure 4, compressed or coded data CD are transferred from image source 122 to buffer CDB of memory 168. These same compressed data are then transferred to the decoder/encoder 80 which, if they correspond to intra or predicted images, retransmits them in decoded form to buffers M1 and M2 of memory 168. In the case where the compressed data correspond to bidirectional images, the decoder/encoder 80 decodes these data and directly supplies display adapter 120 with the decoded data. The display adapter then supplies these data to a display device such as a screen. The intra or predicted images stored in buffers M1 and M2 are transferred to display adapter 120 at the appropriate time and are used in the decoding of subsequent predicted or bidirectional images.

'368 Patent 10:56-11:2. The specification's discussion of storage of data in the compressed form is not relevant to the "direct supply" of bidirectional images. In sum, the Court's construction of "directly supplied" does not include supplying the decoded data from the decoder to the memory and then from the memory to the display adapter. The Court clarifies its construction to remove "for purposes of decoding subsequent images."

The Court construes "directly supplied" and "directly supplies" to mean "supplied/supplies without being stored in main memory."

CONCLUSION

The Court adopts the reasoning and constructions above. The parties should ensure that all testimony that relates to a term addressed in this Order is constrained by the Court's reasoning and by its constructions. In the presence of the jury, however, the parties should not expressly or implicitly refer to each other's claim construction positions and should not expressly refer to any portion of this Order that is not an actual construction adopted by the Court. The references to the claim construction process should be limited to informing the jury of the constructions adopted by the Court.

IT IS SO ORDERED.

SIGNED this 16th day of June, 2016.

ROY S. PAYNE
UNITED STATES MAGISTRATE JUDGE