Not Reported in F.Supp.2d, 2006 WL 3447632 (E.D.Tex.)
(Cite as: 2006 WL 3447632 (E.D.Tex.))

Only the Westlaw citation is currently available.

United States District Court,
E.D. Texas,
Marshall Division.
MAURICE MITCHELL INNOVATIONS, L.P.,
Plaintiff
v.
INTEL CORPORATION, Defendant.
No. 2:04-CV-450.

Nov. 22, 2006.

Franklin Jones, Jr, Jones & Jones, Marshall, TX, Richard L. Schwartz, Whitaker Chalk Swindle & Sawyer, Fort Worth, TX, Andrew Wesley Spangler, Elizabeth L. Derieux, Sidney Calvin Capshaw, III, Brown McCarroll, Thomas John Ward, Jr, Law Office of T. John Ward Jr. PC, Longview, TX, Daniel Rapaport, Wendel Rosen Black & Dean, Oakland, CA, Manny D. Pokotilow, Caesar Rivise Berstein Cohen & Pokotilow, Philadelphia, PA, Otis W. Carroll, Jr, Ireland Carroll & Kelley, Tyler, TX, for Plaintiff.

Eric Hugh Findlay, Ramey & Flock, Allen Franklin Gardner, John Frederick Bufe, Michael Edwin Jones, Potter Minton PC, Tyler, TX, Christa M. Anderson, Clement S. Roberts, Robert A. Van Nest, Ryan M. Kent, Keker & Van Nest, San Francisco, CA, for Defendant.

MEMORANDUM OPINION AND ORDER

LEONARD DAVIS, District Judge.

***1** Before the Court is Defendant Intel Corporation's ("Intel") motion for summary judgment as to invalidity under 35 U.S.C. § 112 (Docket No. 104). Having considered the parties' written submissions and oral argument, the Court **GRANTS** the motion.

BACKGROUND

Maurice Mitchell Innovations, L.P. ("Mitchell") filed suit against Intel on December 17, 2004 alleging infringement of Claim 1 of U.S. Patent No. 4,875,154 ("the '154 patent"). In general, the '154 patent discloses what the patent refers to as a "Bimemory Independent CPU ('central processing unit')" microcomputer, also referred to as a "BICPU microcomputer." According to the specification, the BICPU microcomputer

> is comprised of a known CPU chip with additional circuitry to enable the CPU to interact in a multi BICPU microcomputer system. Each BICPU microcomputer within a system is supplied with an assigned standard memory-mechanically and logically connected to its BICPU's "A" bus circuits. The BICPU microcomputer is also provided with connectors enabling the CPU to be connected to system buses.

Col. 7:3-12. In general terms, the specification says that the invention allows a number of BICPU microcomputers to be linked together in a "bimemory independent pattern" using a "standard" set of system buses to mechanically interconnect "B" or "C" bus circuits of any two BICPU microcomputers. Col. 7:12-22. Mitchell claims Intel's products, including *inter alia*, the ASCI Red super computers, the Pentium II, Pentium III, and Pentium IV processors, contain chipsets that infringe the '154 patent.

At the *Markman* hearing, the Court construed Claim 1 limitations nine and ten, [FN1] and thirteen and fourteen [FN2] as means-plus-function terms and construed the functions of those terms. Intel argued at the hearing that there were no corresponding structures for these functions. At the hearing, Mitchell argued that the terms were not means-plus-function limitations. In order to be fully briefed on the issue of corresponding structure, the Court did not identify the corresponding structures for these functions and instead deferred the issue to summary judgment. The determination of whether a

corresponding structure exists for these functions is now ripe for decision.

> FN1. Limitation nine states "first switch means comprised of at least three distinct parts for connecting said dedicated memory address, data, and control circuits of said path configuring means to each of said first three sets of contacts."
>
> Limitation ten states "second switch means for connecting said dedicated memory address, data, and control lines of said path configuring means to said dedicated memory address, data, and control lines of said CPU respectively."
>
> FN2. Limitations thirteen and fourteen state "means for causing said first and second switch means to remain in said non signal-conducting state upon application of power to said CPU power circuit and to assume a signal conductive state upon receipt of an appropriate signal from said CPU" and to "assume a non signal-conducting state upon receipt of an appropriate signal from said CPU."

APPLICABLE LAW

Summary Judgment Standard

Summary judgment shall be rendered when the pleadings, depositions, answers to interrogatories, and admissions on file, together with the affidavits, if any, show that there is no genuine issue as to any material fact and that the moving party is entitled to judgment as a matter of law. FED.R.CIV.P. 56(c); *Celotex Corp. v. Catrett*, 477 U.S. 317, 323-25 (1986); *Ragas v. Tenn. Gas Pipeline Co.*, 136 F.3d 455, 458 (5th Cir.1998). An issue of material fact is genuine if the evidence could lead a reasonable jury to find for the non-moving party. *Anderson v. Liberty Lobby, Inc.*, 477 U.S. 242, 248 (1986). In determining whether a genuine issue for trial exists, the court views all inferences drawn from the factual record in the light most favorable to the non-moving party. *Id.; Matsushita Elec. Indus. Co. v. Zenith Radio*, 475 U.S. 574, 587 (1986).

Indefiniteness

***2** A patent is entitled to a presumption of validity, and an accused infringer must prove invalidity by clear and convincing evidence. *Metabolite Labs., Inc. v. Lab. Corp.*, 370 F.3d 1354, 1365 (Fed.Cir.2004). The requirement that "claims 'particularly point ... out and distinctly claim ...' the invention is met when a person experienced in the field of the invention would understand the scope of the subject matter that is patented when reading the claim in conjunction with the rest of the specification." *Default Proof Credit Card Sys., Inc. v. Home Depot U.S.A., Inc.*, 412 F.3d 1291, 1298 (Fed.Cir.2005) (quoting *S3 Inc. v. nVIDIA Corp.*, 259 F.3d 1364, 1367 (Fed.Cir.2001)). However, if one " 'employs means-plus-function language in a claim, one must set forth in the specification an adequate disclosure showing what is meant by that language. If an applicant fails to set forth an adequate disclosure, the applicant has in effect failed to particularly point out and distinctly claim the invention as required by the second paragraph of section 112." *See* 35 U.S.C. § 112, ¶ 6." *Id.* (quoting *In Re Donaldson Co.*, 16 F.3d 1189, 1195 (Fed.Cir.1994) (en banc)).

Accordingly, when faced with means-plus-function limitations, courts "must turn to the written description of the patent to find the structure that corresponds to the means recited in the [limitations]." *Default*, 412 F.3d at 1298. " 'A structure disclosed in the specification qualifies as "corresponding" structure only if the specification or prosecution history clearly links or associates that structure to the function recited in the claim.' " *Id.* (quoting *B. Braun Med. v. Abbott Labs.*, 124 F.3d 1419, 1424 (Fed.Cir.1997)). "This duty to link or associate structure to function is the *quid pro quo* for the convenience of employing § 112, ¶ 6." *Id.* (citing *O.I.*

Corp. v. Tekmar Co., 115 F.3d 1576, 1583 (Fed.Cir.1997)). The question is "whether one skilled in the art would understand the specification itself to disclose the structure, not simply whether that person would be capable of implementing that structure." *Med. Instrumentation & Diagnostics Corp. v. Elekta AB,* 344 F.3d 1205, 1212 (Fed.Cir.2003).

ANALYSIS

Corresponding Structure for First and Second Switch Means

The ninth limitation claims a "first switch means" with a function of "connecting said dedicated memory address, data, and control circuits of said path configuring means to each of said first three sets of contacts." Claim Construction Opinion at 32. The tenth limitation claims a "second switch means" with a function of "connecting said dedicated memory address, data, and control lines of said path configuring means to said dedicated memory address, data, and control lines of said CPU respectively." *Id.* at 33.

Mitchell asserts that the corresponding structure for these functions is described at columns 19:64-20:5. This passage says:

> ***3** Each first switch means, second switch means, third switch means 108, fourth switch means 110, fifth switch means 112, sixth switch means 114, and seventh switch means 116, it is noted, actually represents a plurality of logical elements, each of which can logically disconnect an address, data, or control circuit that is mechanically connected to the switch means, under the control of the CPU 102 when power is being supplied to the BICPU microcomputer power circuits.

'154 patent, col. 19:64-20:5. This passage merely refers to a "plurality of logical elements." Even Mitchell himself recognized that a plurality of logical elements can refer to any number of combinations of elements and does not refer to a specific structure.[FN3] Dr. Patterson, Mitchell's expert, corroborated Mitchell's testimony regarding this issue.[FN4]

FN3. When asked in his deposition whether the patent described anywhere which of these thousands of "logical elements" should be used to build the first switch means, Mitchell responded "that leaves that up to the designers." Mitchell Depo. at 224:23-225:12. Mitchell further recognized that the switch means could be built in "almost as many different ways as there were design teams." *Id.*

FN4. When asked about how many possible combinations of circuits could provide this logical connection other than the tri-state device, Patterson responded "there is many other examples ... [t]here is, you got all the combinations of all kinds of things that can be. It can be a big number, I don't know." Patterson Depo. at 155:8-25.

At the hearing on this motion, the Court repeatedly asked Mitchell to identify a structure in the specification that corresponded to the functions.[FN5] Mitchell could only point to the language above and tell the Court that a person skilled in the art would know that a "plurality of logical elements" necessarily referred to tri-state circuitry. Notably, tri-state circuitry is never mentioned the language quoted above, nor does it appear anywhere in the specification.

FN5. The transcript from the hearing at p. 26-27 states:

> **THE COURT:** So what are you saying, though, is the structure and is it supported by the summary judgment proof; and if so where?
>
> **MR. SCHWARTZ:** Well, the structure has to do with the tri-state drivers. The

> tri-state drivers were known to those of ordinary skill in the art at the time this application-
>
> In response, Intel states:
>
> **MR. VAN NEST:** Your Honor, there isn't a word anywhere in the specification about a tri-state driver.

Mitchell argues that a person skilled in the art could read the function of limitations nine and ten and infer from the function that a tri-state circuitry device is *a* device that *could* perform the function. *See* Patterson Supplemental Decl. ISO Sur-Reply to MSJ of Invalidity, ¶ 14. The only authority Mitchell cited in the hearing to support this proposition was *Budde v. Harley-Davidson, Inc.* 250 F.3d 1369 (Fed.Cir.2001). In *Budde*, the Federal Circuit stated, "it is well settled that whether or not the specification adequately sets forth structure corresponding to the claimed function necessitates consideration of that disclosure from the viewpoint of one skilled in the art." *Id.* at 1376. While this is the law, the specification must disclose at least some kind of structure in the first place for this rule to apply. The law is clear: the corresponding structure must appear in the specification, and an expert cannot use his knowledge to select a structure that is capable of performing the recited function. *Atmel*, 198 F.3d at 1382 ("knowledge of one skilled in the particular art ... may only be employed in relation to structure that is disclosed in the specification."). This is the trade off for claiming as means-plus-function. The limitation must 'be construed to cover the corresponding structure ... described in the specification and equivalents thereof.' " 35 U.S.C. § 112, ¶ 6. *Braun Med.*, 124 F.3d at 1424. Therefore, *some* structure must be identified.

Following the hearing on this motion, where Mitchell was unable to articulate a structure, Mitchell filed its Notice of Record Cite and Supplemental Authority (Docket No. 191). Despite the repeated inquiries for Mitchell to identify a structure, even in its supplemental briefing, Mitchell could point to no more than the "logical element" language above. Mitchell reurges the proposition that "[o]ne skilled in the art would know that the logical element, each of which can logically connect or disconnect, is the recitation of the structure of the switch means" and that one skilled in the art would know from the "plurality of logical elements" language that the first and second switch means are tri-state devices. Mitchell's Notice of Record Cite and Supplemental Authority at 6-7. However, again no where in the specification do the phrases "tri-state devices" or "tri-state circuitry" appear.

***4** While tri-state devices may perform the recited functions, and one skilled in the art might know the function could be performed by a tri-state device, the patentee is limited to structures actually disclosed in the specification when the patentee claims as means-plus-function. *See Atmel*, 198 F.3d at 1382. Here, no structure is disclosed in the specification for this function.

Mitchell points to a printing error in the patent office that caused part of a sentence to be deleted in column 14:22. The sentence in the patent reads "[t]he buffers driving the"; and the rest of the sentence is cut off. '154 patent, Col. 14:22. Mitchell argues that in reviewing the prosecution history, it is clear that the sentence at one time read "[t]he buffers driving the data bus lines have full 'three-state' capability. This is necessitated by the fact that the lines are bi-directional." Mitchell's Notice of Record Cite and Supplemental Authority at 5. Mitchell argues that this language is specifically directed towards the "three-state" capability and supports a corresponding structure. *Id.*

Even if this sentence is directed toward tri-state circuitry, and it is debatable that even the complete version of the sentence would support a corresponding structure, at no time did Mitchell file a certificate of correction to remedy this omission. The law requires the structure to be set forth in the specification, not the prosecution history. *See* 35 U.S.C. § 112, ¶ 6. It is the patentee's responsibility to review and correct errors in the patent in a timely

fashion to avoid errors and omissions. *See Sw. Software, Inc. v. Harlequin, Inc.*, 226 F.3d 1280, 1296 (Fed.Cir.2000) ("Moreover, it does not seem to us to be asking too much to expect a patentee to check a patent when it is issued in order to determine whether it contains any errors that require the issuance of a certificate of correction."). The USPTO offers the certificate of correction procedure to cure just such defects so that patent owners can be assured that when the public views their patents, they view accurate representations of the claimed invention. *See id.* (In a case where the corresponding structure was not originally included in the patent, the Federal Circuit noted: "Until the PTO issues a certificate of correction pursuant to 35 U.S.C. § 254 adding the corresponding structure, such a claim would appear invalid to the public, and reasonable competitors would be justified in conducting their affairs accordingly.").

There is no reference to a structure in the specification to support the functions in limitations nine and ten as required by 35 U.S.C. § 112, ¶ 6; therefore, Claim 1 is invalid because it is indefinite.

Corresponding Structure for "means for causing"

The thirteenth and fourteenth limitations claim a "means for causing" with functions of "(1) [c]ausing said first and second switch means to remain in said non signal-conducting state upon application of power to said CPU power circuit and to assume a signal conductive state upon receipt of an appropriate signal from said CPU and (2)[a]ssum[ing] a non-signal conducting state upon receipt of an appropriate signal from said CPU." Claim Construction Opinion at 33. In identifying the corresponding structure to these functions at the *Markman* hearing, Intel proposed adopting Judge Illston's previous construction. Mitchell did not provide the Court with an alternative corresponding structure in its brief or argument; therefore, the Court adopted Judge Illston's structure and stated "[t]o the extent that any structure for the corresponding function of the thirteenth and fourteenth limitations is provided in the specification, that structure is described at col. 24:67-col. 25:56." *Id.* The passage at columns 24:67-25:56 contains no structure. Rather, as discussed below, even Mitchell recognizes that the passage describes the operation of the switch means, but does not disclose any structure.

***5** At the hearing, Mitchell referred the Court to a device called a MCS-6520 and said the device related to tri-state drivers. Hearing on Mot. Summary Judgment Tr. at 30. This device is discussed in column 15 and is completely outside the *Markman* ruling. '154 patent, Col. 15:42-55. Even if the Court considered the MCS-6520 as a possible structure, nothing in this part of the specification links the MCS-6520 with claim limitations thirteen and fourteen. FN6 The MCS-6520 is a chip comprised of various parts including drivers, but no driver is specifically detailed in the description at column 15. Intel argued, and Mitchell did not rebut the statement, that Mitchell is essentially saying that one skilled in the art would read the language at columns 24-25 and then look at the MCS-6520 as a whole and determine that somewhere in that chip is a tri-state device that is the structure for the functions of "means for causing." FN7 Federal Circuit precedent simply does not allow this reading of the patent to satisfy the § 112, ¶ 6 requirement. *See Atmel,* 198 F.3d at 1382. Mitchell could not identify any other possible corresponding structure at the hearing. FN8

FN6. The language reads:

> The MCS6520 is a direct pin for pin replacement for the Motorola MC6820 Peripheral Interface Adapter, the "PIA." As such, it meets all of the "PIA" electrical specifications and is totally hardware compatible with the MC6820.
>
> The MCS6520 is an I/O device which acts as an interface between the microprocessor and the peripherals such as printers, displays, keyboards, etc. The

> prime function of the MCS6520 is to respond to stimulus from each of the two worlds it is serving. On one side, the 6520 is interfacing with the peripherals via two eight-bit-bi-directional peripheral data ports. On the other side, the device interfaces with the microprocessor through an eight-bit data bus....”
>
> '154 patent, Col. 15:42-55.

FN7. **MR. VAN NEST:** What they are saying is you have to read this [Cols 24-25] and then go look at the 6520, which is a whole chip. It is not a switch or a buffer or a driver. It is a whole chip, Your Honor, with thousands and thousands of transistors. They are saying go look at this and somewhere in it you can find a tri-state driver and that is our structure.

> Hearing on Mot. Summary Judgment Tr. at 31.

FN8. Hearing transcript at p. 33:

> **THE COURT:** So what is the structure that one of ordinary skill in the art would have seen and linked up to the function?
>
> **MR. SCHWARTZ:** Yes, Your Honor. That is precisely the point that Mitchell has taken in this case. There is no specific detailed structure set out **in the specification.**

In its post-hearing-supplemental briefing, Mitchell seems to abandon the MCS-6520 argument and instead lays out the entire passage the Court set out in the *Markman* opinion FN9 and argues that the passage “is actually a description of the *operation* of the switch means.” Mitchell's Notice of Record Cite and Supplemental Authority at 8 (emphasis added). Thus, Mitchell's reasoning is the same as its argument for limitations nine and ten: this passage does not identify a specific structure, but one skilled in the art would know that the corresponding structure could be the control elements of the tri-state devices. *Id.* (“What is set forth above in Columns 24 and 25 to one skilled in the art is a description of how control is exerted on the control elements of the tri-state devices.”). Mitchell asserts that the “means for causing” is understood by one skilled in the art as a specific portion of the tri-state circuitry, which is the control element. *Id.* But again, there is no reference to tri-state circuitry, control elements, or any other structure in this passage.

FN9. The passage reads:

> Col. 24, line 67 to Col. 25, line 17:
>
> When power is removed from the BICPU microcomputer power circuits, a first switch means automatically, logically disconnects, and floats each connected circuit, and latches the first switch means in the logically disconnected position. Each logically disconnected and latched, floating, address circuit, data circuit and control circuit stays floating and logically disconnected and latched, when power is supplied to the BICPU microcomputer power circuits, until each first switch means is logically connected by signals from the BICPU microcomputer, after power is supplied to the BICPU microcomputer power circuits.
>
> A first switch means remains under control of the BICPU microcomputer, after power is supplied to the power circuits, and the BICPU microcomputer can logically disconnect and float, or logically connect, each of these circuits connected to a first switch means.
>
> Col. 25, lines 33-49:
>
> Each of these circuits contains a second switch means, similar in action to the first switch means, except the logically disconnected, floating, latched portion of

> the circuit, is connected to the CPU of the BICPU microcomputer. Each logically disconnected, floating, latched CPU address circuit, data circuit and control circuit, stays floating and disconnected and latched, when power is supplied to the BICPU microcomputer power circuits until each second switch means is logically connected, by signals from the BICPU microcomputer after power is supplied to the BICPU microcomputer power circuits.
>
> A second switch means remains under control of the BICPU microcomputer, after power is supplied to the power circuits,. and the BICPU microcomputer can logically disconnect or logically connect, each of the circuits connected to a second switch means.

Once again, there is no reference to a structure in the specification to support the functions in limitations thirteen and fourteen as required by 35 U.S.C. § 112, ¶ 6, thus Claim 1 must fail as invalid because it is indefinite.

CONCLUSION

Accordingly, Mitchell has failed to raise a fact issue as to whether limitations nine, ten, thirteen, and fourteen set forth corresponding structures for their functions as required by 35 U.S.C. § 112, ¶ 6. The Court holds that Claim 1 is indefinite and therefore invalid as a matter of law and **GRANTS** Intel's motion for summary judgment as to invalidity.

So ORDERED.

E.D.Tex.,2006.
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