249 Fed.Appx. 184, 2007 WL 2777968 (C.A.Fed.)
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This case was not selected for publication in the Federal Reporter.

Not for Publication in West's Federal Reporter See Fed. Rule of Appellate Procedure 32.1 generally governing citation of judicial decisions issued on or after Jan. 1, 2007. See also Federal Circuit Rule 32.1 and Federal Circuit Local Rule 32.1. (Find CTAF Rule 32.1)

United States Court of Appeals,
Federal Circuit.
MAURICE MITCHELL INNOVATIONS, L.P.,
Plaintiff-Appellant,
v.
INTEL CORPORATION, Defendant-Appellee.
No. 2007-1108.

Sept. 24, 2007.
Rehearing and Rehearing En Banc Denied Nov. 5, 2007.[FN*]

FN* Circuit Judge Schall did not participate in the vote.

***184** Appealed from United States District Court for the Eastern District of Texas, Leonard Davis, Judge.
Richard L. Schwartz, Whitaker, Chalk, Swindle & Sawyer, L.L.P., of Fort Worth, TX, argued for plaintiff-appellant. Of counsel on the brief was Manny D. Pokotilow, Caesar, Rivise, Bernstein, Cohen & Pokotilow, Ltd., of Philadelphia, PA.

Robert A. Van Nest, Keker & Van Nest LLP, of San Francisco, CA, argued for defendant-appellee. With him on the brief were Christa M. Anderson and Steven A. Hirsch.

Before RADER, MOORE, Circuit Judges, and YEAKEL, District Judge[FN**].

FN** Honorable Lee Yeakel, District Judge, United States District Court for the Western District of Texas, sitting by designation.

RADER, Circuit Judge.

****1** The United States District Court for the Eastern District of Texas granted Intel Corporation's ("Intel") motion for summary judgment that claim 1 of U.S. Patent No. 4,875,154 ("the '154 patent") is invalid as indefinite pursuant to 35 U.S.C. § 112, ¶ 2. *Maurice Mitchell Innovations, L.P. v. Intel Corp.*, No. 2:04-CV-450 (E.D.Tex. ***185** Dec. 11, 2006) ("*Final Judgment*"); *Maurice Mitchell Innovations, L.P. v. Intel Corp.*, No. 2:04-CV-450, 2006 WL 3447632 (E.D.Tex Nov. 22, 2006) ("*Opinion*"); *Maurice Mitchell Innovations, L.P. v. Intel Corp.*, No. 2:04-CV-450, 2006 WL 1751779 (E.D.Tex. Jun. 21, 2006) ("*Claim Construction Opinion*"). Because the district court correctly construed the claim term "means for causing" as a means-plus-function limitation under 35 U.S.C. § 112, ¶ 6 and correctly found the specification did not contain any corresponding structure, this court affirms.

I

The United States Patent and Trademark Office issued the '154 patent, entitled Microcomputer with Disconnected, Open, Independent, Bimemory Architecture, Allowing Large Interacting, Interconnected Multi-microcomputer Parallel Systems Accomodating [sic] Multiple Levels of Programmer Defined Heirarchy [sic], on October 17, 1989 from an application filed on June 12, 1987. The patent abstract states:

> A Bimemory Independent CPU (BICPU) microcomputer which is comprised of a known CPU chip provided with additional circuitry to enable CPU to interact in a multi BICPU microcomputer system. Each BICPU microcomputer in a system

> is supplied with an assigned standard memory mechanically and logically connected to it's [sic] BICPU's "A" bus circuits. The BICPU microcomputer is also provided with connectors enabling the CPU to be connected to system buses. Any number of BICPU microcomputers can be logically chained, linked and treed in a simple logical bimemory independent pattern infinitely in as many dimensions as is reasonably desired, using one standard set of dedicated, simple, single line conductors (system buses) to mechanically interconnect any "B" or "C" bus curcuits [sic] of two different BICPU microcomputers.

'154 Patent Abstract. Generally, the patent describes a BICPU computer system "comprised of a known CPU chip with additional circuitry to enable the CPU to interact in a multi BICPU microcomputer system." '154 Patent col.7 ll.3-6. According to the specification, the invention allows "[a]ny number of BICPU microcomputers [to] be logically chained, linked and treed in a simple logical bimemory independent pattern infinitely in as many dimensions as is reasonably desired, using one standard set of dedicated, simple, single line conductors (system buses) to mechanically interconnect any 'B' or 'C' bus circuits of two different BICPU microcomputers." '154 Patent col.7 ll.12-19. Claim 1 reads:

A microcomputer data processing apparatus, comprising:

[1] a Central Processing Unit (CPU),

[2] *a path configuring means,*

[3] path control circuits connecting said CPU to said *path configuring means,*

****2** [4] a plurality of contacts comprised of a plurality of distinct sets,

[5] wherein said CPU further comprises a dedicated memory address circuit, a dedicated memory data circuit, a dedicated memory control circuit and a dedicated power circuit,

[6] wherein said *path configuring means* further comprises a dedicated memory address circuit, a dedicated memory data circuit and a dedicated memory control circuit,

[7] wherein each dedicated memory address, data, and control circuit includes a plurality of dedicated ***186** memory address, data, and control lines respectively, wherein

[8] said memory control lines are comprised of a read/write line, timing lines and status lines,

[9] first *switch means* comprised of at least three distinct parts of connecting said dedicated memory address, data, and control circuits of said *path configuring means* to each of said first three sets of contacts, and

[10] second *switch means* for connecting said dedicated memory address, data, and control lines of said *path configuring means* to said dedicated memory address, data, and control lines of said CPU respectively,

[11] wherein said first and second *switch means* assume a non signal-conducting state when said CPU power circuit is not supplied with power,

[12] wherein said lines of said CPU an said contacts assume a non-signal conducting state when said first and second *switch means* are in said non-signal conducting state,

[13] *means for causing* said first and second *switch means* to remain in said non signal-conducting state upon application of power to said CPU power circuit and to assume a signal-conductive state upon receipt of an appropriate signal from said CPU, and to

[14] assume a non signal-conducting state upon receipt of an appropriate signal from said CPU.

'154 Patent col.90 l.59-col.91 l.37 (emphases and [limitation numbers] added).

Maurice Mitchell Innovations, L.P. ("Mitchell") brought suit against Intel in the United State District Court for the Eastern District of Texas alleging a number of Intel's products infringe Claim 1 of the '154 patent. In construing the claims, the district court adopted the claim construction of District Judge Susan Illston of the United States District Court for the Northern District of California. *Claim Construction Opinion; see, Maurice Mitchell v. Samsung Electronics Co., Ltd.*, No. C 01-0295 SI (N.D.Cal. Jan. 29, 2002). Specifically, the district court construed "first switch means," "second switch means," and "means for causing" as means-plus-function limitations governed by 35 U.S.C. § 112, ¶ 6. *Id.* The district court then determined that the '154 patent specification did not disclose structure for the "switch means" limitations and the "means for causing" limitation. *Opinion.* As a result, the district court found Claim 1 of the '154 patent indefinite and therefore invalid as a matter of law. *Id.*

II

****3** This court reviews a district court's grant of summary judgment without deference, drawing all justifiable inferences in favor of the nonmovant. *Genentech, Inc. v. Amgen, Inc.*, 289 F.3d 761, 767 (Fed.Cir.2002). Claim construction is a matter of law that this court reviews without deference. *Cybor Corp. v. FAS Techs., Inc.*, 138 F.3d 1448, 1456 (Fed.Cir.1998) (en banc); *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed.Cir.1995), *aff'd*, 517 U.S. 370, 116 S.Ct. 1384, 134 L.Ed.2d 577 (1996). "The review of indefiniteness under 35 U.S.C. § 112, paragraph 2, proceeds as a question of law without deference." *SmithKline Beecham Corp. v. Apotex Corp.*, 403 F.3d 1331, 1338 (Fed.Cir.2005).

"A patent issued from the United States Patent and Trademark Office (PTO) bears the presumption of validity under 35 U.S.C. § 282. An accused infringer, therefore,***187** must prove patent invalidity under the clear and convincing evidentiary standard." *Metabolite Labs., Inc. v. Lab. Corp. of Am. Holdings*, 370 F.3d 1354, 1365 (Fed.Cir.2004). Specifically, "[t]he claims as granted are accompanied by a presumption of validity based on compliance with, inter alia, § 112 ¶ 2." *S3 Inc. v. NVIDIA Corp.*, 259 F.3d 1364, 1367 (Fed.Cir.2001).

As stated in § 112 ¶ 2, "[t]he specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention." Claims "particularly point[ ] out and distinctly claim[ ]" the invention when one of ordinary skill in the art would understand the scope of the invention when the claims are read in conjunction with the specification. *Default Proof Credit Card Sys., Inc. v. Home Depot U.S.A., Inc.*, 412 F.3d 1291, 1298 (Fed.Cir.2005); 35 U.S.C. § 112 ¶ 2. But, if an applicant "employs means-plus-function language in a claim, one must set forth in the specification an adequate disclosure showing what is meant by that language." *In re Donaldson*, 16 F.3d 1189, 1195 (Fed.Cir.1994) (en banc); 35 U.S.C. § 112 ¶ 6. Therefore, "[i]f there is no structure in the specification corresponding to the means-plus-function limitation in the claims, the claim will be found invalid as indefinite." *Biomedino, LLC v. Waters Technologies Corp.*, 490 F.3d 946, 950 (Fed.Cir.2007).

III

The district court found that "means for causing" was a means-plus-function limitation without any descriptive corresponding structure within the specification. The only possible structure corresponding to the claimed function appears at Col.24 l.67 to Col.25 l. 56. *Opinion*, slip op. at 8. The district court then determined this passage did not contain any structure.

As illustrated by the claim language in limitation 13, the "means for causing" controls the first and second switch means. In other words, the "means

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for causing" would need a structure (i.e., device or driver) to control the function of the switch means. Mitchell contends that the '154 patent specification contains an adequate disclosure corresponding to the "means for causing" limitation to satisfy § 112 ¶ 2. Mitchell argues that the district court incorrectly limited the corresponding structure to the disclosure at Col.24 l.67 to Col.25 l.56 when the following additional passages also disclose structure: Col.15, ll.40-56; Col.19, line 34 to Col.20, line 5; Col.13, ll.11-19; Col.7, ll.37-44; Col.44, ll.21-46; Col.89, ll.14-49; Col.90, ll.16-30; and Col.16, ll.48-53.

****4** Like the district court, however, this court discerns little, if any, structure for "means for causing" in the specification and no disclosed link between that purported structure and the claimed function. This court also credits the district court's finding that Mitchell's counsel admitted during the summary judgment hearing that the Col.24 l.67 to Col.25 l.56 passage does not include any structure linked to the claimed function. *Maurice Mitchell Innovations v. Intel Corp.*, 2:04cv450, slip op. at 35 (E.D.Tex. Sept. 28, 2006) (Transcript of Pretrial and Motion Hearing). Beyond that passage, however, this court finds no specific structure disclosed anywhere in the specification to carry out the "means for causing" function.

Mitchell also offers another source of structure for the claimed means. The specification refers to the MCS6520 Peripheral Interface Adaptor ("PIA"). ' 154 Patent col.15 ll.40-55. The MCS6520 is a complex integrated circuit (i.e., chip) containing numerous individual circuits which ***188** functions as an interface between a microprocessor and peripheral devices such as printers, displays and the like. Mitchell contends that the MCS6520 contains tri-state circuitry or tri-state drivers and that a person of ordinary skill in the art would understand the tri-state structure in the MCS6520 to be capable of performing the "means for causing" function.

While the MCS6520 may contain tri-state or driver type circuits, the specification does not identify the tri-state circuits in the MCS6520 as the structure to carry out the "means for causing" limitation. The mere mention of a complicated integrated circuit, comprised of hundreds if not thousands of circuits, is much too broad to sufficiently indicate the precise "means for causing" structure to a person of ordinary skill in the art. *See Med. Instrumentation & Diagnostics Corp. v. Elekta AB*, 344 F.3d 1205, 1212 (Fed.Cir.2003) ("It is important to determine whether one of skill in the art would understand the specification itself to disclose the structure, not simply whether that person would be capable of implementing that structure."). In other words, as the district court noted, the MCS6520 is both too broad and not linked to the "means for causing" limitation. *Opinion*, slip op. at 8-9.

Mitchell also attempts to identify structure in a variety of generalized passages in the specification. This court has examined these passages and finds no specific structure. Mitchell only states that "[t]hese passages are additional disclosures of the details of the structure, readily apparent to a person of ordinary skill in the art." In effect, Mitchell merely references various passages in the specification without providing any information to show structure corresponding to "means for causing." Mitchell appears to be arguing that a person of ordinary skill in the art would be able to ascertain the corresponding structure by combining a variety of passages in the specification with their knowledge of the art. However, "in order for a claim to meet the particularity requirement of ¶ 2, the corresponding structure(s) of a means-plus-function limitation must be disclosed in the written description in such a manner that one skilled in the art will know and understand what structure corresponds to the means limitation." *Atmel Corp. v. Info. Storage Devices, Inc.*, 198 F.3d 1374, 1382 (Fed.Cir.1999). Thus, the statute requires more than just the possibility that an artisan of ordinary skill may be able to figure out the corresponding structure. The quid pro quo for using a means-plus-function limitation requires specificity in reciting structure and linking that structure to the limitation. *Id.* Mitchell does not carry

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out its part of the quid pro quo bargain. This court sustains the finding that claim 1 is indefinite under U.S.C. § 112, ¶ 2.

****5** This court need not reach the "switch means" and "path configuring means" limitations because the district court's decision can be affirmed solely on the "means for causing" limitation.

IV

Because the district court correctly construed the claim term "means for causing" as a means-plus-function limitation under 35 U.S.C. § 112, ¶ 6 and correctly found the specification did not contain any corresponding structure for this limitation, this court affirms.

AFFIRMED

COSTS

Each party shall bear its own costs.

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