Aloft's Exhibit A

REQUEST FOR CONTINUED EXAMINATION (RCE) TRANSMITTAL

Address to:
Mail Stop RCE
Commissioner for Patents
P.O. 1450
Alexandria, VA 22313-1450

Application No.	10/658,612
Filing Date	September 8, 2003
First Named Inventor	Gopalan Ramanujam
Art Unit	2193
Examiner Name	Mai, Tan V.
Attorney Docket Number	42P14609
Confirmation Number	2531

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.

Request for Continued Examination (RCE) practice under 37 CFR § 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application.

1. **Submission required under 37 CFR 1.114** Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

a. ☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

i. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on ____

ii. ☐ Other _____

b. ☒ Enclosed

i. ☒ Amendment/Reply

ii. ☐ Affidavit(s)/Declaration(s)

iii. ☐ Information Disclosure Statement (IDS)

iv. ☐ Other _____

2. **Miscellaneous**

a. ☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months. (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

b. ☐ Other _____

3. **Fees** The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

a. ☒ The Director is hereby authorized to charge the following fees, any underpayment of fees, or credit any overpayments, to Deposit Account No. 02-2666.

i. ☒ RCE fee required under 37 CFR 1.17(e)

ii. ☐ Extension of time fee (37 CFR 1.136 and 1.17)

iii. ☐ Other: ($.00) _____

b. ☐ Check in the amount of $810.00 enclosed

c. ☐ Payment by credit card (Form PTO-2038 enclosed)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Signature	Brent E. Vecchia	Date	September 10, 2010
Name *(Print/Type)*	Brent E. Vecchia, 48,011	*Registration No. (Attorney/Agent)*	48,011

CERTIFICATE OF MAILING OR TRANSMISSION

This Request for Continued Examination is being submitted electronically to the United States Patent and Trademark Office via EFS-Web on **September 10, 2010**

Name *(Print/Type)*	Shannon Serrano		
Signature	Shannon Serrano	Date	September 10, 2010

Based on PTO/SB/30 (04-05) as modified by Blakely, Sokoloff, Taylor & Zafman (wlr) 06/15/2007.
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application. No.	: 10/658,612	Confirmation No.	: 2531
1st Named Inventor	: Ramanujam	Art Unit	: 2193
Filed	: September 8, 2003	Examiner	: Mai, Tan V.
Docket No.	: 42390.P14609	Customer No.	: 45209

PRELIMINARY AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Prior to examination of the present RCE application, Applicants respectfully request that the Examiner enter the following amendments and consider the following remarks.

CERTIFICATE OF SUBMISSION/TRANSMISSION (37 CFR 1.8A)

I hereby certify that this correspondence is, on the date shown below, being:

EFS WEB

✔ *submitted electronically via EFS Web to the Patent and Trademark Office.*

FACSIMILE

☐ *transmitted by facsimile to the Patent and Trademark Office.*

Shannon Serrano 9/10/10

Shannon Serrano *Date*

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) An apparatus comprising:

a destination storage location corresponding to a first architectural register;

~~a functional~~ an execution unit having circuitry to process a packed format values by converting, responsive to a control signal, a first packed first format value in a first format selected from a first plurality of packed first format values in the first format to a first plurality of second format values, said first packed first format value having a plurality of sub elements each having a first number of bits, each of the first plurality of second format values being a number represented in a second format and having a second number of bits which is greater than the first number of bits, said ~~functional~~ execution unit to store all of said first plurality of second format values into said first architectural register.

2. (Original) The apparatus of claim 1 wherein the second number of bits is a power-of-two multiple of the first number of bits.

3. (Original) The apparatus of claim 2 wherein a source specifier is to specify either a second architectural register or a memory location as a source storage location and further wherein a destination specifier is to specify the first architectural register as the destination storage location.

4. (Original) The apparatus of claim 3 wherein said first format is an integer format and wherein said second format is a floating point format.

5. (Original) The apparatus of claim 4 further comprising:

a decoder to receive a single convert instruction, said decoder to generate said control signal in response to the single convert instruction.

6. (Currently Amended) The apparatus of claim 1 wherein said ~~functional~~ execution unit chooses one of said first plurality of packed first format values to convert based on an immediate operand value.

7. (Original) The apparatus of claim 5 wherein an opcode portion of said single convert instruction specifies which of said first plurality of packed first format values to convert.

8. (Original) The apparatus of claim 5 wherein said control signal comprises a micro operation generated by the decoder in response to the single convert instruction.

9. (Original) The apparatus of claim 5 further comprising a register renaming circuit, wherein said source storage location and said destination storage location are physical registers that each have a correspondence to an architectural register, said correspondence being tracked by the register renaming circuit.

10. (Original) The apparatus of claim 9 wherein said single convert instruction comprises an opcode and an operand specifier, wherein the operand specifier is in a MOD R/M format.

11. (Original) The apparatus of claim 9 wherein said first plurality of packed first format values are N bit integer values and wherein said first packed first format value is an N bit integer value, wherein said plurality of sub elements is M sub elements and wherein each of the M sub elements has N/M bits, and further wherein each of the first plurality of second format values is an N-bit floating point result.

12. (Currently Amended) The apparatus of claim 1 further comprising a second destination storage location, wherein said ~~functional~~ execution unit is further responsive to a second control signal to convert a second plurality of second format values in the second format having the second number of bits to a second first format value and to store the second first format value in one of a plurality of packed first format value positions in said second destination storage location, wherein said second first format value comprises saturated representations of the second plurality of second format values in the first format.

13. (Original) The apparatus of claim 3 wherein said first architectural register and said second architectural register are part of a first group of architectural registers, the first group of architectural registers having a first size.

14. (Original) The apparatus of claim 12 wherein first architectural register and said second destination storage location are registers in a group of xmm registers.

15. (Currently Amended) An apparatus comprising:

a decoder to receive a first instruction and to decode said first instruction into a control signal;

~~a functional~~ an execution unit coupled to the decoder the execution unit having circuitry to receive the control signal, the ~~functional~~ execution unit to responsively process a plurality of floating point values value by converting convert a first plurality of floating point values in a first floating point format having a first number of bits into a first integer value comprising a plurality of sub elements each having a second number of bits less than the first number of bits and to store said first integer value in a first position in a first register, the first register being capable of storing a plurality of integer values in a plurality of individually accessible positions.

16. (Currently Amended) The apparatus of claim 15 wherein said first instruction comprises an opcode, a first operand specifier, an immediate operand, and a second operand specifier, wherein the first operand specifier specifies a source from which the ~~functional~~ execution unit is to retrieve the first plurality of floating point numbers, the second operand specifier specifies the first register from a plurality of registers, and wherein the immediate operand specifies one of a plurality of locations in the first register in which the first integer value is to be stored.

17. (Currently Amended) The apparatus of claim 16 wherein said decoder is to decode a second instruction and to responsively generate a second signal, and wherein said ~~functional~~ execution unit, responsive to said second signal, is to convert a second integer value to a second plurality of floating point values in the first floating point format and to store said second plurality of floating point values into a second register.

18. (Original) The apparatus of claim 17 wherein said first register and said second register are part of a first group of architectural registers, and further wherein said plurality of sub elements comprise saturated representations of said first plurality of floating point values.

19. (Original) The apparatus of claim 18 wherein a second immediate operand is to specify one location of a second plurality of locations within a register from which to retrieve the second integer value.

20. (Currently Amended) A method comprising:

a module fetching a first instruction that specifies a location of a first format value in a first format among a plurality of first format values of a packed data, the first format value having a plurality of sub elements each sub element having a first number of bits;

~~a functional~~ an execution unit processing the first format value by converting the first format value to a first plurality of second format values in a second format with circuitry, each of the first plurality of second format values having second format and corresponding to one of the plurality of sub elements, the second format having a multiple of the first number of bits;

storing the first plurality of second format values into a first register.

21. (Original) The method of claim 20 wherein said location is a second register, wherein said first register and said second register are registers in a single group of architectural registers.

22. (Original) The method of claim 21 further comprising:

fetching a second instruction that specifies a second location of a second plurality of second format values in the second format;

converting the second plurality of second format values to a second first format value;

storing the second first format value in a third register, wherein the third register is also in the single group of architectural registers.

23. (Original) The method of claim 22 further comprising:

specifying which of the plurality of first format values to convert by an immediate operand;

specifying one a plurality of destination packed data positions for the second first format value with a second immediate operand.

24. (Original) The method of claim 22 wherein said first format is an integer format and wherein said second format is a floating point format.

25. (Original) The method of claim 24 further comprising:

saturating each of the second plurality of second format values to generate a plurality of clamped sub elements of the second first format value.

26. (Original) A system comprising:

a memory to store a first instruction and an image processing sequence that operates on image data in a second format;

a processor coupled to the memory to process a first operand comprising a plurality of packed integer data values according to the first instruction by converting one of the plurality of packed integer data values into a first plurality of values in a second format and to store said first plurality of values in the second format into a register corresponding to an architectural register, said first plurality of values in the second format being manipulated as part of an image by said image processing sequence;

a graphics interface coupled to the processor to receive graphical data representative of the image from said processor;

a display to display said image.

27. (Original) The system of claim 26 wherein said first plurality of values in said second format have a larger total number of bits than said one of said plurality of packed integer data values.

28. (Original) The system of claim 26 wherein said memory stores a second instruction to cause the processor to convert a second plurality of values in the second

format which are a result of manipulation of said first plurality of values in the second format by said image processing sequence into a second integer data value and to store the second integer data value to a second register corresponding to a second architectural register, and further wherein said second integer data value is written to the graphics interface as a pixel value.

29. (Original) The system of claim 28 wherein said first instruction is a first convert instruction, wherein each of the plurality of packed integer data values has a plurality of sub elements each having a first number of bits and wherein each of the first plurality of values corresponds to one of the plurality of sub elements and has a first floating point format having a multiple of the first number of bits.

30. (Original) The system of claim 26 wherein said first instruction specifies a first one of the plurality of packed integer data values, and wherein said plurality of packed integer data values comprises N integer data values, wherein the memory stores N convert instructions including the first instruction to convert the N integer data values into a set of N pluralities of floating point values.

31. (Original) The system of claim 30 wherein said image processing sequence is to operate on said set of N pluralities of floating point values to generate a second N pluralities of floating point values as a portion of the image, and further wherein said memory stores a second plurality of N convert instructions to convert each of second N pluralities of floating point values back to integer data values in a packed format.

32. (Currently Amended) A tangible machine readable medium storing ~~carrying~~ an instruction, which if executed by a machine, causes the machine to perform the operations of:

converting with an arithmetic logic unit an integer value, the integer value being among a plurality of integer values of a packed data and having a first integer format having a plurality of sub elements each having a first number of bits, to a plurality of floating point values, each of the plurality of floating point values having a first floating point format, the first floating point format having a multiple of the first number of bits;

storing the plurality of floating point values into a first register, wherein the tangible machine readable medium is one of a memory, a magnetic storage disc, and an optical storage disc.

33. (Original) The machine readable medium of claim 32, wherein said machine readable medium further stores one or more additional instructions, which if executed by the machine, cause the machine to perform:

converting a second plurality of floating point values in the first floating point format to a second integer value in the first integer format;

storing the second integer value in a third register, wherein the third register is also in the group of architectural registers and is capable of storing a plurality of integer values in the first integer format.

REMARKS

The Applicants respectfully request reconsideration of this application in view of the above amendments and the following remarks.

35 U.S.C. § 101 Rejection

Claims 1-25 and 32-33 are rejected under 35 U.S.C. § 101 because the claimed invention is allegedly directed to non-statutory subject matter.

Applicants respectfully submit that independent claims 1, 15, and 32 have been amended to overcome the rejection.

For example, claim 1 has been amended to recite "***an execution unit*** *having* ***circuitry*** *to process a packed format values by converting, responsive to a control signal, ...*" An apparatus including an execution unit having circuitry to process a packed format value responsive to a control signal is believed to be statutory subject matter.

Similarly, independent claims 15 and 32, and their dependent claims, are believed to be directed to statutory subject matter.

Accordingly, Applicants respectfully request that the rejection of claims 1-25 and 32-33 be withdrawn.

Conclusion

In view of the foregoing, it is believed that all claims now pending patentably define the subject invention over the prior art of record and are in condition for allowance. Applicants respectfully request that the rejections be withdrawn and the claims be allowed at the earliest possible date.

Request For Telephone Interview

The Examiner is invited to call Brent E. Vecchia at (303) 740-1980 if there remains any issue with allowance of the case.

Request For An Extension Of Time

The Applicants respectfully petition for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17 for such an extension.

Charge Our Deposit Account

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: September 10, 2010

By Brent E. Vecchia

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