EXHIBIT L

2009 WL 1134839 (Bd.Pat.App. & Interf.)

Board of Patent Appeals and Interferences
Patent and Trademark Office (P.T.O.)

***1** Ex Parte Jonathan E. Greene

Appeal 2008-4073
Application 10/643,164 Technology Center 2100

Decided:
[FN1]

April 24, 2009

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Before LEE E. BARRETT, LANCE LEONARD BARRY, and ST. JOHN COURTENAY III
Administrative Patent Judges
COURTENAY
Administrative Patent Judge

DECISION ON APPEAL

STATEMENT OF THE CASE

This is a decision on appeal under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 60 and 61. Claims 1-59 have been cancelled.[FN2] We have jurisdiction under 35 U.S.C. § 6(b).

We AFFIRM.

INVENTION

The invention on appeal is directed generally to methods and an apparatus that improve on existing Fast Fourier Transform (FFT) calculations. More particularly, Appellant's invention provides a multistage FFT calculation in which the final stage is characterized by two processing loops that store the outputs of butterfly calculations in a shuffled order that results in the FFT outputs being correctly ordered with no need to perform an additional bit-reversal ordering pass. (Spec. 5).

CLAIMS ON APPEAL

For convenience, claims 60 and 61 are reproduced here:

60. A computer system for performing a fast Fourier transform on N ordered inputs in n stages comprising:
one or more vector processors configured as a non-final stage calculating means for repetitively performing in-place butterfly calculations for n-1 stages;
the one or more vector processors further configured as a final stage calculating means for performing a final stage of butterfly calculations including:
a first loop means for performing a portion of the final stage butterfly calculations, the first loop means performing a set of butterfly calculations, and storing butterfly calculation outputs in shuffled order in place of the selected inputs to result in a correct ordering of transform outputs; and
a second loop means for performing a remaining portion of the final stage butterfly calculations, the second loop means performing two sets of butterfly calculations, and storing butterfly calculation outputs from a first one of the two sets of butterfly calculations in shuffled order in place of the inputs selected for a second one of the two sets of butterfly calculations and storing butterfly calculation outputs from the second one of the two sets of butterfly calculations in shuffled order in place of the inputs selected for the first one of the two sets of butterfly calculations to result in a correct ordering of transform outputs,
wherein the final stage calculating means performs all butterfly calculations as radix-4 butterflies having four inputs and four outputs, wherein N is a power of two, and wherein the non-final stage calculating means performs a first stage of radix-8 butterfly calculations followed by n-2 stages of radix-4 butterfly calculations,
***2** wherein the computer system produces the correct ordering of transform outputs with no need to perform an additional bit-reversal ordering pass.

61. The computer system of claim 60, wherein the non-final and final stage calculating means include a four-fold single instruction multiple data (SIMD) processor for performing four radix-4 butterfly calculations at a time.

THE REJECTION

Claims 60 and 61 stand rejected under 35 U.S.C. § 101 as being directed to non-statutory subject matter.

APPELLANT'S CONTENTIONS

Appellant contends that "[a] claim is statutory if it provides a 'useful, concrete, and tangible result,' even if that result is merely a set of numbers," citing *State St. Bank & Trust Co. v. Signature Fin. Group*, 149 F.3d 1368, 1375 (Fed. Cir. 1998) which further cites *In re Alappat*, 33 F.3d 1526, 1544 (Fed. Cir. 1994) (App. Br. 10). Appellant reasons that since "[c]laim 60 recites a computer system that uses hardware components (i.e., vector processors) to generate a series of values (i.e., butterfly calculation outputs) representing values of coefficients, without need for additional processing (i.e., an additional bit-reversal ordering pass)" that this compares favorably, from the perspective of 35 U.S.C. § 101, with claims that the Court found patentable in *Alappat; Arrhythmia Research Technology Inc. v. Corazonix Corp.*, 958 F.2d 1053, 1033 (Fed. Cir. 1992); and, *State St. Bank & Trust Co.* (App. Br. 10).

Appellant further contends that each time the claimed invention is used, it produces ordered transform outputs. Therefore the result is tangible as it is a "real world" result in the form of outputs that are ordered. Appellant also avers that the results of the instant invention are useful in that the ordered outputs are specific, substantial, and credible, where the ordering of the outputs allows them to used [without] any additional post-processing of the outputs, as described in the Applicant's Specification on page 5. (App. Br. 13).

Appellant further contends that claim 60 is directed to statutory subject matter because the claim identifies a physical structure in terms of hardware or hardware and software. Specifically, Appellant states that claim 60 "defines a computer system that includes specific hardware structures, namely, vector processors. Moreover, it defines those structures in connection with *means,* (implemented in software) namely, the *first loop means, second loop means,*

non-final stage calculating means, and final stage calculating means that are implemented, in the specification, in software." (App. Br. 13-14).

***3** In the Reply Brief, Appellant restates that the results of the FFT are tangible as they are "real world results" in the "form of ordered outputs that can be used without any additional post-processing, as described in Appellant's specification on page 5." (Reply Br. 3).

EXAMINER'S RESPONSE

The Examiner states that claims 60 and 61 stand rejected under 35 U.S.C. § 101 because they claim one or more vector processors for performing a FFT (i.e., mathematical algorithm) that fail to produce a specific practical physical application or useful, concrete, and tangible result. The Examiner reasons that without a specific practical physical application or useful, concrete, and tangible result, claim 60 appears to preempt every substantial practical application of the idea embodied within the claim (i.e., a FFT) (Ans. 5-6). The Examiner also concludes that claim 60 is non-statutory because the claimed vector processors are configured to perform a set of calculations by software subroutines and the claim does not disclose any particular hardware for performing a FFT, but rather merely a general vector processor. (Ans. 6).

ISSUE

Has Appellant shown the Examiner erred in concluding that claims 60 and 61 are directed to non statutory subject matter under 35 U.S.C. § 101?

PRINCIPLES OF LAW

Fundamental principles, such as "laws of nature, natural phenomena, and abstract ideas," are not patent eligible. *In re Bilski*, 545 F.3d 943, 952 (Fed. Cir. 2008) ("Specifically, the Court has held that a claim is not a patent-eligible 'process' if it claims 'laws of nature, natural phenomena, [or] abstract ideas. Such fundamental principles are 'part of the storehouse of knowledge of all men … free to all men and reserved exclusively to none.'" (Citations omitted.)).

In determining whether an applicant is seeking to claim an unpatentable fundamental principle or a patent eligible application of the fundamental principle, the inquiry is whether the claim preempts substantially all uses of that fundamental principle. *Id.* at 953 "[*Diamond v. Diehr*, 450 U.S. 175 (1981)] can be understood to suggest that whether a claim is drawn only to a fundamental principle is essentially an inquiry into the scope of that exclusion; i.e., whether the effect of allowing the claim would be to allow the patentee to pre-empt substantially all uses of that fundamental principle. If so, the claim is not drawn to patent-eligible subject matter."); *Bilski*, 545 F.3d at 954 (The Supreme Court stated in *Gottschalk v. Benson*, 409 U.S. 63 (1972) that "the patent would wholly pre-empt the mathematical formula and in practical effect would be a patent on the algorithm itself."). The Federal Circuit stated: "The question before us then is whether Applicants' claim recites a fundamental principle and, if so, whether it would pre-empt substantially all uses of that fundamental principles if allowed." *Bilski*, 545 F.3d at 954.

FINDINGS OF FACT

***4** In our analysis *infra*, we rely on the following findings of fact (FF) that are supported by a preponderance of the evidence:

APPELLANT'S SPECIFICATION

1. Appellant's Specification discloses that "[t]he FFT method of the invention can be implemented in any man-

ner in which its logic can practically be carried out." (Spec. 16, ll. 9-10).
2. Appellant's Specification discloses that "[t]he method can be embodied in software that can run on a variety of computers known in the art, including *without limitation*, personal computers, workstation computers, and supercomputers known in the art." (Spec. 16, ll. 10-12, emphasis added).
3. Appellant's Specification discloses that "[i]n one preferred embodiment, the FFT method of the invention is implemented in software and executed on a computer having one or more vector processors such as the PowerPC® G4® processor having AltiVec® technology." (Spec. 16, ll. 12-15).
4. Appellant's Specification discloses that "[a]n example of computer code useful for programming such a computer to carry out the method of the invention is included in United States Patent Application Serial No. 60/168,027, from which this application claims priority, and which is incorporated by reference into this disclosure." (Spec. 16, ll. 15-18).
5. Appellant's Specification discloses that "[i]n addition, the logic of the FFT method of the invention can be implemented in a special purpose circuit, such as a circuit including ASICs having the specific logic employed herein deployed within the circuit, or in a system that combines such special purpose circuits with a general purpose computer with software." (Spec. 16, ll. 18-22).

APPELLANT'S PRINCIPAL BRIEF

6. Appellant states that

> [c]laim 60 comports with the above guideline as it defines a computer system that includes specific hardware structures, namely, vector processors. Moreover, it defines those structures in connection with means (implemented in software), namely, the first loop means, second loop means, non-final stage calculating means, and final stage calculating means that are implemented, in the specification, in software.

(App. Br. 13-14).

ANALYSIS

We decide the question of whether Appellant has shown the Examiner erred in concluding that claims 60 and 61 are directed to non-statutory subject matter under 35 U.S.C. § 101.

Appellant's principal contention is that "[a] claim is statutory if it provides a 'useful, concrete, and tangible result,' even if that result is merely a set of numbers," citing *State St. Bank & Trust Co.* 149 F.3d at 1375; *In re Alappat*, 33 F.3d at 1544 (App. Br. 10).

***5** In response, we note that our reviewing court recently determined that the "useful, concrete, and tangible result" test associated with *State Street Bank & Trust Co. v. Signature Financial Group, Inc.*, 149 F.3d 1368, 1373 (Fed. Cir. 1998) is inadequate. *See In re Bilski*, 545 F.3d at 959-960 ("Therefore, we also conclude that the 'useful, concrete and tangible result' inquiry is inadequate and reaffirm that the machine-or-transformation test outlined by the Supreme Court is the proper test to apply."). Therefore, we find Appellant's argument unavailing that claims 60 and 61 are directed to statutory subject matter because the transform output is purportedly a useful, concrete, and tangible result (*See* App. Br. 10).

Nevertheless, we find the claims before us to be clearly distinguished from the method or process claims considered by the court in *Bilski*. Here, we note that the preamble of independent claim 60 positively recites a computer system which is supported in the language found in the body of the claim ("wherein *the computer system* produces the correct ordering of transform outputs with no need to perform an additional bit-reversal ordering pass."). *See Bell Communications Research, Inc. v. Vitalink Communications Corp.*, 55 F.3d 615, 620 (Fed. Cir. 1995) ("[W]hen the claim drafter chooses to use both the preamble and the body to define the subject matter of the claimed invention, the invention so defined, and not some other, is the one the patent protects."). Therefore, we consider Appellant's claimed "computer system" as an apparatus which executes a software program.

When we apply the broadest reasonable construction that is consistent with Appellant's Specification, we also interpret the claimed "vector processors" of claim 60 and the "single instruction multiple data (SIMD) processor" of dependent claim 61 as conventional *hardware components* that execute software to implement Appellant's FFT mathematical algorithm (*See* FF 3, 6).[FN3] Accordingly, we consider claims 60 and 61 as apparatus claims that implement a mathematical algorithm (i.e., a Fast Fourier Transform).

Thus, we see the question before us to be whether the "mathematical algorithm" exception applies to an apparatus claim where the practical result of granting such a claim would preempt substantially all uses of a fundamental principle.

In *Alappat*, the court noted that the Supreme Court has held that "certain mathematical subject matter is not, standing alone, entitled to patent protection." *In re Alappat*, 33 F.3d at 1543 (citing *Diamond v. Diehr*, 450 U.S. 175, [185]; *Parker v. Flook*, 437 U.S. 584, [589]; *Gottschalk v. Benson*, 409 U.S. 63, [67]).

***6** As also set forth in *Alappat*, the Federal Circuit recognized that their own precedent suggests that the "mathematical algorithm" exception may be applicable to an apparatus claim." *In re Alappat*, 33 F.3d at 1542 (citing *In re Johnson*, 589 F.2d 1070, 1077 (CCPA 1978) ("*Benson* [referring to *Gottschalk v. Benson*, 409 U.S. 63, 93 S.Ct. 253, 34 L.Ed.2d 273 (1972)] applies equally whether an invention is claimed as an apparatus or process, because the form of the claim is often an exercise in drafting.")).

However, the court in *Alappat* determined that "[e]ven if the mathematical subject matter exception to § 101 does apply to true apparatus claims, the claimed subject matter in this case does not fall within that exception." *In re Alappat*, 33 F.3d at 1542. Of particular significance here, we note that the court in *Alappat* grounded its reasoning, at least in part, on the "useful, concrete, and tangible result" test recently abrogated by *In re Bilski*. *See In re Alappat*, 33 F.3d at 1544 ("This is not a disembodied mathematical concept which may be characterized as an 'abstract idea,' but rather a specific machine to produce a useful, concrete, and tangible result.").

When considering the language of instant claims 60 and 61 as a whole, we conclude that these claims merely implement an optimized Fast Fourier Transform on a conventional computer system that includes one or more conventional vector processors. As claimed, we find the transform output *results* of the FFT calculation are not used for any practical purpose or inventive application whatsoever. *Cf. Parker v. Flook*, 437 U.S. 584, 591-594 (1978) ("Even though a phenomenon of nature or mathematical formula may be well known, an *inventive application* of the principle may be patented. Conversely, the discovery of such a phenomenon cannot support a patent unless there is some other inventive concept in its application.") (emphasis added).

In addition, we observe that Appellant has not limited the scope of the claimed invention to a *particular* type of computer system. Indeed, Appellant's Specification expressly discloses that "[t]he method can be embodied in software that can run on a variety of computers known in the art, including *without limitation*, personal computers, workstation computers, and supercomputers known in the art." (FF 2, emphasis added).

***7** It is clear that without the recited conventional hardware elements, Appellant's claim would be non-statutory under 35 U.S.C. § 101 as being directed to an abstract idea and/or a fundamental principal (i.e., a mathematical algorithm). Therefore, the question that remains is whether drafting an invention in a different statutory category (i.e., as a conventional apparatus or machine) is all that is necessary to overcome a § 101 rejection of a pure mathematical algorithm, particularly in view of the Federal Circuit's recent discussion of Benson, stating that a computer-implemented method is not patent-eligible if the mathematical algorithm has no other use than operating on a digital computer and would preempt the fundamental principle since all uses of the algorithm are still covered by the claim. *Bilski*, 545 F.3d at 955.

As discussed *supra*, we have found that the claimed transform outputs of Appellant's FFT calculation are not used for any practical purpose or inventive application whatsoever. We also note that Appellant has not limited the scope of the claimed invention to a *particular* type of computer system. Indeed, we find the spectrum of hardware supported in Appellant's Specification to be sweeping in breadth (*See* FF 2, 3, 5).

Therefore, we find the nominal recitation of conventional computer components in an apparatus claim otherwise directed to a pure mathematical algorithm (e.g., a Fast Fourier Transform) does not impose any meaningful limits on the scope of the claim. We conclude that Appellant's claims effectively preempt substantially all uses of the recited mathematical algorithm as a fundamental principal.

We hold that merely adding a nominal recitation of conventional computer hardware in a claim otherwise directed to a pure mathematical algorithm is merely an exercise in claim drafting that cannot, by itself, render the claim statutory. It is our reasoned view that to hold otherwise would exalt form over substance and the practical effect would be a patent on the mathematical algorithm itself. We are of the view that the purpose of 35 U.S.C. § 101 would be defeated if a patent applicant is able to evade a § 101 rejection of a pure mathematical algorithm by a nominal claim to structure.

Accordingly, we sustain the Examiner's rejection of claims 60 and 61 as being directed to non-statutory subject matter under 35 U.S.C. § 101.

CONCLUSION

Based on the findings of facts and analysis above, Appellant has not established that the Examiner erred in rejecting claims 60 and 61 as being directed to non-statutory subject matter under 35 U.S.C. § 101.

DECISION

***8** We affirm the Examiner's decision rejecting claims 60 and 61.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

FN1. The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Data (electronic delivery).

FN2. Cancelled claims 1-46 previously issued in parent application No. 09/728,469, now U.S. Patent 6,609,140 (*See* App. Br. 5).

FN3. Appellant acknowledges in the principal Brief that the *first loop means, second loop means, non-final stage calculating means, and final stage calculating means* are implemented, in the specification, in software. (FF 6.)

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