IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

VLSI TECHNOLOGY LLC, *Plaintiff,*	§	
	§	
	§	**6:21-CV-057-ADA**
v.	§	
	§	
INTEL CORPORATION, *Defendant.*	§	
	§	

ORDER DENYING DEFENDANT INTEL'S RULE 52 MOTION FOR JUDGMENT OF NO INFRINGEMENT OF U.S. PATENT NO. 7,725,759 UNDER THE DOCTRINE OF EQUIVALENTS (ECF No. 593)

Before this Court is Defendant Intel Corporation's ("Intel") Motion for Judgment of No Infringement of U.S. Patent No. 7,725,759 under the Doctrine of Equivalents pursuant to Fed. R. Civ. P. 52. Intel filed its Motion on April 9, 2021. ECF No. 593. Plaintiff VLSI Technology LLC ("VLSI") filed its Response in Opposition on May 7, 2021. ECF No. 607. Defendant Intel filed its Reply in Support on May 21, 2021. ECF No. 616. After reviewing the parties' briefs and the relevant law, Intel's Motion is **DENIED** for the reasons set out below.

I. BACKGROUND

Plaintiff VLSI filed its suit for patent infringement on April 11, 2019. ECF No. 1. In its Complaint, VLSI accused Intel of infringing U.S. Patent Nos.7,523,373 ("the '373 Patent") and 7,725,759 ("the '759 Patent"). The Court held a jury trial, which concluded on March 2, 2021, with a verdict in VLSI's favor. ECF No. 556. The jury found infringement of the '759 Patent only under the doctrine of equivalents ("DOE"). ECF No. 593 at 1. The jury awarded over $2 billion in damages to VLSI, which included a $675 million lump sum for infringement of the '759 Patent. Intel filed its Motion for Judgment on April 9, 2021.

The '759 Patent relates to controlling clock frequency in an electronic device. ECF No. 607 at 2. The Patent seeks to "deliver faster clock speeds while also managing power consumption." *Id.* The '759 Patent "discloses and claims a system in which a first master device of a plurality of master devices provides a 'request' to change a clock frequency of a high-speed clock 'in response to a predefined change in performance of the first master device.'" *Id.* at 3. A "programmable clock controller" receives this "request" and provides outputs to independently control (1) a clock frequency of a second master device coupled to a bus, and (2) a variable clock frequency of the bus. *Id.* VLSI asserted that Intel infringed on claims 14, 17, 18, and 24 of the '759 Patent, both literally and under DOE.

VLSI's DOE theory was presented by its expert Dr. Thomas M. Conte. *Id.* at 3. He testified that the combination of core 1 ("first master device") and core 1's associated code in the PCU ("programmable clock controller") provides the claimed "request" in the '759 Patent. *Id.* Specifically, he explained that the core sends a Core_Active signal to the PCU whenever the core becomes active. *Id.* C0 residency counters, which are counters in the PCU, measure the activity of the core over a predefined time interval whe[redacted], the code in the PCU generates a "request" for a higher or lower frequency. *Id.* VLSI's literal infringement theory of "request" was based on the Core_Active signals, but its DOE theory was based on the output of the core in combination with the code in the PCU. *Id.* at 4.

Intel now moves for judgment as a matter of law under Rule 52 that Intel does not infringe on the '759 Patent. It argues that three defenses to DOE present questions for the Court to decide: prosecution history estoppel, ensnarement, and claim vitiation. The parties have stipulated that

Intel's defenses are appropriate for resolution pursuant to a bench trial on the papers without any additional live testimony. ECF No. 587.

II. STANDARD OF REVIEW

In a bench trial, "[i]f a party has been fully heard on an issue ... and the court finds against the party on that issue, the court may enter judgment against the party on a claim or defense that, under the controlling law, can be maintained or defeated only with a favorable finding on that issue." Fed. R. Civ. P. 52(c) ("A judgment on partial findings must be supported by findings of fact and conclusions of law as required by Rule 52(a)."). Such findings are made pursuant to Rule 52(a), under which "the court must find the facts specially and state its conclusions of law separately." Fed. R. Civ. P. 52(a). "Rule 52(a) only requires weighing the evidence to determine whether the plaintiff has proven his case." *Thanedar v. Time Warner, Inc.*, 352 F. App'x 891, 897 n.1 (5th Cir. 2009).

In ruling on a Rule 52 motion, the trial court need not consider the evidence in a light favorable to the plaintiff and may render judgment for the defendant if it believes the plaintiff's evidence is insufficient to make out a claim." *Kaneka Corp. v. JBS Hair, Inc.*, 3:10-CV-01430-P, 2013 WL 12190524, at *3 (N.D. Tex. Aug. 30, 2013). Under Rule 52(c), "[a] judgment on partial findings must be supported by findings of fact and conclusions of law as required by Rule 52(a)." Fed. R. Civ. P. 52(c). Rule 52(a) does not require that the district court set out findings on all factual questions that arise in a case. *See Valley v. Rapides Parish Sch. Bd.*, 118 F.3d 1047, 1053-54 (5th Cir. 1997). Rather, the district court is expected to provide a clear understanding of the analytical process by which ultimate findings and conclusions were reached. *Id.* Under Rule 52, the court is "entitled to weigh evidence, make credibility judgments, and draw inferences unfavorable to the [any party]." *Id.* On a Rule 52 motion, the court "make[s] a determination in

accordance with its own view of the evidence." *Fairchild v. All Am. Check Cashing, Inc.*, 815 F.3d 959, 963 n.1 (5th Cir. 2016).

III. FINDINGS OF FACT

The Court makes the following findings of fact.

A. The Parties

1. Plaintiff VLSI is a Delaware limited liability company duly organized and existing under the laws of the State of Delaware. The address of the registered office of VLSI is Corporation Trust Center, 1209 Orange St., Wilmington, DE 19801. ECF No. 1 ¶ 1.

2. Intel is a corporation duly organized and existing under the laws of the State of Delaware, having a regular and established place of business at 1300 S. Mopac Expressway, Austin, Texas 78746. ECF No. 61 ¶ 3.

B. Background of the '759 Patent

3. U.S. Patent No. 7,725,759 was filed June 29, 2005, and is entitled "System And Method of Managing Clock Speed In An Electronic Device." Plaintiff's trial exhibit ("PTX") PTX-5.1. The '759 patent issued on May 25, 2010. *Id.*

4. The '759 patent recognized that one way to increase the performance of an electronic device was to increase the clock frequency of the clock used in the device. "One way to increase the performance of the MP3 player and provide quicker access to stored files is to increase the clock frequency of the clock used in the device." '759 Patent 1:16-19.

5. The inventor of the '759 patent also recognized that increasing performance of the device also increases power consumption. "However, as the clock frequency increases to deliver more performance, the power consumption of the MP3 player also increases." *Id.* at 1:19-21.

6. The inventor recognized that there was a need to balance performance and power to selectively deliver faster clock speeds. "Accordingly, there is a need for an improved system and method of controlling a clock frequency in an electronic device in order to selectively deliver faster clock speeds." *Id.* at 1:22-24.

7. The '759 patent discloses and claims a system in which a first master device of a plurality of master devices provides a "request" to change a clock frequency of a high-speed clock "in response to a predefined change in performance of the first master device." A "programmable clock controller" receives the request and provides outputs to independently control (1) a clock frequency of a second master device coupled to a bus, and (2) a clock frequency of the bus. *Id.* at 8:50-9:4 (claim 14), 9:19-40 (claim 18).

C. Prosecution History of the '759 Patent

8. At trial, VLSI's expert, Dr. Conte, testified that Intel infringes the '759 patent under the DOE by using a combination of a core ("first master device") and the core's associated code in the PCU ("programmable clock controller") to provide the "request" claimed in the '759 patent.

1) The Ansari Reference

9. One of the references cited by the Examiner during prosecution of the '759 patent was U.S. patent No. 7,007,121 to Ansari ("Ansari"). ECF No. 608-4. Ansari is entitled "Method And Apparatus For Synchronized Buses." *Id.* at 1.

10. Figure 6 of Ansari, reproduced below, shows a block diagram of Ansari's system. "FIG. 6 is a functional block diagram illustrating the operation of a bus according to one embodiment of the present invention." *Id.* at 9:59:61; Fig. 6.

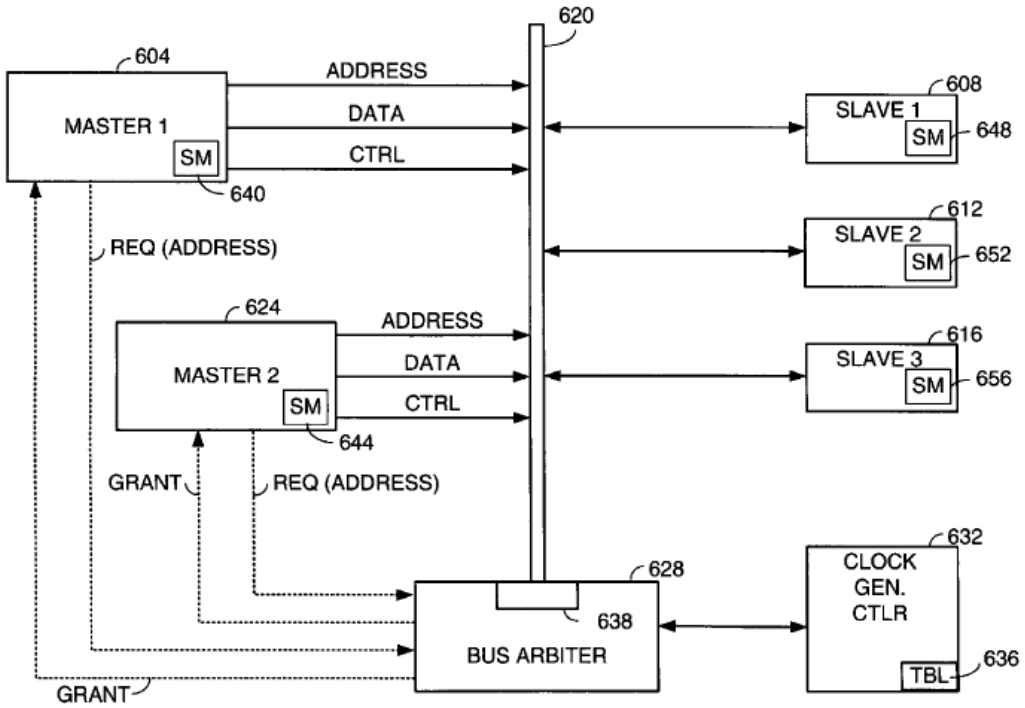

FIG. 6

11. Masters 604 and 624 as well as devices 608, 612, and 616 are coupled to a bus 620. *Id.* at 9:61-65; Fig. 6.

12. Ansari discloses that a master generates a request to a bus arbiter 628 in order to access the bus 620 and initiate a transaction, e.g., to transfer data on the bus to a target device. "In operation, in one embodiment of the present invention, a master, for example, master 624, generates a request to bus arbiter 628 to gain control of bus 620 for a transaction. In addition to generating the request, master 624 specifies an address of a slave to which the communication is to be transmitted." *Id.* at 11:4-9. The masters in Ansari do not request a change (increase or decrease) in the clock frequency of the bus 620.

13. Ansari discloses that the bus arbiter 628 determines the bus speed for the transaction, based on specific parameters. "Because there are at least two masters in the network of FIG. 6, a bus arbiter 628 is required to determine which master 604 or 624 can access and control communications on the bus and a bus rate or speed for the required

transaction. . . . In general, however, the parameters that effect the bus speed include an examination of the source of the communication or transaction, the destination, the length of bus between the two, the number of devices connected to the bus, and other factors such as the relative frequency rates between the two devices." *Id.* at 9:65–10:2, 10:18–23.

14. During prosecution, the Applicant replaced one claim set that recited "at least one" and "the at least one" master device with a new claim set that recited "a" and "the" master device. PTX-8-A.314-.318; PTX-8-A.367-.370.

15. The Applicant did not add any words to the claims such as "only" one master device making a request or the master device "alone" making a request. PTX-8-A.367-.369.

16. The Applicant did not make any arguments during prosecution requiring one master device alone making a request. PTX-8-A.371.

17. The Examiner did not make any statements to convey an understanding that a reference to "a master device" and "the master device" referred to only one master device making a request. PTX-8-A.385. The Examiner simply identified a "Claim Objections" stating: "Claims 30-43 are objected to because of the following informalities: line 6 of claim 30 recite 'the at least one master device' which lacks antecedent basis." *Id*.

18. The following claims were pending as of the Applicant's April 28, 2008 Response: claims 1, 3, 5-15, and 17-29. PTX-8-A.314-.318.

19. Claim 1 recited, in pertinent part: "monitoring a plurality of master devices," "receiving an input from at least one of the plurality of master devices, wherein the input is to *request* an increase to the clock frequency of the bus" and "setting a high frequency flag for the at least one of the plurality of master devices." PTX-8-A.314. Similarly, claim 10 recited, in pertinent part: "receiving a bus master request from at least one of the plurality of devices,

wherein the bus master request is a request to communicate via the bus and to increase the clock frequency of the bus" and "determining whether the at least one of the plurality of devices is a preferred device." PTX-8-A.315. Similarly, independent claim 18 and dependent claim 22 recited, in pertinent part: "at least one master device coupled to the bus" (claim 18) and "wherein the at least one master device provides a corresponding trigger input, wherein the trigger input includes a request to change the variable clock frequency" (claim 22). PTX-8-A.316-317.

20. In the Remarks Section of the April 28, 2008, Response, the Applicant distinguished then-pending claim 1 from the Ansari, stating: The cited portions of Ansari fail to disclose or suggest receiving an input from at least one of the plurality of master devices, wherein the input is to request an increase to the clock frequency of the bus, as in claim 1. Ansari discloses that masters 604 and 624 transmit bus requests to the bus arbiter 628 to gain control of or to "own" the bus 620 for a transaction. *(See e.g.*, Ansari, 8:66, 9:5, 10:30–33). PTX-8-A.319.

21. In other words, the Applicant argued that claim 1 recited "the input is to request an increase to the clock frequency of the bus" and Ansari disclosed a request to *gain access* to the bus rather than request an increase in clock frequency of the bus.

22. The Applicant made a similar argument to distinguish then-pending claim 10 from Ansari, stating:

> The cited portions of Ansari do not disclose or suggest the specific combination of claim 10. For example, the cited portions of Ansari do not disclose receiving a bus master request from at least one of the plurality of devices, wherein the bus master request is a request to communicate via the bus and to increase the clock frequency of the bus and setting a high frequency flag for the at least one of the plurality of devices when the at least one of the plurality of devices is a preferred device, as in claim 10. The Office asserts that Ansari receives a bus master request that is a request to communicate via the bus and references lines 3-17 of column 11. *(See*

> Office Action, page 6). ***Ansari discloses that masters 604 and 624 transmit bus requests to the bus arbiter 628 to gain control of or to "own" the bus 620 for a transaction.*** (*See* e.g., Ansari, Col. 8, line 66 - Col. 9, lines 5; and Col. 10, lines 30-33). . . . The cited portions of Ansari fail to disclose or suggest that the bus request transmitted by the master 604 or 624 requests an increase to the clock frequency of the bus 620.

PTX-8-A.323 (emphasis added).

23. In response to a further Office Action (PTX-8-A.336-.357), the Applicant cancelled claims 1–29 and introduced new claims 30-58. PTX-8-A.367-.370.

24. New claim 30 recited, in pertinent part: "monitoring a plurality of master devices," "receiving a request to change the clock frequency of the bus from a master device of the plurality of master devices, the request sent from the master device in response to a predefined change in performance of the master device." PTX-8-A.367. New claim 44 recited, in pertinent part: "a master device coupled to the bus, the master device operable to provide a request to change the clock frequency of the bus in response to a predefined change in performance of the master device." PTX-8-A.368. New claim 49 recited, in pertinent part: "a master device coupled to the bus" and "the clock controller operable to receive a request to change the clock frequency of the bus from the master device, the request sent from the master device in response to a predefined change in performance of the master device." PTX-8-A.369.

25. In the Remarks Section of the September 10, 2008, Response, the Applicant distinguished then-pending claim 30 from the cited prior art including Ansari, stating:

> For example, the cited portions of Ansari, Kurosawa, Baek, and Velasco fail to disclose or suggest receiving a request to change the clock frequency of the bus from a master device of the plurality of master devices, the request sent from the master device ***in response to a predefined change in performance of the master device***, as in claim 30. In contrast to claim 30, for example, Ansari discloses receiving a request from a device that happens to cause an arbiter to increase the bus speed. However, a request from a device that happens to cause an arbiter to increase the bus speed is not a request to change the bus speed.

PTX-8-A.371 (emphasis added).

26. Applicant's Response makes clear that Applicant was distinguishing Ansari because the master in Ansari did not send a request "in response to a predefined change in performance of the master device."

27. Furthermore, the Applicant argued, consistent with its September 17, 2007, and April 28, 2008 Responses, that the master device in Ansari does not request a change of the bus clock speed. In other words, the master in Ansari simply requests access to the bus to initiate a bus transaction, and that it is the bus arbiter that may increase the clock speed of the bus. At no point did the Applicant distinguish Ansari for purportedly disclosing a first master device and a programmable clock controller (or any other device) that, in combination, provided the claimed request. Nor did the Applicant argue that the then-pending claims required only the first master device alone to make the claimed request.

28. When Applicant introduced new claim 30 in the September 10, 2008, Response, it erroneously used the old formulation "from the at least one master device" in the last limitation of claim 30, despite reciting "a master device" earlier in the claim.

30. (New) A method of controlling a clock frequency of a bus, the method comprising:

monitoring a plurality of master devices coupled to the bus;

receiving a request to change the clock frequency of the bus from a master device of the plurality of master devices, the request sent from the master device in response to a predefined change in performance of the master device; and

in response to receiving the request from the at least one master device, controlling the clock frequency of the bus.

PTX-8-A.367 (highlighting added for emphasis).

29. In a subsequent Office Action, the Patent Office noted this minor error, stating "Claims 30-43 are objected to because of the following informalities: line 6 of claim 30 recite

'the at least one master device', which lacks antecedent basis." PTX-8-A.385. There were no statements by the Examiner that the claims necessarily refer to *only* one master device making the request. *Id*.

30. In a subsequent Response, the Applicant corrected the minor error by amending claim 30 to recite "in response to receiving the request from the at least one master device." PTX-8-A.405. In the Remarks section, the Applicant stated: "The Office has objected to claims 30-43 because of informalities. Applicant has amended the claims to cure the informalities." PTX-8-A.410. There were no statements by the Applicant that the amended claims necessarily refer to *only* one master device making a request. *Id*.

31. The following claims were pending as of the Applicant's September 17, 2007, Response: claims 1, 3, and 5–29. PTX-8-A.235-.239.

32. Then-pending independent claim 1 in the September 17, 2007 Response recited:

1. (Currently Amended) A method of controlling a clock frequency, the method comprising:

monitoring a plurality of master devices coupled to a bus within a system;

receiving an input from at least one of the plurality of master devices, wherein the input is to request an increase to the clock frequency of the bus;

determining whether to enable the request to increase the clock frequency of the bus and,

setting a high frequency flag when the request is enabled;

monitoring a plurality of high frequency flags; and

selectively increasing a clock frequency in response to at least one of the plurality of high frequency flags being set.

PTX-8-A.235 (highlighting added for emphasis). Then pending independent claim 10 recited a similar limitation. PTX-8-A.236.

33. In its September 17, 2007, Response, the Applicant explained that Ansari sends a bus request to initiate a transaction on the bus, not to request an increase in frequency, and that

it is the bus arbiter that determines an appropriate frequency to use for the transaction. "A master device seeking bus resources to initiate a transaction sends a bus request and a destination address to the bus arbiter so that the arbiter can determine a corresponding bus frequency. (Col. 8, line 66 to col. 9, line 6). Thus, in Ansari, a master device sends a bus request to the bus arbiter. The master device does not determine or request a desired bus frequency because it is the bus arbiter that determines the bus frequency based on various factors." PTX-8-A.241-.242 (emphasis added).

34. Thus, consistent with Ansari's teaching, the Applicant argued that the masters in Ansari only request access to the bus to initiate a transaction, such as a data transfer.

35. In the Remarks Section of the April 28, 2008 Response, the Applicant distinguished then-pending claim 1 from the Ansari, stating:

> The cited portions of Ansari fail to disclose or suggest receiving an input from at least one of the plurality of master devices, wherein the input is to request an increase to the clock frequency of the bus, as in claim 1. Ansari discloses that masters 604 and 624 transmit bus requests to the bus arbiter 628 to gain control of or to "own" the bus 620 for a transaction. (*See* e.g., Ansari, Col. 8, line 66 - Col. 9, lines 5; and Col. 10, lines 30-33).

PTX-8-A.319.

36. In other words, Applicant argued that claim 1 recited "the input is to request an increase to the clock frequency of the bus" and Ansari disclosed a request to *gain access* to the bus rather than request an increase in clock frequency of the bus.

37. The Applicant made a similar argument to distinguish then-pending claim 10 from Ansari, stating:

> The cited portions of Ansari do not disclose or suggest the specific combination of claim 10. For example, the cited portions of Ansari do not disclose receiving a bus master request from at least one of the plurality of devices, wherein the bus master request is a request to communicate via the bus and to increase the clock frequency of the bus and setting a high frequency flag for the at least one of the plurality of

> devices when the at least one of the plurality of devices is a preferred device, as in claim 10. The Office asserts that Ansari receives a bus master request that is a request to communicate via the bus and references lines 3-17 of column 11. *(See* Office Action, page 6). ***Ansari discloses that masters 604 and 624 transmit bus requests to the bus arbiter 628 to gain control of or to "own" the bus 620 for a transaction.*** (*See* e.g., Ansari, Col. 8, line 66 - Col. 9, lines 5; and Col. 10, lines 30-33). . . . The cited portions of Ansari fail to disclose or suggest that the bus request transmitted by the master 604 or 624 requests an *increase* to the clock frequency of the bus 620.

PTX-8-A.323.

38. Applicant's arguments in the April 28, 2008, Response were consistent with what Applicant argued in its September 17, 2007, Response.

39. In the Remarks Section of the September 10, 2008, Response, the Applicant distinguished then-pending claim 30 from the cited prior art including Ansari, stating:

> For example, the cited portions of Ansari, Kurosawa, Baek, and Velasco fail to disclose or suggest receiving a request to change the clock frequency of the bus from a master device of the plurality of master devices, the request sent from the master device in response to a predefined change in performance of the master device, as in claim 30. In contrast to claim 30, for example, Ansari discloses receiving a request from a device that happens to cause an arbiter to increase the bus speed. However, a request from a device that happens to cause an arbiter to increase the bus speed is not a request to change the bus speed.

PTX-8-A.371 (emphasis in original).

40. The Applicant was distinguishing Ansari because the master in Ansari did not send a request "in response to a predefined change in performance of the master device." Furthermore, the Applicant argued, consistent with its September 17, 2007, and April 28, 2008, Responses, that the master device in Ansari does not request a change of the bus clock speed. In other words, the master in Ansari simply requests access to the bus to initiate a bus transaction, and that it is the bus arbiter that may increase the clock speed of the bus.

D. VLSI's Infringement Claims in This Litigation

41. VLSI's infringement claims have not shifted during the litigation.

42. In its complaint for patent infringement, VLSI accused "Intel products that use infringing Hardware-Controlled Performance States ('HWP' or 'Speed Shift') technology" infringe at least claim 1 of the '759 patent both literally and under the doctrine of equivalents. ECF No. 1.

43. In its July 22, 2019, Preliminary Infringement Contentions, VLSI identified the products accused of infringing claims of the '759 patent as including "all Intel products that support Speed Shift (collectively, 'Speed Shift') according to the '759 Patent that were public released in or after 2013, derivatives, including server variants" including Skylake, Kaby Lake, Coffee Lake, and Cannon Lake. ECF No. 592-4.

44. In its January 2, 2020, Amended Infringement Contentions, VLSI identified the products accused of infringing claims of the '759 patent as including "all Intel products that support Speed Shift (collectively, 'Speed Shift') according to the '759 Patent that were public released in or after 2013, which to VLSI's present knowledge include the following Intel products and any derivatives, including server variants" including Skylake, Kaby Lake, Coffee Lake, Cannon Lake, Amber Lake, and Whiskey Lake. ECF No. 592-5.

45. In its January 2, 2020 Amended Infringement Contentions, VLSI identified the products accused of infringing claims of the '759 patent as including "all Intel products that support Speed Shift (collectively, 'Speed Shift') according to the '759 Patent that were public released in or after 2013, which to VLSI's present knowledge include the following Intel products and any derivatives, including server variants" including Skylake, Kaby Lake, Coffee Lake, Cannon Lake, Amber Lake, and Whiskey Lake. *Id.*

46. In its January 26, 2020 Second Amended Infringement Contentions, VLSI identified the products accused of infringing claims of the '759 patent as including "all Intel

products that support Speed Shift (collectively, 'Speed Shift') according to the '759 Patent that were public released in or after 2013, which to VLSI's present knowledge include the following Intel products and any derivatives, including server variants" including Skylake, Kaby Lake, Coffee Lake, Cannon Lake, Amber Lake, Whiskey Lake, Comet Lake, Ice Lake, and Tiger Lake. ECF No. 592-6. VLSI asserted both literal infringement and infringement under the doctrine of equivalents. *See, e.g., id*., at 27, 84, and 131.

47. In its January 31, 2020 Final Infringement Contentions, VLSI identified the products accused of infringing claims of the '759 patent as including "all Intel products that support Speed Shift (collectively, 'Speed Shift') according to the '759 Patent that were public released in or after 2013, which to VLSI's present knowledge include the following Intel products and any derivatives, including server variants" including Skylake, Kaby Lake, Coffee Lake, Cannon Lake, Amber Lake, Whiskey Lake, Cascade Lake, Comet Lake, Ice Lake, and Tiger Lake. ECF No. 592-7. VLSI asserted both literal infringement and infringement under the doctrine of equivalents. *See, e.g., id*., at 27–28, 93, and 148.

48. In the December 22, 2020 Joint Final Pretrial Order, VLSI asserted that "Intel infringes Claims 1, 14, 17, 18, 24, and 26 of U.S. Patent No. 7,725,759 by making, using, selling, offering for sale, and/or importing into the United States Intel's Skylake client and server processors, Kaby Lake processors, Coffee Lake processors, Whiskey Lake processors, Amber Lake processors, Comet Lake processors, Cannon Lake processors, Cascade Lake server processors, Ice Lake client and server processors, and Tiger Lake processors, all other Intel products that include Intel's Speed Shift Technology, and any other processors with essentially the same structures as those identified in VLSI's infringement analysis ("'759 Accused Products"). Intel infringes Claims 1, 14, 17, 18, 24, and 26 of the '759 Patent, directly

or indirectly, either literally or under the doctrine of equivalents. The doctrine of equivalents is available and has been properly applied for the Asserted Claims." ECF No. 398-02 at 7.

49. During discovery, Intel only asserted prosecution history estoppel and ensnarement defenses. Intel first raised the issues of alleged ensnarement for the '759 Patent on April 17, 2020, generally asserting that: "Further, VLSI's doctrine-of-equivalents theories cannot be asserted because they would ensnare the prior art" followed by a general listing of the same prior art asserted by Intel in its invalidity contentions. *See* ECF No. 608-7.

50. Additionally, despite raising the issue of claim vitiation for other patents in April 2020, Intel did not amend its responses ever to include such an assertion for the '759 patent. *See* ECF No. 608-7 at 269–287.

51. Further, Intel only sought responses to its assertion of ensnarement on June 17, 2020, the last possible day to serve written discovery, when it served its Third Set of Interrogatories. In Interrogatory No. 22 it asked: "If You contend that the doctrine of ensnarement does not bar VLSI from obtaining relief for Intel's alleged infringement of any of the Asserted Patents, set forth the complete basis for each and every such contention on a patent-by-patent basis." ECF No. 608-9 at 3. VLSI responded by explaining how Intel's vague assertion of ensnarement was insufficient and that its infringement theories, as memorialized in its highly detailed infringement contentions, demonstrate that no prior art is "ensnared." ECF No. 608-10 at 64–65.

52. Intel never sought responses to any claims of prosecution history estoppel or claim vitiation.

53. VLSI preemptively responded to Intel's allegations in expert discovery. In his Opening Report, Dr. Conte addressed ensnarement and provided an implicit hypothetical claim through his doctrine of equivalents analysis. ECF No. 608-2 ¶¶ 616, 638, 1057, 1077.

54. Intel set forth its general ensnarement, prosecution history estoppel, and claim vitiation defenses in the Rebuttal Report of Dr. Dirk Grunwald, which did not allow for VLSI to address these assertions made by Dr. Grunwald for the first time in a written report. Dr. Grunwald's Opening Report did not include an assertion of any of these defenses.

55. VLSI provided Intel with notice of a hypothetical claim that would both literally capture the accused products but not the vaguely asserted prior art. *See, e.g., id.* ¶¶ 613-639, and 1054–1078.

56. Intel filed a motion for summary judgment of no infringement under the doctrine equivalents on the basis of prosecution history estoppel only. *See* ECF No. 253. Intel did not assert claim vitiation or ensnarement as defenses in its motion.

57. In the Joint Pre-Trial Order, Intel reasserted its assertions of prosecution history estoppel, ensnarement, and the "all elements" rule. ECF No. 398-02 ¶ 41; *see also id.* ¶ 77. Intel did not list any prior art specific to ensnarement, but listed Yonah, Chen, Terrell, Rusu, and Kiriake as prior art for anticipation and/or obviousness. *Id.* ¶ 42. VLSI responded that it disagrees with Intel's contentions. *Id.* ¶ 19.

58. During fact discovery, VLSI asserted that Intel products infringe claims of the '759 patent under the doctrine of equivalents. For example, in its January 31, 2020, Final Infringement Contentions, VLSI identified that Intel products (including Skylake, Kaby Lake, Coffee Lake, Cannon Lake, Amber Lake, Whiskey Lake, Cascade Lake, Comet Lake, Ice Lake, and Tiger Lake) infringe claims of the '759 patent under the doctrine of equivalents.

ECF No. 592-7 at 2728, 48, 53–54, 59–60, 66–67, 93, 116, 147–148, 165–166, 175–176, and 185.

59. For example, VLSI asserted: "In the Accused Products, for instance, requests within the PCU to change the frequency of the clock achieve substantially or exactly the same function (e.g., to change the clock frequency of the clock in response to a predefined change in performance of a master device as configured in the Accused Products) in substantially or exactly the same way as set forth in the claim (e.g., by using circuitry/logic in the master device and/or PCU of the Accused Products), to achieve substantially or exactly the same result (e.g., control the clock frequency of a second master device coupled to the bus as implemented in the Accused Products)." ECF No. 592-7 at 93, 147–148.

60. VLSI's technical expert, Dr. Conte, asserted that Intel products infringe claims of the '759 patent under the doctrine of equivalents. ECF No. 608-2 ¶¶ 613-639 and 1054–1078.

61. For example, Dr. Conte explained that the "Accused Products perform the substantially the same/identical function as recited in the claim in substantially the same way, namely, by using the combination of a core and the PCU to provide a request to change a clock frequency of a high-speed clock in response to a predefined change in performance of the first master device . . . ." *Id.* ¶ 616.

62. In his expert report on infringement of the '759 patent, Dr. Conte, explained that under the doctrine of equivalents the combination of the core and the PCU provides the claimed request. "The Accused Products perform the substantially the same/identical function as recited in the claim in substantially the same way, namely, by using the combination of a core and the PCU to provide a request to change a clock frequency of a high-speed clock in response to a predefined change in performance of the first master device . . . ." *Id.* ¶ 616.

63. Dr. Conte's analysis in his expert report identified a hypothetical claim in support of his doctrine of equivalents theory, namely, "by using the combination of a core and the PCU to provide a request." *Id.*

64. Dr. Conte expressly addressed ensnarement in his expert report, stating that the manner in which he was reading the claim did not ensnare the prior art.

> 638. My application of this claim term under the doctrine of equivalents does not encompass the prior art. I have read Intel's interrogatory response where it assert that "VLSI's doctrine-of-equivalents theories cannot be asserted because they would ensnare the prior art." 06- 24-2020 Intel Response to Interrogatory No. 15, at 519; see also id., at 520-536. I disagree. As an initial matter, Intel has not provided any explanation or analysis for how the doctrine of ensnarement could allegedly bar my analysis of infringement under the doctrine of equivalents (and, in fact, the doctrine does not bar it). For example, the manner in which I am reading this claim term on the '759 Accused Products differs from the teaching of the alleged prior art cited by Intel. By way of another example, my opinions herein under the doctrine of equivalents do not ensnare the cited prior art at least because Intel's cited prior art fails to teach, alone or in combination, other claim terms as well as the claimed combinations recited the claims of the '759 patent. I expect that I will address the reasons why the cited prior art fails to anticipate or render obvious the claims of the '759 patent in response to any report from an Intel expert on the topic.

Id. ¶ 638.

E. Hypothetical Claim

65. The following is a hypothetical claim presented by VLSI that is based on claim 14 of the '759 patent, with additions thereto shown in underline text and deletion shown in strikethrough text.

> Hypothetical Claim. A system comprising: a bus capable of operation at a variable clock frequency; a first master device coupled to the bus, the first master device <u>or the first master device and its associated code in a programmable clock controller</u> configured to provide a request to change a clock frequency of a high-speed clock in response to a predefined change in performance of the first master device, wherein the predefined change in performance is due to loading of the first master device as measured within a predefined time interval; and <u>the</u> ~~a~~ programmable clock controller having an embedded computer program therein, the computer program including instructions to: receive the request provided by the first master device <u>or the first master device and its associated code in the programmable clock controller</u>; provide the clock

> frequency of the high-speed clock as an output to control a clock frequency of a second master device coupled to the bus in response to receiving the request provided by the first master device or the first master device and its associated code in the programmable clock controller; and provide the clock frequency of the high-speed clock as an output to control the variable clock frequency of the bus in response to receiving the request provided by the first master device or the first master device and its associated code in the programmable clock controller.

66. VLSI's technical expert, Dr. Conte, testified at trial that Intel's accused products infringe under the doctrine of equivalents consistent with the scope of the foregoing Hypothetical Claim. Sealed Trial Tr. 36:3-61:23, Trial Tr. 487:17-488:10, 1417:25-1420:1; ECF No. 553-02 PDX4.154-214, PDX4.216-220; ECF No. 553-03 PDX5.13.

67. Intel's expert, Dr. Grunwald, never asserted Terrell, Ansari, or any obviousness combination at trial.

F. This Court Previously Rejected Intel's Arguments on Prosecution History Estoppel

68. Intel previously raised the same arguments with respect to prosecution history estoppel in its Motion for Summary Judgment of No Infringement Under the Doctrine of Equivalents. *See* ECF No. 253. Specifically, Intel argued that the Applicant narrowed the claims during prosecution and as such VLSI was barred from asserting the doctrine of equivalents.

69. This Court rejected Intel's arguments—the same arguments raised in Intel's Rule 52 Motion—finding that Intel had not proven its defense of prosecution history estoppel. ECF Nos. 411, 507.

G. VLSI's DOE Case at Trial

70. At trial, VLSI's expert, Dr. Conte, testified that Intel infringed claims 14, 17, 18, and 24 of the '759 patent, both literally and under the doctrine of equivalents. Sealed Trial Tr. 36:3-61:23, Trial Tr. 487:17-488:10, 1417:25-1420:1; ECF No. 553-02 PDX4.154-214, PDX4.216-220; ECF No. 553-03 PDX5.13.

71. At trial, Dr. Conte testified that the claimed "master device" was the cores in the Intel accused products. Sealed Trial Tr., 38:20-22; ECF No. 553-02 PDX4.166-167, PDX4.174.

72. Dr. Conte further testified that the claimed "request" was the Core_Active signal provided by the core(s) in the Intel accused products. Trial Tr. 417:17-23, 474:5-8; Sealed Trial Tr., 39:23-40:7, 40:18-41:8, 42:13-43:9; ECF No. 553-02 PDX4.171-174.

73. Dr. Conte testified that the Core_Active signal is sent by a core in response to a predefined change in performance of the core, [redacted]. "Q. Okay. So is there a request as required by the claims? A. There is. So the way it works is that workload changes . . . . You launch Word, and it runs on a core. [redacted] Sealed Trial Tr. 39:23-40:7; PTX-1805; *see also* Sealed Trial Tr. 42:13-43:4; ECF No. 553-02 PDX4.171-172:

[redacted]

74. Dr. Conte further testified that the claimed "programmable clock controller" included, among other circuitry, the PCU in Intel's accused products. Sealed Trial Tr., 40:18-23; ECF No. 553-02 PDX4.178-184.

75. Dr. Conte testified that Intel's accused products also infringe claims 14, 17, 18, and 24 of the '759 patent under the doctrine of equivalents. Sealed Trial Tr., 52:21-24, 57:21-58:1, 61:18-23; ECF No. 553-02 PDX4.202-214, PDX4.224.

76. Dr. Conte testified that the "core and the Core 1's P-code . . . provides the same function as required by the master device in the claim, that is to provide a request." Sealed Trial Tr., 55:1-6; 53:14-56:3; ECF No. 553-02 PDX4.204-214.

77. Dr. Conte further testified that "[t]he claim says 'the first master device provides a request.' Now, it's the first master device and its P-code that provides the request." Sealed Trial Tr., 55:7-11.

78. Dr. Conte testified that Intel's documentation also calls what Dr. Conte points to as the request, namely the output of a core's P-Code, as "a request for higher or lower frequency."

[redacted]

Sealed Trial Tr., 54:9-22; ECF No. 553-02 PDX4.205-208, PDX4.210.

79. [redacted]

[redacted]

[redacted] PTX-3484.3.

80. Dr. Conte further testified that the PCU's decision instructions treats the output of the core's P-Code as requests.

Sealed Trial Tr., 56:7-57:7; D-1154.

81. Dr. Conte testified that he applied the function-way-result test for his doctrine of equivalents opinions. "Q. Okay. So now, let's go back to your Doctrine of Equivalents analysis. Did you apply the function/weigh/result test? A. I did. . . ." Sealed Trial Tr., 55:1-6; ECF No. 553-02 PDX4.202.

82. Dr. Conte testified that Intel accused products "provides the same function as required by the claim ,that is to provide a request." Sealed Trial Tr., 55:4-6; Dkt. ECF No. 553-02 PDX4.208.

83. Dr. Conte testified that Intel's accused products provide a literal request in substantially the same way as the claim. Sealed Trial Tr., 55:1-11. Dr. Conte testified that the different between Intel's products and the claim is "just a difference of where an engineer draws this [dotted] line" and that it is "a design choice." Sealed Trial Tr., 55:12-17; ECF No. 553-02 PDX4.207, -.209:

84. Dr. Conte testified that "the result is that a request is provided" and that the Intel accused products provide "the same result as required by the claim." Sealed Trial Tr., 55:18-20, 56:3; ECF No. 553-02 PDX4.210.

85. Dr. Conte testified that the [redacted] within the PCU receives the request from the core and its P-code. Sealed Trial Tr., 56:4-57:16; ECF No. 553-02 PDX4.207; D-1154.

86. Dr. Conte did not identify C0 residency counters as a "request" under his DOE analysis at trial. Dr. Conte, instead, explained how C0 residency counters in Intel's products

87. Dr. Conte further testified that "[i]nside the PCU are these counters. They're called C0 residency counters. And the way they work is that Core_Active sends a signal to the PCU, and that starts these counters counting." Trial Tr. 1419:2-8; ECF No. 553-02 PDX5.13.

88. Dr. Conte explained the relationship between C0 Residency and the Core_Active signal, stating: "The core sends Core_Active signal and that starts this counter counting. And that's measured in this activity window we talked about." Trial Tr. 1419:12-18; ECF No. 553-02 PDX5.13.

89. Dr. Conte testified that "those [C0 residency] counters are going to be adjusted because you get the . . . Core_Active signal from the cores." Trial Tr. 1453:15-22.

90. Dr. Conte testified that "Core_Active starts these C0 residency counters. And then you send an inactive, it stops them." Trial Tr. 487:24-488:3.

91. Dr. Conte testified that the "Core_Active" signals are not sent periodically, but are sent "whenever the core becomes active." Trial Tr. 488:4-7 ("Q. Are Core_Active signals sent periodically? A. No. Q. When are they sent? A. They're sent whenever the core becomes active.").

92. Dr. Conte testified that the "testimony about periodic signals" do not "apply to the Core_Active requests." Trial Tr. 488:8-10 ("Q. So does any of that testimony about periodic signals apply to the Core_Active requests? A. No.").

93. Dr. Conte further testified how the C0 residency counters change, stating: "These counters change as you go through these windows. So imagine you start at the window with a five in one of those counters; and you go all the way to the end of the window, and at the end, it's five. Then you go to the next window, and during the next window there's a Core_Active and it goes six, seven, eight, nine, ten, and then you end. So what Dr. Rotem is not considering a request is really the fact that the counter from this window to this window actually changes. But if you recall, there was a lot of talk about that on Tuesday. And I said that that's indicative of a request." Trial Tr. 1454:14-1455:4.

94. Dr. Conte disputed Dr. Grunwald's demonstrative DDX-10.26 regarding the operation of Speed Shift, and modified Dr. Grunwald's demonstrative to show the relationship between Core_Active signal sent by the core and the C0 Residency counter in the PCU. Trial Tr. 1419:2-14:20:1; ECF No. 553-02 PDX5.13:

95. Dr. Conte testified that the "Core_Active then [is] an input to the autonomous algorithms that calculate the speed of the cores" and that "[i]f you didn't have that signal to turn on the counters, the PCU would never know that the cores' load changed. It would never change the speed of the cores due to loading." Trial Tr. 1419:19-1420:1.

96. At trial, Intel engineer, Dr. Efraim Rotem, testified that there are people at Intel that write the P-code for the PCU and identified Mr. Dan Borkowski. Dr. Rotem did not identify himself as writing P-code for the Intel accused products. Trial Tr. 1088:4-14.

97. At trial, Dr. Rotem never addressed or responded to Dr. Conte's testimony regarding the Core_Active signal sent by the cores to the PCU as part of the Dr. Conte's literal and doctrine of equivalents infringement analyses. *See generally* Trial Tr. 1045-1135 (Rotem Trial Testimony).

98. At trial, Intel engineer, Dan Borkowski, testified that "[w]e write the code, the P-code." Sealed Trial Tr. 96:20-21; Trial Tr. 1138:5-13.

99. At trial, Mr. Borkowski never addressed or responded to Dr. Conte's testimony regarding the Core_Active signal sent by the cores to the PCU as part of the Dr. Conte's literal and doctrine of equivalents infringement analyses. *See generally* Sealed Trial Tr. 96:8-108:7; Trial Tr. 1136-1153 (Borkowski Trial Testimony).

H. At Trial, the Jury Found Infringement of the '759 Patent Under the Doctrine of Equivalents

100. The jury found that Intel has infringed claims 14, 17, 18, and 24 of the '759 patent under the doctrine of equivalents. ECF No. 564 at 3.

IV. ANALYSIS

Having made its findings of fact, the Court now turns to the merits of Intel's Motion. Intel argues that VLSI is barred from relying on a DOE theory. Even if there is no literal infringement, DOE may constitute infringement if the differences between a claim limitation and the accused product are insubstantial. *Warner-Jenkinson Co. v. Hilton Davis Chem. Co.*, 520 U.S. 17, 24 (1997). Intel argues that VLSI's DOE claim is legally barred for three independent reasons: prosecution history estoppel, the ensnarement doctrine, and claim vitiation. These three arguments are addressed below.

A. Prosecution history estoppel does not bar VLSI's doctrine of equivalents theory.

A patent's prosecution history can legally bar application of a DOE claim in two ways: "(1) by making a narrowing amendment to the claim ('amendment-based estoppel) or (2) by surrendering claim scope through argument to the patent examiner ('argument-based estoppel')." *Amgen Inc. v. Coherus BioSciences Inc.*, 931 F.3d 1154, 1159 (Fed. Cir. 2019).

1) VLSI's amendment to the '759 Patent does not trigger the application of amendment-based prosecution history estoppel.

Amendment-based estoppel "arises when an amendment is made to secure the patent and the amendment narrows the patent's scope." *Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 535 U.S. 722, 736 (2002). "[The doctrine] applies when a claim is amended for 'a substantial reason related to patentability,' including 'to avoid the prior art . . . .'" *GeoTag, Inc. v. Starbucks Corp.*, No. 2:10-CV-572-MHS-RSP, 2014 WL 12639927, at *2 (E.D. Tex. Aug. 1, 2014). To assess whether amendment-based estoppel arises, "[t]he first question . . . is whether an amendment filed in the Patent and Trademark Office ('PTO') has narrowed the literal scope of a claim. If the amendment was not narrowing, then prosecution history estoppel does not apply." *Festo Corp.*, 344 F.3d at 1366. A "patentee's decision to narrow his claims through amendment may be presumed to be a general disclaimer of the territory between the original claim and the amended claim." *Pharma Tech Sols., Inc. v. LifeScan, Inc.*, 942 F.3d 1372, 1380 (Fed. Cir. 2019).

Intel argues that VLSI triggered amendment-based prosecution history estoppel when it amended the '759 patent claims to disclose "the first master device" in generating a request rather than "at least one master device" or "at least one of the plurality of master devices." ECF No. 593 at 11. A comparison between the original and amended claim language is shown in the table below:

Rejected Claim 22	**Asserted Claim 14**
at least one master device coupled to the bus, … wherein ***the at least one*** master device provides a corresponding trigger input, wherein the trigger input includes a request to change the variable clock frequency	***a*** first master device coupled to the bus, ***the*** first master device configured to provide a request to change a clock frequency of a highspeed clock in response to a predefined change in performance of ***the*** first master device
Rejected Claim 1	**Issued Claim 1**
monitoring a plurality of master devices coupled to a bus within a system; receiving an	monitoring a plurality of master devices coupled to a bus; receiving a request, from ***a***

input from ***at least one of the plurality*** of master devices, wherein the input is to request an increase to the clock frequency of the bus	first master device of the plurality of master devices,

According to Intel, VLSI's decision to amend the claim in response to the Examiner's express confirmation that such an amendment necessarily refers to "only one master device" creates a presumption that the narrowing relates to patentability. *Id.* at 12. Intel contends that VLSI sought to cover subject matter surrendered by amendment when it alleged that Intel infringed under the doctrine of equivalents based on a theory that the "request" was a "calculated speed change" in combination with an entirely different device. *Id.* at 13.

VLSI argues two reasons as to why the September 10, 2008, amendment was not narrowing. First, the word "alone" never appears in any of the claims. ECF No. 607 at 7. Second, VLSI argues that the indefinite article "a" itself means "at least one" and, consequently, has no impact on the claim's scope. ECF No. 607 at 1 (citing *Crystal Semiconductor v. Tritech Microelectronics*, 246 F. 3d 1336, 1347 (Fed. Cir. 2001). Further, VLSI notes that "[t]he subsequent use of definite articles 'the' or 'said' in a claim to refer back to the same claim term does not change the general plural rule, but simply reinvokes that non-singular meaning." ECF No. 607 at 7 (citing *Baldwin Graphic Sys., Inc. v. Siebert, Inc.*, 512 F.3d 1338, 1342 (Fed. Cir. 2008)). Thus, the claim does not require that "the first master device" alone generate the request. VLSI asserts that the Examiner did not confirm a change in patent scope; instead, the Examiner pointed out an antecedent basis "informality" as described in the Office Action, which VLSI subsequently cured. *Id.* at 8. VLSI argues that this correction cannot serve as a basis for estoppel and notes that "if the amendment was not narrowing, then prosecution history estoppel does not apply." ECF No. 607 at 6 (citing *Festo Corp.*, 344 F.3d at 1366).

In its Reply, Intel argues that "a" can mean "one" "where the language of the claims . . . or the prosecution history necessitate[s]." ECF No. 616 at 1 (citing *Baldwin Graphic Sys., Inc. v. Siebert, Inc.*, 512 F.3d 1338, 1342-43 (Fed. Cir. 2008)). Intel claims this is a case where the prosecution history through the amendment shows an intent to have "a" mean "one." *Id.* Relying on *Laitram Corp. v. NEC Corp.*, Intel argues that any amendment following a rejected claim scope must be a substantive change. 163 F.3d 1342, 1348 (Fed. Cir. 1998) (stating it is "difficult to conceive of many situations in which the scope of a rejected claim that became allowable when amended is not substantively changed by the amendment"). Finally, Intel argues that the Examiner's no antecedent basis rejection must have constituted claim narrowing because the rejection makes no sense under VLSI's theory that "a master device" means the same thing as "at least one master device." *Id.* If VLSI's theory was correct, Intel posits that the earlier appearing "a master device" language would have provided an antecedent basis for the "at least one master device" limitation. *Id.*

The Court finds that amendment-based estoppel does not apply. The 2008 amendment did not cause a substantive change in the claim language. The Applicant's change did not impact the claim scope because the Federal Circuit has long held that the indefinite article "a" means "at least one." *Crystal Semiconductor*, 246 F. 3d at 1347. In *Crystal Semiconductor*, the Court explained that "[t]his court has consistently emphasized that the indefinite articles 'a' or 'an,' when used in a patent claim, mean 'one or more' in claims containing open-ended transitional phrases such as 'comprising.' . . . . 'Under this conventional rule, the claim limitation 'a,' without more, requires at least one.'" *Id.* The amendment was not a substantive change and did not transform the meaning of the claim to somehow mean "the first master device' *alone* to generate the 'request'". Without any reference to "alone" in any of the claims, this Court will not reinterpret the Federal Circuit's

instruction that "a" means "at least one." Moreover, the Examiner's characterization of the rejection as an informality indicates a non-substantive impact on patentability. If the Examiner understood that curing the informality would materially change the patent claim's scope, it likely would not have described the rejection as such. Moreover, although "a" can mean "one" where the prosecution history necessitates such an interpretation, the prosecution history in this case does not reveal such an interpretation.

Here, the amendment did not narrow the claim scope. Accordingly, VLSI's DOE theory is not barred by amendment-based prosecution history estoppel.

2) VLSI's amendment to '759 patent claims does not trigger the application of argument-based prosecution history estoppel.

Argument-based estoppel arises when an applicant distinguishes prior art through argument (rather than amendment) made during prosecution. *Amgen*, 931 F.3d at 1159. To invoke argument-based estoppel, "the prosecution history must evince a clear and unmistakable surrender of subject matter." *Conoco, Inc. v. Energy & Env't Int'l, L.C.*, 460 F.3d 1349, 1364 (Fed. Cir. 2006). The clear and unmistakable standard is a high bar. *Silt Saver, Inc. v. Hastings*, No. 1:16-CV-1137-SCJ, 2017 U.S. Dist. LEXIS 216827, at *25 (N.D. Ga. Oct. 18, 2017). "The relevant inquiry is whether a competitor would reasonably believe that the applicant had surrendered the relevant subject matter." *Id.* "[T]he determinations concerning whether the presumption of surrender has arisen and whether it has been rebutted are questions of law for the court, not a jury, to decide." *Festo* Corp, 344 F.3d at 1368. The Court "do[es] not presume a patentee's arguments to surrender an entire field of equivalents through simple arguments and explanations to the patent examiner." *Conoco, Inc.*, 460 F.3d at 1364.

Intel asserts that argument-based prosecution history estoppel bars VLSI's equivalents theory because it clearly and unmistakably surrenders any claim that the "request" limitations can

be met in systems where a master device "selects the frequency based on a number of factors." ECF No. 593 at 15. Intel claims that the distinction VLSI drew between its claim and the Ansari reference to overcome a prior art rejection demonstrates that the selection of "frequency based on a number of factors" is not "a master device making a request" and requires that an input do more than "happen to cause" a change to the master device's frequency. *Id.* Consequently, Intel contends that VLSI inappropriately presented an equivalents theory barred by argument-based prosecution history estoppel because the accused Intel products evaluate "various factors" that may "happen to cause" a change in clock speed in deciding whether to change frequency. *Id.* at 16.

VLSI argues that the prosecution history does not evince clear and unmistakable surrender of its DOE theory. ECF No. 607 at 9. VLSI contends that the Intel's argument rests on an entirely different DOE theory than the one VLSI actually presented at trial. *Id.* Specifically, VLSI's theory turned on the combination of components that generate the "request" rather than the "request" itself, as Intel suggests. *Id.* Thus, VLSI claims to have distinguished the '759 Patent from Ansari because the reference disclosed a request from a master device that "happens to cause an arbiter to increase the bus speed" instead of a master device that causes a change in bus speed itself. *Id.* at 10. Further, VLSI argued that Intel's internal documents proved that the Accused Products fell within the scope of the limitation because they disclosed a ratio produced by a combination of components for modifying the clock frequency depending on the core's workload. *Id.* at 11.

The Court looks first to the argument made during prosecution of the '759 Patent. In response to the Examiner's prior art rejections, the Applicant explained that in Ansari a "master device seeking bus resources to initiate a transaction sends a bus request and a destination address to the bus arbiter so that the arbiter can determine a corresponding bus frequency." PTX-8-A.241-.242. The bus request in Ansari is sent by the master device to the arbiter to *access* the bus. *Id.*

Crucially, the "master device does not determine or request a desired bus frequency because it is the bus arbiter that determines the bus frequency based on various factors." *Id.* By contrast, the '759 Patent recites a first master device that provides a request to change the clock frequency of a high-speed clock. '759 Patent 8:52–55. The bus request to an arbiter causing *access* to the bus in Ansari is distinct from the bus request to *increase* the clock frequency in the '759 Patent. Thus, the Applicant distinguished the "request" from Ansari from the "request" in the '759 Patent.

The Court looks next to the DOE theory that VLSI presented at trial. Dr. Conte, VLSI's expert, testified to VLSI's infringement theory at trial. He explained that the core and its associated code in the programmable clock controller generate the "request." Sealed Trial Tr. 55:1-6; 53:14-56:3; ECF No. 553-02 PDX4.204-214. Intel mischaracterizes his testimony as a DOE opinion based on the claimed "request." Dr. Conte testified as to how the combination of the core ("first master device") and its code in the programmable clock controller ("PCU") provide the request. ECF No. 607 at 10. Specifically, Dr. Conte explained that the core sends Core_Active signals to the PCU [redacted]3-40:7; PTX-1805; *see also* Sealed Trial Tr. 42:13-43:4; ECF No. 553-02 PDX4.171-172. The PCU's "C0 residency counters" then measure the activity of the core, and those counters start counting when the core sends the Core_Active signal to the PCU. Trial Tr. 1419:2-18; ECF No. 553-03 PDX5.13. [redacted], the "P-Code" in the PCU sends a request for a higher or lower frequency. PTX-3484.3. [redacted] 553-02 PDX4.207; D-1154. Although the literal infringement opinion was based on the Core_Active signals, the DOE theory was predicated on the combination of the core's output and the P-Code. PTX-3484.3. Dr. Conte also supported his DOE opinion using the "function, way, result" test. Sealed Trial Tr., 55:1-6; ECF No. 553-02 PDX4.202. He explained that the difference

between Intel's products and the '759 Patent is "just a difference of where an engineer draws this [dotted] line . . . a design choice." Sealed Trial Tr., 55:12-17; ECF No. 553-02 PDX4.207, -.209.

Having reviewed the argument to the Examiner and the DOE theory presented at trial, the Court finds that argument-based estoppel does not apply. VLSI's conduct fails to rise to the level of a "clear and unmistakable surrender of subject matter." First, VLSI's DOE theory is sufficiently distinct from the arguments the Applicant made to the Examiner in distinguishing Ansari. The Applicant did not argue that that master device and arbiter together provide a request to change the clock frequency. Rather, the Applicant argued that the master device sends a bus request to the arbiter in order to access the bus. Nothing in the Applicant's argument disclaimed the idea that the core and its associated P-Code in the PCU could provide the request. VLSI's DOE theory turned on the components that provide the request in Intel's accused products, not the request itself, as Intel suggests. Second, even if Intel is correct that the Applicant's argument encompassed VLSI's DOE theory, there is simply not enough evidence of "clear and unmistakable surrender" of VLSI's DOE theory. Intel has failed to meet this high bar. Thus, this Court will not prevent VLSI from relying on its DOE theory on the ground of argument-based prosecution history estoppel.

B. The ensnarement doctrine does not bar VLSI's doctrine of equivalents theory.

"Ensnarement bars a patentee from asserting a scope of equivalency that would encompass, or 'ensnare,' the prior art." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 567 F.3d 1314, 1322 (Fed. Cir. 2009). That is, "there can be no infringement if the asserted scope of equivalency of what is literally claimed would encompass the prior art." *Wilson Sporting Goods Co. v. David Geoffrey & Assocs.*, 904 F.2d 677, 683 (Fed. Cir. 1990). Whether a proposed equivalent ensnares prior art is typically based on a "hypothetical claim analysis," which puts the burden on the patentee to identify a hypothetical claim that contains both the literal claim scope and the proposed

equivalent without ensnaring the prior art. *Intendis GMBH v. Glenmark Pharms. Inc.*, 822 F. 3d 1355, 1363 (Fed. Cir. 2016). However, a "hypothetical claim analysis is not the only method in which a district court can assess whether a doctrine of equivalents theory ensnares the prior art." *G. David Jang, M.D. v. Box. Sci. Corp.*, 872 F.3d 1275, 1285, n.4. (Fed. Cir. 2017). In the context of a hypothetical claim analysis, "[t]he burden of producing evidence of prior art to challenge a hypothetical claim rests with an accused infringer, but the burden of proving patentability of the hypothetical claim rests with the patentee." *Interactive Pictures Corp. v. Infinite Pictures, Inc.*, 274 F.3d 1371, 1380 (Fed. Cir. 2001)

As a preliminary matter, the parties dispute whether VLSI proposed a hypothetical claim and whether that disclosure was timely. Intel argues that the ensnarement doctrine bars VLSI's equivalents theory for the '759 Patent because VLSI failed to propose a hypothetical claim that does not ensnare the prior art. ECF No. 593 at 18. To suggest that the burden lies on VLSI to assert the defense, Intel points to a Northern District of California case stating that "(1) because the patent holder was on notice of the asserted ensnarement defense, the patent holder 'must articulate an adequate hypothetical claim'" as "a necessary step in the [doctrine of equivalents] infringement theory," and (2) by failing to take "this necessary step in its infringement theory, . . . patent owner too disclaims the theory." *Id.* at 19 (citing *Fluidigm Corp. v. IONpath, Inc.*, No. C 19-05639 WHA, 2021 WL 292033 (N.D. Cal. Jan. 28, 2021)). Intel proposes that the same outcome should apply to this case given that it notified VLSI of an ensnarement defense over a year before filing this motion. *Id.*

In response, VLSI notes that a hypothetical claim analysis is not required in assessing whether a DOE theory ensnares the prior art. ECF No. 607 at 13. Still, VLSI asserts that it did propose a hypothetical claim implicitly through Dr. Conte's testimony. *Id.* at 14. Specifically, Dr.

Conte testified that the accused products triggered application of DOE "by using the combination of a core and the PCU to provide a request" to modify a clock frequency. *Id.* VLSI asserts that Dr. Conte's testimony illustrated how the "request" limitation did not ensnare the prior art and provided Intel notice of a hypothetical claim supporting VSLI's DOE theory. *Id.* When a hypothetical claim is proposed, the accused infringer has the burden to challenge it. VLSI argues that although Intel referred to certain alleged prior art, it failed to provide a detailed analysis satisfying its affirmative burden of production. *Id.*

The Court finds that a hypothetical claim was not required for this Court to determine whether VLSI's DOE theory ensnares the prior art. *Jang*, 872 F.3d at 1285, n.4; see also *Conroy v. Reebok Int'l, Ltd.*, 14 F.3d 1570, 1577 (Fed. Cir. 1994) ("While the hypothetical claim analysis is a useful methodology because the clear step-by-step process facilitates appellate review, nothing in *Wilson* mandates its use as the only means for determining the extent to which the prior art restricts the scope of equivalency that the party alleging infringement under the doctrine of equivalents can assert."). Still, the Court notes that VLSI asserted a hypothetical claim, and its disclosure was timely. The parties in this case expressly agreed to defer for submission any proposed findings of fact and conclusions of law relating to Intel's ensnarement defense. ECF No. 398-02. In fact, it is commonplace for courts to accept hypothetical claims after a jury has rendered a verdict. *See Jang*, 872 F.3d at 1285 (district court considered hypothetical claims proposed by plaintiff for the first time in a post-verdict hearing). VLSI's hypothetical claim in its proposed findings of fact is thus timely. Intel nevertheless claims to have suffered prejudice from this post-verdict disclosure, but this Court finds that Intel had sufficient notice of VLSI's hypothetical claim. Dr. Conte's testimony that the accused products invoked the doctrine of equivalents "by using a combination of a core and the PCU to provide the request" to modify a clock frequency was

sufficiently detailed to provide timely notice to Intel of VLSI's DOE theory. Intel had time to take discovery on this issue and could have challenged the DOE theory during Dr. Conte's deposition. Any arguments about untimeliness and prejudice are unpersuasive.

Notwithstanding the lack of a hard-and-fast requirement for a hypothetical claim analysis, VLSI contends that its hypothetical claim is also patentable in view of the Terrell, Ansari, and Yonah references. ECF No. 607 at 15–17. VLSI's proposed hypothetical claim, which corresponds to claim 14 of the '759 Patent, is below:

> Hypothetical Claim. A system comprising: a bus capable of operation at a variable clock frequency; a first master device coupled to the bus, the first master device or the first master device and its associated code in a programmable clock controller configured to provide a request to change a clock frequency of a high-speed clock in response to a predefined change in performance of the first master device, wherein the predefined change in performance is due to loading of the first master device as measured within a predefined time interval; and the ~~a~~ programmable clock controller having an embedded computer program therein, the computer program including instructions to: receive the request provided by the first master device or the first master device and its associated code in the programmable clock controller; provide the clock frequency of the high-speed clock as an output to control a clock frequency of a second master device coupled to the bus in response to receiving the request provided by the first master device or the first master device and its associated code in the programmable clock controller; and provide the clock frequency of the high-speed clock as an output to control the variable clock frequency of the bus in response to receiving the request provided by the first master device or the first master device and its associated code in the programmable clock controller.

Intel contends that VLSI's hypothetical claim improperly ensnares prior art for four reasons. ECF No. 616 at 8. First, Intel alleges that VLSI's hypothetical claim fails to cover the full scope of its equivalents theory because it provides periodically sampled data continuously, not "in response to a predefined change in performance." *Id.* Second, Intel claims that VLSI failed to address several prior art references Intel identified as ensnared prior art during discovery. *Id.* Third, Intel states that VLSI improperly alleges that the Terrell reference does not expressly disclose a

requirement for teaching a system bus. *Id.* Lastly, Intel argues that VLSI's hypothetical claim ensnares the Ansari reference when combined with Terrell. *Id.*

It is unclear whether Intel has met its burden in producing prior art to challenge the hypothetical claim. Its Motion focuses on the timeliness of disclosure and prejudice, and its Reply devotes only one and a half pages to the hypothetical claim analysis. Still, the Federal Circuit has indicated this is a burden of production, and Intel at the very least has produced, albeit through vague citations, three references that this Court will consider—Terrell, Ansari, and Yonah. VLSI has the burden to prove that the hypothetical claim is patentable.

VLSI first argues that the hypothetical claim is patentable over Terrell, alone or in combination. ECF No. 607 at 16. Several elements of the hypothetical claim are lacking in Terrell. Among these include the fact that Terrell does not teach the limitation of providing the clock frequency of the high-speed clock as an output to control the variable clock frequency of the bus. Dr. Conte testified that Terrell lacks this element of controlling the clock frequency of the bus, and Intel's expert, Dr. Dirk Grunwald, admitted that Terrell does not teach this limitation. ECF No. 608-3 ¶ 515. Without that limitation, the hypothetical claim cannot encompass Terrell.

VLSI next argues that the hypothetical claim is patentable over Ansari. *Id.* at 16–17. There are at least three distinctions between the hypothetical claim and Ansari. As explained above, Ansari discloses a master device that makes a request to the bus arbiter to access the bus. ECF No. 608-3. The hypothetical claim, by contrast, recites "the first master device or the first master device and its associated code in a programmable clock controller configured to provide a request to change a clock frequency of a high-speed clock in response to a predefined change in performance of the first master device." The hypothetical claim does not request access, but rather requests an increase in clock frequency of a high-speed clock or the bus. Another distinction is that the Ansari

master device makes a request to access the bus and does not make request "in response to a predefined change in performance." ECF 608-4, col. 11:4–9. By contrast, the hypothetical claim discloses a request that is provided "in response to a predefined change in performance." Both of those distinctions were made by the Applicant during the prosecution of the '759 Patent. ECF No. 607. Lastly, the hypothetical claim recites "provide the clock frequency of the high-speed clock as an output to control a clock frequency of a second master device coupled to the bus in response to receiving the request." PTX-5, col. 8:63-67 (claim 14); *see also* col. 9:26-30 (claim 18). Ansari does not disclose this controlling the clock frequency of a second master device in response to receiving a request from the first master device. ECF No. 607 at 17.

VLSI also argues that the hypothetical claim is patentable over Yonah. ECF No. 607 at 17–18. The Yonah processor was discussed at trial. When questioned about Yonah, Dr. Conte testified that the Yonah processor did not have "a programmable clock controller having an embedded computer program therein, the computer program including instructions to: receive the request . . . ; provide the clock frequency of the high-speed clock as an output to control a clock frequency of a second master device coupled to the bus . . . ; and provide the clock frequency of the high-speed clock as an output to control the variable clock frequency of the bus." Trial Tr. [Conte] 1410:12-20; *see also* Trial Tr. 1412:17-1417:20. By contrast, the hypothetical claim recites this programmable clock controller with an embedded program that includes instructions. At trial, the jury found that Yonah did not anticipate the claims of the '759 Patent. ECF No. 564 at 6.

This Court finds that neither of the three prior art relied on by Intel ensnare Dr. Conte's DOE infringement analysis. First, the disclosed limitation does not ensnare Ansari. One such distinction is that the master device in Ansari makes a request to the bus arbiter to *access* the bus 620 to initiate a transaction, but the master device in the hypothetical claim makes a request to

increase clock frequency of a high-speed clock or the bus. Similarly, Terrell fails to teach controlling the clock frequency of the high-speed clock in the hypothetical claim. Lastly, Yonah lacks the programmable clock controller that is recited in the hypothetical claim. VLSI has met its burden to show that its hypothetical claim is patentable over the prior art. Therefore, this Court holds that VLSI's equivalents theory does not ensnare the prior art.

C. The claim vitiation doctrine does not bar VLSI's doctrine of equivalents theory.

Another limit on the doctrine of equivalents is the "all elements" rule. Under the doctrine of equivalents, "the range of equivalents cannot be divorced from the scope of the claims." *Vehicular Techs. Corp. v. Titan Wheel Int'l, Inc.*, 212 F.3d 1377, 1382 (Fed. Cir. 2000). "[I]f a theory of equivalence would entirely vitiate a particular claim element, partial or complete judgment should be rendered by the court . . . ." *Warner-Jenkinson Co. v. Hilton Davis Chem. Co.*, 520 U.S. 17, 39 n. 8 (1997). The "all elements" rule precludes using the doctrine of equivalents when "a limitation would be read completely out of the claim—i.e., the limitation would be effectively removed or 'vitiated.'" *DePuy Spine*, 469 F.3d at 1017.

Intel's final argument is that VLSI's proposed equivalent improperly vitiates the requirements of the asserted claims under the "all elements" rule. ECF No. 593 at 19. According to Intel, the claim requires not only providing the "request" but also specifies that the request should be generated "in response to a predefined change in performance of the first master device." *Id.* at 20. But Dr. Conte testified that its proposed equivalent, C0 residency data, is sent without regard to a change in performance, not in response to a change in performance. *Id.* Because VLSI's expert agreed that C0 residency data is not the claimed "request," Intel argues that any equivalents theory based on such data must fail. *Id.* Intel argues that such a reading would vitiate the claim

requirement that "requests" are sent "in response to a predefined change in performance of the first master device." *Id.*

There are two problems with Intel's claim vitiation argument. First, Intel mischaracterizes the law. Claim vitiation "is not an exception or threshold determination that forecloses resort to the doctrine of equivalents, but is instead a legal conclusion of a lack of equivalence based on the evidence presented and the theory of equivalence asserted." *Bio-Rad Lab'ys, Inc. v. 10X Genomics Inc.*, 967 F.3d 1353, 1366–67 (Fed. Cir. 2020). At its core, claim vitiation is a conclusion that "no reasonable jury could conclude that an element of an accused device is equivalent to an element called for in the claim, or that the theory of equivalence to support the conclusion of infringement otherwise lacks legal sufficiency." *DePuy Spine*, 469 F.3d at 1018–19. Intel's claim vitiation arguments attempt to substitute de novo review for substantial evidence review, which places a heavy burden on Intel to prove that the jury's verdict is not supported by substantial evidence. Intel has failed to meet that burden. Intel presents no compelling reason to believe that substantial evidence did not support the jury's verdict.

Second, Intel's claim vitiation argument mischaracterizes VLSI's expert testimony. Contrary to Intel's assertion, Dr. Conte did not opine that C0 residency counters are "requests." Rather, he explained that the C0 residency counters count how long the Core_Active signal from the core is active. Trial Tr. 1419:2-18; ECF No. 553-03 PDX5.13. [redacted] then the combination of the P-Code in the PCU and the core (which sends the Core_Active signals) produce the "request" for a change in frequency. Sealed Trial Tr., 56:7-57:7; D-1154. In sum, Dr. Conte's testimony established that under the doctrine of equivalents, (1) the core sends a Core_Active signal in response to a "predefined change in performance" of the core, (2) the Core_Active signal

starts the [redacted], and (3) the output of processing of the Core_Active signals constitutes a "request." ECF No. 607 at 20.

This Court agrees with VLSI that its doctrine of equivalents theory does not read out any claim limitations. The limitations that Intel complains are vitiated are: (1) the requirement to provide the "request" and (2) that the request should be generated "in response to a predefined change in performance of the first master device." First, VLSI's DOE theory includes a requirement to provide a "request" through the combination of the P-Code in the PCU and the output of the Core_Active signals. Second, VLSI's DOE theory does generate a request "in response to a predefined change in performance of the first master device." VLSI proved that the Core_Active signals are sent "whenever the core becomes active." Trial Tr. 488:4-7. Dr. Conte's testimony confirms this: "Q. Are Core_Active signals sent periodically? A. No. Q. When are they sent? A. They're sent whenever the core becomes active." *Id.* Intel cherry picks Dr. Conte's testimony about periodic signals and Core_Active signals to try and reshape VLSI's DOE theory into something it is not. Accordingly, this Court holds that claim vitiation under the "all elements" rule does not apply to VLSI's DOE theory.

IV. CONCLUSION

This Court finds that prosecution history estoppel, the ensnarement doctrine, and claim vitiation do not preclude VLSI's DOE theory. Therefore, Intel's Motion for Judgment of No Infringement of the '759 Patent Under the Doctrine of Equivalents is **DENIED**.

SIGNED this 18th day of March, 2022.

ALAN D ALBRIGHT
UNITED STATES DISTRICT JUDGE