UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

VLSI TECHNOLOGY LLC, *Plaintiff,*	§	
	§	
	§	**CIVIL NO. 6:21-CV-057-ADA**
v.	§	
	§	
INTEL CORPORATION, *Defendant.*	§	
	§	

ORDER DENYING DEFENDANT INTEL'S RULE 50(B) MOTION FOR JUDGMENT AS A MATTER OF LAW

Before the Court is Defendant Intel Corporation's ("Intel") Rule 50(b) Motion for Judgement as a Matter of Law ("JMOL"). ECF No. 591. Plaintiff VLSI Technology LLC ("VLSI") filed its Response on May 7, 2021. ECF No. 603. Intel then filed its Reply on May 21, 2021. ECF No. 615. Intel asks this Court for a judgment of no infringement for U.S. Patent Nos. 7,523,373 and 7,725,759, a judgment of invalidity for the asserted claims of the '759 patent, and a judgment of no damages. *Id.* After considering the parties' briefs and relevant law, the Court **DENIES** Defendant's Motion on all counts for the reasons below.

I. BACKGROUND

VLSI filed its suit for patent infringement on April 11, 2019. ECF No. 1 at 1. In its Complaint, VLSI accused Intel Corporation ("Intel") of infringing U.S. Patent Nos. 7,523,373 ("the '373 Patent"), and 7,725,759 ("the '759 Patent"). On March 2, 2021, following a six-day trial, the jury found that Intel literally infringed claims 1, 5, 6, 9, and 11 of the '373 Patent, and infringed claims 14, 17, 18, and 24 of the '759 patent under the doctrine of equivalents. ECF No. 564 at 2–3. The jury also found that Intel had not met its burden to prove that claims 14, 17, 18, and 24 of the '759 patent were invalid. *Id.* at 5. The jury awarded VLSI a total of $2.175 billion in

damages: a $1.5 billion lump sum for infringement of the '373 patent and a lump sum of $675 million for infringement of the '759 patent. *Id.* at 6–7. Intel subsequently filed a Rule 50(b) Motion for JMOL on April 9, 2021. ECF No. 591.

II. LEGAL STANDARD

A court may grant JMOL against a prevailing party only if a reasonable jury would not have a legally sufficient evidentiary basis to find for the non-moving party on that issue. Fed. R. Civ. P. 50(a)(1). In deciding a renewed JMOL motion, a "court must draw all reasonable inferences in favor of the nonmoving party, and it may not make credibility determinations or weigh the evidence." *Taylor-Travis v. Jackson State University*, 984 F.3d 1107, 1112 (5th Cir. 2021). The court must disregard all evidence favorable to the moving party that the jury is not required to believe. *Id*. This is because "[c]redibility determinations, the weighing of the evidence, and the drawing of legitimate inferences from the facts are jury functions, not those of a judge." *Wellogix, Inc. v. Accenture, L.L.P.*, 716 F.3d 867, 874 (5th Cir. 2013).

Courts grant JMOL for the party bearing the burden of proof only in extreme cases, when the party bearing the burden of proof has established its case by evidence that the jury would not be at liberty to disbelieve, and the only reasonable conclusion is in its favor. *Mentor H/S, Inc. v. Medical Device Alliance, Inc.*, 244 F.3d 1365, 1375 (Fed. Cir. 2001). JMOL is inappropriate if the record evidence is such that reasonable and fair-minded men in the exercise of impartial judgment might reach different conclusions. *Laxton v. Gap Inc.*, 333 F.3d 572, 579 (5th Cir. 2003).

A jury verdict must stand unless there is a lack of substantial evidence, in the light most favorable to the successful party, to support the verdict. *Am. Home Assur. Co. v. United Space Alliance, LLC*, 378 F.3d 482, 487 (5th Cir. 2004). Substantial evidence is more than a scintilla, but less than a preponderance. *Nichols v. Reliance Standard Life Ins. Co.*, 924 F.3d 802, 808 (5th Cir.

2019). Thus, JMOL must be denied if a jury's verdict is supported by legally sufficient evidence that amounts to more than a mere scintilla. *Laxton*, 333 F.3d at 585.

III. DISCUSSION

I. Substantial Evidence Supports the Jury's Infringement Findings for the '373 and '759 Patents.

The jury found that the C6 SRAM power multiplexer in Intel's accused products literally infringed the '373 patent. It also found that the Speed Shift feature in Intel's accused products infringed the '759 patent under the doctrine of equivalents. Intel seeks JMOL on those findings.

A. Substantial Evidence Supports the Jury's Infringement Verdict For the '373 Patent.

1. Substantial Evidence Supports the Jury's Infringement Finding for The "Minimum Operating Voltage" Limitations.

The asserted method claims of the '373 Patent require "storing the value of the minimum operating voltage" of a memory. '373 Patent 13:13–14. The asserted apparatus claims require "a memory location that stores a value representative of the minimum operating voltage." *Id.* at 13:63–64. The jury found that the C6 SRAM power multiplexer in Intel's Haswell and Broadwell products infringe on claims 1, 5, 6, 9, and 11 of the '373 Patent. ECF No. 591 at 2. At trial, VLSI identified the accused "memory" as the C6 SRAM in Intel's products and the accused "value of the minimum operating voltage" as being stored in Intel's RING_RETENTION_VOLTAGE fuse. *Id.* Intel argues that the accused products do not store the "minimum operating voltage" and therefore do not infringe on the '373 Patent. *Id.*

The Court first looks to the evidence that VLSI presented at trial to determine whether there is substantial evidence to support the jury's verdict. VLSI argues that it presented substantial evidence that the accused "memory" is the C6 SRAM, and the "minimum operating voltage of the memory" is the RING_RETENTION_VOLTAGE. ECF No. 603 at 1–2. VLSI points to Intel

internal documents that indicate that the "[redacted]" *Id.* at 2 (citing PTX-3662.702; PTX-3851.1280). Dr. Thomas M. Conte, VLSI's infringement expert, testified that Intel's use of the term "retention" is synonymous with "memory" and that [redacted] applies to C6 SRAM memory. 2/23 Sealed Trial Tr. 5:1-6. He then explained that the RING_RETENTION_VOLTAGE stores the minimum retention voltage for the C6 SRAM. *Id.* at 75:23-76. Dr. Conte further explained that the [redacted] "defines the lowest safe voltage" and thus "the minimum operating voltage." *Id.* at 4:19-25, 9:10-22. VLSI corroborated his testimony with source code in the Haswell and Broadwell products. 3/1 Trial Tr. 1451:4-1452:5.

The Court looks next to Intel's arguments that the above evidence fails to show that its products satisfy the "minimum operating voltage" limitation. According to Intel, RING_RETENTION_VOLTAGE is merely a voltage at which the C6 SRAM *can* retain data, not necessarily the minimum voltage at which data retention occurs as the asserted claims require. ECF No. 591 at 2. Intel contends that Dr. Conte confirmed as much when he admitted that the RING_VF_VOLTAGE_0 fuse value—which is below the RING_RETENTION_VOLTAGE voltage value—reflects a voltage that is "actually used" in the accused products. *Id.* at 5. Because the C6 SRAM, as a ring component, operates at voltages below the RING_RETENTION_VOLTAGE, Intel alleges that no reasonable jury could find that the RING_RETENTION_VOLTAGE fuse stores the C6 SRAM's minimum operating voltage. *Id.* Further, Intel contends that there is no relationship between RING_RETENTION_VOLTAGE and the C6 SRAM *specifically* as opposed to the *entire* ring domain because the voltage applies *generally* to the ring domain, which contains multiple components beyond the C6 SRAM. *Id.*

The first problem with Intel's argument is that it misrepresents Dr. Conte's testimony about the RING_VF_VOLTAGE_0 fuse value. Intel argues that the RING_RETENTION_VOLTAGE cannot store the C6 SRAM's minimum operating voltage because, as Dr. Conte admitted, the accused products "actually use" the RING_VF_VOLTAGE_0 value, which is a lower voltage. ECF No. 591 at 5. But even if the RING_VF_VOLTAGE_0 *fuse* value is below the RING_RETENTION_VOLTAGE *voltage* value, there is still a factual dispute for the jury to resolve as to whether the ring operates at the RING_VF_VOLTAGE_0 *fuse* value. Dr. Conte testified that the ring operates at a higher operating voltage level that is derived from the fuse value after inverse temperature dependence compensations calculations are applied. 3/1 Trial Tr. 1425:1-1432:5, 1434:9-1437:7, 1450:8-1452:12. Dr. Conte explained that Intel's witnesses did not account for the inverse temperature dependence compensations when comparing the RING_VF_VOLTAGE_0 and the RING_RETENTION_VOLTAGE. *Id.* His testimony thus shows that the operating voltage from the RING_VF_VOLTAGE_0 fuse value is higher than the RING_RETENTION_VOLTAGE. This testimony was also corroborated with multiple Intel internal documents. One such example is an Intel specification that shows [redacted] [redacted] *Id.* at 1425:1-1426:20. He came to this conclusion after reviewing Intel's source code for the accused products. *Id.* at 1451:4-1452:5. The jury was free to credit that testimony over Intel's witnesses, particularly after Intel's expert was impeached with Intel documents. ECF No. 603 at 6. As VLSI indicated, Intel's internal documents described RING_RETENTION_VOLTAGE as the [redacted] for "memory", or the C6 SRAM, where the [redacted] is the lowest safe voltage and thus the minimum operating voltage. ECF No. 603 at 2.

The second problem with Intel's argument is that it mischaracterizes the relationship between the RING_RETENTION_VOLTAGE and the C6 SRAM. As VLSI argues, the '373 Patent claims do not recite the word "specifically" to require that the RING_RETENTION_VOLTAGE apply to the C6 SRAM specifically. ECF No. 603 at 2. Nor does the '373 Patent bar the "minimum operating voltage of the memory" from applying to parts in addition to the memory. ECF No. 603 at 2. The patent claims draw no distinction between a specific or general relationship connecting the minimum operating voltage to the C6 SRAM. Instead, the '373 Patent claims include the transition term "comprising", and it is black-letter law that "[t]he transitional term 'comprising' . . . is inclusive or open-ended and does not exclude additional, unrecited elements." *CollegeNet, Inc. v. ApplyYourself, Inc.*, 418 F.3d 1225, 1235 (Fed. Cir. 2005). Because RING_RETENTION_VOLTAGE applies to both the "LLC" and C6 SRAM memories, VLSI concludes that RING_RETENTION_VOLTAGE is the minimum operating voltage of the C6 SRAM. *Id.* VLSI presented several sources supporting its claim, including multiple Intel documents and source code reviews. *Id.* at 6. The jury ultimately believed VLSI's expert over Intel's witnesses.

This Court agrees that VLSI has presented substantial evidence supports the jury's infringement finding for the "minimum operating voltage" limitations. VLSI's presentation of Dr. Conte's expert testimony, Intel internal documents, and Dr. Conte's source code analysis provided substantial evidence to support the jury's infringement finding. Although Intel makes several distinct but related arguments that it cannot infringe on this limitation, the Court finds that VLSI presented substantial evidence to the contrary. Intel's arguments fall short of the high bar required for JMOL, which demands a showing that the jury would not be at liberty to disbelieve Intel's non-infringement theory considering the evidence. Instead, Intel's internal documentation and claim

construction argument reinforces the jury's infringement verdict as a reasonable one. Accordingly, this Court denies Intel's motion for JMOL on this ground.

2. Substantial Evidence Supports the Jury's Infringement Finding for the "When" Limitations.

The asserted method claims recite limitations "providing" "as the operating voltage of the memory" (1) "the first regulated voltage . . . when the first regulated voltage is at least the value of the minimum operating voltage," and (2) "the second regulated voltage . . . when the first regulated voltage is less than the value of the minimum operating voltage." '373 Patent 13:20–28, 41–44, 45–52. The asserted apparatus claims also require "a power supply selector that supplies" as the operating voltage of the memory (1) "the first regulated voltage ... when the first regulated voltage is at least the minimum operating voltage" and (2) "the second regulated voltage ... when the first regulated voltage is below the minimum operating voltage." *Id.* at 13:59–14:15, 14:20–23. At trial, VLSI argued that the "first regulated voltage" was Intel's VCCR, the "second regulated voltage" is the VCCIO, and the minimum operating voltage is RING_RETENTION_VOLTAGE.

Intel alleges that VLSI introduced no evidence that the RING_RETENTION_VOLTAGE fuse value is ever used to guide "when" VCCR and VCCIO are supplied. ECF No. 591 at 6. Intel alleges that VLSI ignores the evidence that VCCR is supplied to the C6 SRAM even when VCCR is below RING_RETENTION_VOLTAGE conditions that are the opposite of what the claims require. ECF No. 615 at 4. To avoid confronting this, Intel claims VLSI improperly characterizes the plain meaning of the "when" limitations as an untimely claim construction dispute. *Id.*

VLSI responds that it offered substantial evidence that these limitations are met. Dr. Conte demonstrated that the "first regulated voltage" (VCCR) is supplied when the first regulated voltage is at least the value of RING_RETENTION_VOLTAGE, the minimum operating voltage. 2/23 Sealed Trial Tr. 13:2-16. He explained this using a demonstrative that showed the jury how VCCR

is supplied when it is at least the minimum voltage. PDX4.79. He also confirmed this infringement argument using Intel's documents. 2/23 Sealed Trial Tr. 13:23-14:11.

This Court agrees that VLSI presented sufficient evidence to support the jury's infringement finding. Intel argues VLSI introduced "no evidence" that the RING_RETENTION_VOLTAGE fuse value is ever used to guide "when" the "first regulated voltage" and "second regulated voltage" are supplied ECF No. 591 at 6. Yet Dr. Conte demonstrated that RING_RETENTION_VOLTAGE acts as the threshold for when the voltages are supplied. *Id.* at 7. He supported his testimony with Intel documents, which together provide substantial evidence that Intel met this limitation. Intel rebuts by pointing to an admission by VLSI's expert that he did not refer to RING_RETENTION_VOLTAGE in describing multiplexer operation, but this argument merely introduces a factual dispute. The significance of this dispute is questionable, given that the claims only require that the "first regulated voltage" rise to at least the minimum operating voltage rather than require the minimum operating voltage "to guide." ECF No. 603 at 7. At best, Intel provides evidence of a legitimate factual dispute; at worst, Intel attempts to prevail with a red herring. In either case, Intel petitions this Court to subvert the jury's role by weighing the evidence and making credibility determinations. That is not the Court's task at this stage. See *Wellogix*, 716 F.3d at 874. Accordingly, this Court preserves the jury's verdict and declines JMOL on this ground.

3. Substantial Evidence Supports the Jury's Infringement Finding for The "First Regulated Voltage" And "Functional Circuit" Limitations.

The asserted method claims recite that "while the second regulated voltage is provided as the operating voltage of the memory, the first regulated voltage is provided to the functional circuit." '373 Patent 13:26–28, 41–44, 45–52. The asserted apparatus claims "a power supply

selector" that "supplies the second regulated voltage" to the memory "while the second regulated voltage is supplied as the operating voltage, the circuit uses the first regulated voltage." *Id.* at 14:8–15, 14:20–23. At trial, VLSI identified Intel's VCCR as the "first regulated voltage" and the VCCIO as the "second regulated voltage." ECF No. 591 at 7.

Intel contends that the functional circuit in its products are not provided with and do not use the first regulated voltage while the second regulated voltage is provided to the memory. *Id.* at 6. Intel's witnesses testified the "first regulated voltage" is actually unregulated and the ring domain components are inoperable during the state in which the "second regulated voltage" powers the C6 SRAM bitcells. *Id.* Moreover, Intel contends that Dr. Conte admitted that the [redacted] *Id.* Thus, Intel alleges that VLSI identifies no evidence supporting its claim that VCCR is regulated during Package C7. *Id.* Intel complains that VLSI's reliance on one Intel document does not account for its engineer's testimony that the "first regulated voltage" is not actually regulated during Package C7. ECF No. 614 at 4. Consequently, Intel asserts JMOL is required because no reasonable jury could find that the "first regulated voltage" is regulated and provided to or used by a "functional circuit" while the "second regulated voltage" is "provided" or "supplied" to what VLSI identifies as the claimed "memory." ECF No. 591 at 8.

To rebut, VLSI cites Dr. Conte's testimony that the "first regulated voltage" is regulated, controlled, and non-zero for the ramp-down period while the "second regulated voltage" is provided to the memory. 2/23 Sealed Trial Tr. 19:16-20:2. Dr. Conte further testified that the circuit is using the voltage and that it is a regulated voltage for the entirety of the Package C7 state. *Id.* VLSI corroborates Dr. Conte's testimony with Intel's internal documents that show that the

[redacted]

see also 2/25 Trial Tr. 870:20–872:25. VLSI argues that Dr. Conte's testimony, coupled with Intel's documents, are substantial evidence that supported the infringement verdict. ECF No. 603 at 8.

This Court agrees with VLSI that substantial evidence supports the jury's infringement finding. JMOL is inappropriate if the record evidence is such that reasonable and fair-minded people in the exercise of impartial judgment might reach different conclusions. *Laxton*, 333 F.3d at 579. Here, Intel presents several points on which expert testimony conflict as to whether the accused products supply a "first regulated voltage" and "second regulated voltage … when the first regulated voltage is below the minimum operating voltage." For example, Intel points out that "the first regulated voltage" is not regulated at all, which directly contradicts Dr. Conte's testimony that the "first regulated voltage" is regulated, controlled, and non-zero. ECF No. 603 at 8. Intel's counters that VLSI lodged an unsubstantiated claim by basing it on an Intel document with no reference to regulation. ECF No. 614 at 4.

This Court's role, however, is not to resolve factual disputes, but to consider whether the evidence mandates non-infringement as the only reasonable conclusion. At best, Intel has demonstrated that there is a legitimate factual dispute over which reasonable minds could differ, rendering JMOL improper. Intel's core contention is that the relevant evidence failed to provide a sound basis for the jury's verdict because it clearly shows, among other things, that the "first regulated voltage" is unregulated. But Intel takes for granted that the jury need only base its verdict on legally sufficient evidence amounting to more than a mere scintilla. The conflicting expert testimonies satisfy that evidentiary standard. Intel's JMOL on this ground is therefore denied.

B. Substantial Evidence Support's The Jury's Doctrine of Equivalents Infringement Verdict for the '759 Patent.

VLSI presented both literal and doctrine of equivalents infringement theories on the '759 patent's "request" limitation. The jury found that the Speed Shift feature in Intel's products infringes multiple claims of the '759 patent under the doctrine of equivalents. Intel argues, however, that JMOL of no infringement should enter because that verdict is contrary to law and not supported by substantial evidence. ECF No. 591 at 8. Intel makes several legal arguments as to why VLSI's doctrine of equivalents claim should be barred. These include prosecution history estoppel and claim vitiation. *Id.* at 9–10. The Court does not address those arguments in this opinion because it already addressed them in its Order denying Intel's Motion for Judgment of No Infringement Under the Doctrine of Equivalents. *See* ECF No. 685. Those arguments are moot. Still, Intel argues that JMOL should be granted because no reasonable juror could have found infringement under the doctrine of equivalents.

In response, VLSI argues that there was substantial evidence sufficient for a reasonable jury to find infringement. ECF No. 603 at 9. But the jury did not find that Intel literally infringed. ECF No. 615 at 5. Whether there was substantial evidence supporting VLSI's rejected claim of literal infringement is irrelevant. To overturn the jury's rejection of its literal infringement claim, VLSI would have had to show that there was no substantial evidence from which a jury could reasonably find non-infringement. *Id.* VLSI has not attempted to meet that burden. *Id.* Therefore, this Court maintains the jury's verdict that the accused products infringe under the doctrine of equivalents and not under literal infringement.

1. Substantial Evidence Supports the Jury's Infringement Finding for the "Request" Limitation.

The '759 Patent relates to the controlling clock frequency in an electronic device. The '759 Patent discloses and claims a system in which a first master device of a plurality of master devices provides a "request" to change a clock frequency of a high-speed clock "in response to a predefined change in performance of the first master device." '759 Patent 7:66–8:15. A "programmable clock controller" receives this "request" and provides outputs to independently control (1) a clock frequency of a second master device coupled to a bus, and (2) a variable clock frequency of the bus. *Id.* VLSI asserted that Intel's Speed Shift feature infringed on claims 14, 17, 18, and 24 of the '759 Patent.

The Court looks first to VLSI's doctrine of equivalents theory and the evidence it used to support its infringement claim. Dr. Conte testified that the combination of core 1 ("first master device") and core 1's associated code in the PCU ("programmable clock controller") provides the claimed "request" in the '759 Patent. Sealed Trial Tr. 55:1-11; 53:14-56:3. Specifically, he explained that the core sends a Core_Active signal to the PCU whenever the core becomes active. Trial Tr. 1419:2-18; 488:4-7. C0 residency counters, which are counters in the PCU, measure the activity of the core over a predefined time interval when the core is active. *Id.* at 1419:12–18. [redacted] generates a "request" for a higher or lower frequency. Sealed Trial Tr., 54:9-22; ECF No. 553-02 PDX4.205-208, PDX4.210. VLSI's literal infringement theory of "request" was based on the Core_Active signals, but its equivalents theory was based on the output of the core in combination with the code in the PCU.

The Court looks next to Intel's arguments that the above evidence fails to show that its products satisfy the "request" limitations. Intel asserts two reasons as to why its products cannot

meet the "request" limitations. ECF No. 591 at 10. First, the C0 residency counters in Intel's products are [redacted]" and are not sent "in response to a predefined change in performance" as the claims require. *Id.* Intel claims that Dr. Conte admitted that C0 residency data is "[redacted]" and "[redacted]", thus contradicting the claims. *Id.* Second, Intel alleges that VLSI's equivalents theory is inconsistent with the claim, which requires the "request" to be (1) "provided" or "sent" by the "first master device" and (2) "received" by the "clock controller." *Id.* Dr. Conte testified that the "request" in Intel's products is provided by the combination of core and its associated P-code in the PCU ("the first master device"). *Id.* at 11. But Intel argues that this is improper because the claims do not allow the same component to both provide and receive the request. *Id.* Thus, Intel argues that no reasonable jury could find the "request" limitations met under the doctrine of equivalents. *Id.*

There are several problems with Intel's argument. First, Intel mischaracterizes Dr. Conte's testimony by claiming that C0 residency information occurs "[redacted]" and "[redacted]" ECF No. 591 at 9. When asked whether his testimony about period signals applies to the Core_Active requests, Dr. Conte responded in the negative and further clarified that a [redacted]. ECF No. 603 at 10. Thus, the C0 residence information is sent "in response to" changes in the Core_Active signals sent to the PCU. Dr. Conte testified that the C0 residency counters [redacted] depending on changes in Core_Active signals, which reflect changes in core performance. ECF No. 603 at 10. Therefore, Dr. Conte's testimony cannot be understood to vitiate the "request" limitation by proving that C0 residency information is completely untethered to core performance, as Intel suggests.

Second, Intel's argument that VLSI's equivalents theory is inconsistent with the claims misconstrues Dr. Conte's testimony. Dr. Conte did not testify that the claims require the PCU to send and receive the claimed "request." *Id.* Instead, he testified that a separated core in conjunction with the PCU's internal P-Code can generate the request received by the [redacted]. 2/23 Sealed Trial Tr. 55:1-19, 57:11-15. Intel understands this as suggesting that the PCU both provides and receives the request, but VLSI's demonstrative graphically depicts the core and PCU as separate entities. *Id.* Dr. Conte distinguished the core and PCU when he testified that "the core and Core 1's P-Code" and "[redacted]" provided and received the request, respectively. *Id.* Moreover, to the extent Intel contends the "first master device" and "programmable clock controller" must always comprise entirely separate and distinct circuits, Intel appears to be asking this Court for a new claim construction. Even if this Court accepts Intel's characterization of the claims, Intel cannot prevail because it ultimately proposes a new claim construction, which it waived by omission. By neglecting to raise the issue to this Court in its Rule 50(a) motion, Intel has waived its right to bring a Rule 50(b) motion on this ground. And the Federal Circuit has held that the "doctrine of equivalents does not require a one-to-one correspondence between the accused device and that disclosed in the patent." *Intel Corp. v. ITC*, 946 F.2d 821, 832 (Fed. Cir. 1991); *see also Ethicon Endo-Surgery, Inc. v. U.S. Surgical Corp.*, 149 F.3d 1309, 1320 (Fed. Cir. 1998) ("[o]ne-to-one correspondence of components is not required, elements or steps may be combined without ipso facto loss of equivalency.").

This Court agrees with VLSI that substantial evidence supported the jury's finding that the Speed Shift feature satisfied the "request" limitation under the doctrine of equivalents. Intel claims JMOL of no infringement is proper for two reasons, namely that expert testimony vitiated the "request" limitation, and that the expert proposed an equivalents theory inconsistent with the claim.

But as explained above, Intel's arguments fail on both points. VLSI's presentation of Dr. Conte's testimony was sufficient to support a finding that the output of the core in combination with the code in the PCU provides the claimed "request."

2. Substantial Evidence Supports the Jury's Infringement Finding for the "Provide . . . As An Output to Control" Limitations.

Claims 14 and 17 require "provid[ing] the clock frequency of the high-speed clock as an output to control" both "a clock frequency of a second master device" and a "clock frequency of the bus," and claims 18 and 24 require "the clock controller configured to output a clock frequency of a high-speed clock to control the variable clock frequency of the bus and to control a clock frequency of a second master device coupled to the bus." '759 Patent at 8:63–64, 9:15–18, 9:26–30, 10:21–24.

The Court looks first to VLSI's doctrine of equivalents theory and the evidence it used to support its infringement claim. Dr. Conte testified that Intel's products include a PCU and clock circuit that has instructions to "provide the clock frequency of the high-speed clock as an output to control a clock frequency of a second master device" 2/23 Sealed Trial Tr. 44:9-46:25, 47:17-50:17. That constitutes the programmable clock controller. *Id.* Dr. Conte also testified that the programmable clock controller includes instructions to "provide the clock frequency of the high-speed clock as an output to control the variable clock frequency of the bus." *Id.* at 50:18-52:20. VLSI contends this is substantial evidence to support its theory that Intel's products meet the "provide . . . as an output to control" limitations. ECF No. 603 at 13.

Intel alleges that what VLSI identified as the "second master device" in the accused products is [redacted] ECF No. 591 at 12. Because [redacted] control the clock frequency of the cores and the clock frequency of the bus, Intel argues that

VLSI's infringement theory is contrary to the plain meaning of the claims, which stipulates that the same clock frequency must be "output to control" both the second master device and the bus. *Id.* at 13. According to Intel, [redacted] is not output to either the second master device or the bus—it is output to the [redacted] respectively—and [redacted] control the second master device and the bus. *Id.* Therefore, Intel concludes that no reasonable jury could find that the separate and independent control structure of Intel's products meets these claim limitations. *Id.*

VLSI responds that Intel's non-infringement theories ignore the claim language and the law. ECF No. 603 at 14. First, the claims do not require controlled clocks to have the same frequency and allow for different frequencies. *Id.* Second, Intel says "the same clock frequency must be 'output to control' both the second master device and the bus." ECF No. 591 at 13. Dr. Conte confirmed that the accused products meet this limitation when he explained that the same [redacted] is provided "as an output to control" both the "clock frequency of a second master device" and the "variable clock frequency of the bus." ECF No. 603 at 14. Third, the claims do not prohibit the use of intermediate components in effectuating that control, rendering Intel's non-infringement arguments based on the [redacted] and [redacted] contrary to law. *Id.* at 15. The claims use the transitional term "comprising," which "is inclusive or open-ended and does not exclude additional, unrecited elements." *CollegeNet*, 418 F.3d at 1235. As Dr. Conte confirmed, "a system comprising" in the claims means that "as long as all of the elements in the claim are present, the fact that one is adding additional features or elements would not change the question of whether a product infringes." ECF No. 603 at 15.

This Court agrees that VLSI presented substantial evidence supporting the jury's infringement finding for the "provide . . . as an output to control" limitation. Intel argues that

different clock frequencies separately output by the [redacted] and [redacted] to a second master device and the bus do not satisfy the claim's plain meaning, yet in doing so Intel draws a distinction without a difference.

As VLSI points out, Intel's accused products include a PCU and clock circuit with instructions to "provide the clock frequency of the high-speed clock as an output to control a clock frequency of a second master device" and "the variable clock frequency of the bus." ECF No. 603 at 13. Two critical distinctions between the accused products and the claim language, according to Intel, are that the accused products leverage intermediate hardware—that is, the [redacted] and [redacted] instead of a PCU and clock circuit directly—to provide an output signal, and that the signals are transmitted at different frequencies. ECF No. 591 at 12. But the claims do not require that the high-speed clock transmit its output directly to the second master device or the bus. ECF No. 603 at 14. Instead, they recite a high-speed clock that produces an output *to control* the second master device or bus. *Id.* The claim's plain language does not limit "control" to direct control as Intel argues and, therefore, covers the [redacted] and [redacted] as a means for effectuating that control, especially when considering the claim's open-ended transitional term, "comprising." Further, the claims do not require the controlled clocks to have the same frequency, and if they did, expert testimony confirms that [redacted] of the same frequency to both the "clock frequency of a second master device" and the "variable clock frequency of the bus." *Id.* at 13.

Ultimately, Intel fails to meet its burden for JMOL. Even if this Court accepts Intel's arguments, they fail to prove that reasonable minds could *only* conclude that judgment of no infringement is proper. At best, Intel presents a legitimate factual dispute and critiques the logical inferences underlying the jury's conclusion. Yet JMOL is only proper when the evidence presented shows the jury would not have been at liberty to disbelieve and pointing out legitimate factual

disputes over which reasonable minds could differ fails to meet this bar. The jury relied on more than a scintilla of evidence when it weighed both parties' expert opinions, including the factual disputes embedded therein, and rendered its verdict. Therefore, this Court declines to grant JMOL of no infringement on this ground.

C. Intel's Motion for JMOL on Claims Not Argued at Trial Is Improper.

VLSI represented that it was no longer asserting indirect infringement and claimed that it reserved the right to assert those claims later. ECF No. 591 at 13. But VLSI did not dismiss its inducement or contributory infringement claims, and Intel's declaratory judgment counterclaims on both issues are still live. *Id.* Thus, Intel argues that this Court should enter judgment of no induced and no contributory infringement because VLSI did not offer any evidence at trial on either issue. *Id.* However, Federal Rule of Civil Procedure 50 states that relief in this context is appropriate only "if a party has been fully heard on an issue during a jury trial." *Rembrandt Wireless Techs., LP v. Samsung Elecs.*, 2016 WL 633909, at *5 (E.D. Tex. Feb. 17, 2016). ECF No. 603 at 15. Here, the jury could not have fully heard contributory or indirect infringement issues because, by Intel's own admission, VLSI did not assert evidence supporting either claim at trial. Accordingly, this Court denies Intel's motion on this ground as improper.

II. Substantial Evidence Supports the Jury's Verdict on Invalidity for the '759 Patent.

A patent is invalid if before the patented invention, "the invention was made in this country by another inventor who had not abandoned, suppressed, or concealed it." 35 U.S.C. § 102(g) (pre-AIA). At trial, Intel asserted that claims 14, 17, 18, and 24 of the '759 patent were invalid. The jury found that Intel did not prove by clear and convincing evidence that those claims of the '759 patent were invalid. ECF No. 564. Intel argues, however, that this Court should enter JMOL of invalidity because a reasonable jury "could only conclude" that the Yonah processor anticipates

each asserted claim. ECF No. 591 at 14. According to Intel, VLSI based its contrary assertions solely on its argument that Yonah did not have a hardware-based "programmable clock controller," but the claim language and specification foreclose VLSI's argument. *Id.*

VLSI argues there was substantial evidence for a reasonable jury to conclude that Yonah did not anticipate the '759 Patent. VLSI alleges that Intel provided bare assertions that Yonah purportedly had a "programmable clock controller" while failing to identify what in Yonah met these limitations. ECF No. 603 at 16. VLSI claims that Intel's witnesses failed to explain how any alleged "programmable clock controller" in Yonah meets the limitations of "having an embedded computer program therein" or being "coupled to the arbiter and coupled to the first master device." *Id.* at 17. VLSI further contends that Dr. Conte provided the jury with even more reason to reject Intel's flawed theory in rebuttal. *Id.* According to Dr. Conte, "Yonah is the old approach" to speed changes, whereas the '759 patent and Intel's infringing processors use "the new approach." *Id.* In the '759 patent's new approach, speed changes are controlled by a "computer-in-a-computer," *i.e.*, a "programmable clock controller with an embedded computer program." *Id.* By contrast, the operating system in Yonah made speed control decisions. *Id.* Yonah did not include a "PCU," nor any other "programmable clock controller" with "an embedded computer program" as required by the '759 patent claims. *Id.*

After losing at trial, Intel argued that "the claim language and specification make clear that a hardware-based controller is not required and that software may be used." *Id.* at 18. VLSI argues that Intel ultimately seeks a new claim construction, but Intel waived that right by failing to request a one before trial. *Id.* Notwithstanding Intel's waiver, VLSI alleges that Intel's new argument contradicts the plain claim language. *Id.* Claim 14 recites a system with hardware components, such as the programmable clock controller with an embedded computer program therein. *See* PTX-

5 ("A *system comprising*: a *bus* …; a *first master device coupled to* the bus …; and a *programmable clock controller* having an *embedded* computer program *therein*...."). Claim 18 similarly recites a system with hardware components that are "coupled to" each other. *See* PTX-5 ("A *system comprising*: a *bus* …; a *first master device coupled to* the bus; an *arbiter coupled to* the bus and *coupled to* the first master device …; and a *clock controller coupled to* the arbiter and *coupled to* the first master device …."). Contrary to Intel's assertion, the claims thus do include requirements for a hardware-based programmable clock controller. Even if Intel had presented its new theory, VLSI suggests that a reasonable jury could reach different conclusions as to whether the "operating system [being] executed in the cores of Yonah" is a "programmable clock controller having an embedded computer program therein," making JMOL improper. ECF No. 603 at 19.

This Court agrees that substantial evidence supported the jury's invalidity verdict for two reasons. First, Intel could not affirmatively show that Yonah anticipated each claim of the '759 patent, much less by clear and convincing evidence. Second, VLSI sufficiently distinguished the '759 patent from Yonah using expert testimony.

Although Intel contends that the operating system in Yonah's anticipates the "programmable clock controller" with "an embedded computer program" disclosed by the '759 patent claims, it failed to identify what they were referring to specifically. ECF No. 603 at 16. Further, Intel could not clearly articulate what in Yonah anticipated the '759 patent's limitations or how Yonah allegedly met those limitations. *Id.* Instead, Intel resorts to criticizing VLSI's distinctions between Yonah and the '759 patent. But a party cannot meet an affirmative burden of proof—here, clear and convincing evidence—by pointing to deficiencies in the opposing party's validity arguments. Indeed, Intel's generic allegations dismissing VLSI's expert testimony as "conclusory" are themselves conclusory and insufficient to meet their affirmative burden of proof.

By contrast, VLSI presented substantial evidence supporting the jury's verdict in two ways. First, VLSI pointed out deficiencies in Intel witness testimony, including the absence of any reasonable statement connecting Yonah's "programmable clock controller" and the limitations of "having an embedded computer program therein" or being "coupled to the arbiter and coupled to the first master device." ECF No. 603 at 16. Second, VLSI's distinction between Yonah as the old approach and the '759 patent as the new approach carries more weight than Intel acknowledges. Contrary to Intel's portrayal, Dr. Conte reasonably substantiated his testimony by pointing to specific differences between the two approaches—namely, the '759 patent's programmable clock controller with an "embedded computer program" as the mechanism for triggering speed changes, rather than Yonah's operating system. *Id.* at 17. Intel believes it made clear to the jury that Yonah disclosed a combination of hardware and software running on a chip, not the operating system, but that provides even more reason to preserve the jury's finding. Under Intel's theory, the jury would have clearly understood Intel's arguments when deciding against them, which increases the likelihood that they made an informed decision rather than a clearly unreasonable one warranting reversal.

"Courts grant JMOL for the party bearing the burden of proof only in extreme cases, when the party bearing the burden of proof has established its case by evidence that the jury would not be at liberty to disbelieve and the only reasonable conclusion is in its favor." *Mentor H/S, Inc. v. Medical Device Alliance, Inc.*, 244 F.3d 1365, 1375 (Fed. Cir. 2001). Here, both parties' experts provided plausible invalidity theories to the jury, which the jury was free to believe or discredit as it saw fit. Given the technical distinctions Dr. Conte drew between the '759 and the Yonah processor, this Court believes that the evidence did not weigh so heavily in Intel's favor that the jury "could have only" rendered the '759 patent invalid as Intel suggests. VLSI provided more

than a mere scintilla of legally sufficient evidence to give the jury the liberty to disbelieve either party and, therefore, adequately supported the jury's invalidity verdict.

III. Substantial Evidence Supported the Jury's Damages Award.

The jury awarded a lump sum of $1.5 billion for infringement of the '373 Patent and a lump sum of $675 million for infringement of the '759 Patent. ECF No. 564. Intel argues that it is entitled to JMOL of no damages. ECF No. 591 at 17. First, Intel alleges that no reasonable jury could value the asserted patents at $2.175 billion considering the asserted patents' sales price, the lack of a formal valuation of the asserted patents, and comparable agreements for lower amounts. *Id.* Second, Intel asserts that the jury's damages award is not supported by legally sufficient evidence because it is based on noncomparable settlement agreements. *Id.*at 17–18. Under Federal Circuit precedent, those noncomparable agreements cannot support the jury's damages award. See *Lucent Techs., Inc. v. Gateway, Inc.*, 580 F.3d 1301, 1332, 1340 (Fed. Cir. 2009) (reversing denial of JMOL in part because damages expert relied on noncomparable licenses). Third, Intel argues that the jury's award is not supported by Dr. Sullivan's opinions. *Id.* at 18–19. Accordingly, Intel requests that this Court enter JMOL of no damages. *Id.*

VLSI responds that it presented substantial evidence supporting the damages award. First, VLSI argues Intel's patent valuation arguments rely on evidence favorable to the moving party that the jury is not required to believe. ECF No. 603 at 19. Second, VLSI alleges that there is no support for Intel's speculation that the jury based its damages numbers on noncomparable agreements. *Id.* at 20. According to VLSI, Intel "does not really know" if the jury based its award on any agreement, and a source matching an awarded number does not somehow "put the number . . . off limits to the jury." *Spectralytics, Inc. v. Cordis Corp.*, 649 F.3d 1336, 1346-47 (Fed. Cir. 2011). *Id.* Third, VLSI claims that Intel rehashes arguments previously rejected by this Court in

Daubert motions in questioning the Dr. Sullivan's reliability. *Id.* Consequently, VLSI requests that this Court deny Intel's motion for JMOL of no damages. *Id.*

This Court agrees with VLSI that the jury's damages award was supported by sufficient evidence. First, Intel alleges that the jury's $2.175 billion dollar verdict contravenes "overwhelming evidence" that the asserted patents are lower in value. But the jury considered evidence presented by both parties. This included Intel's "overwhelming evidence" of lower patent family prices, no prior ownership, and non-comparable agreements. VLSI also presented substantial evidence that Intel made over [redacted] from the nearly one billion products it sold with the infringing performance and power saving features of the patents. 2/24 Trial Tr. 593, 653-74; PDX7.74-76. The jury exercised reasonable discretion in crediting VLSI's damages evidence over Intel's damages evidence. Second, Intel contends that the jury improperly based its verdict on a non-comparable Nvidia agreement, and that Dr. Sullivan admitted as much. *Id.* Intel refuted its own argument, however, when it admitted that it "does not really know" whether the jury based its figure on any agreement. ECF No. 603 at 20. Any argument that the verdict was based on a purportedly non-comparable agreement is entirely speculative. Third, Intel argues that VLSI's damages case was unreliable, in part, because VLSI rooted it in unreliable and speculative expert testimony. ECF No. 615 at 10. But this Court has already considered and rejected these arguments in Intel's prior *Daubert* motions and its Rule 59 Motion. By asking this Court to render JMOL with no additional compelling reasons, Intel seeks to deploy the same reliability arguments and obtain different results. And contrary to Intel's argument that the damages numbers were not put into the record, Dr. Sullivan explained Intel's revenues to the jury, and any omissions were because he refrained from disclosing Intel's confidential information. 2/24 Trial Tr. 651:23–658:2; PTX3903, PTX3904.

Ultimately, Intel questions the degree to which the evidence justified the jury's verdict, but that is not the relevant question. Rather than consider how well the totality of the evidence supported the jury's finding, this Court must limit itself to determining whether the jury based its verdict on legally sufficient evidence that amounts to more than a scintilla. Here, the jury satisfied that standard by relying on the damages expert's testimony that Intel made over [redacted] dollars by infringing VLSI's patents. Intel disagrees with the outcome but falls short of proving that a verdict of no damages is the only reasonable conclusion from the evidence. Therefore, the jury's finding stands.

IV. CONCLUSION

For the reasons above, the Court finds that VLSI produced sufficient evidence to support the jury's verdict in this case. The Court therefore **DENIES** Intel's Motion for Judgment as a Matter of Law (ECF No. 591).

SIGNED this 18th day of March, 2022.

ALAN D ALBRIGHT
UNITED STATES DISTRICT JUDGE