IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF VIRGINIA
Richmond Division

SAMSUNG ELECTRONICS CO., LTD,
et al,

Plaintiffs,

v. Civil Case No. 3:14-cv-757

NVIDIA CORPORATION,
et al,

Defendants.

MEMORANDUM OPINION

This matter is before the Court for claim construction of U.S. Patent Nos. 5,860,158 (the "'158 Patent"), 6,262,938 (the "'938 Patent"), 6,287,902 (the "'902 Patent"), 6,819,602 (the "'602 Patent"), 8,252,675 (the "'675 Patent"), and 6,804,724 (the "'724 Patent'").

BACKGROUND

The Plaintiffs, Samsung Electronics Co., LTD and Samsung Electronics America ("Samsung") assert claims for infringement of the '158 Patent, the '938 Patent, the '902 Patent, the '602 Patent, the '675 Patent, and the '724 Patent (collectively the "Patents-in-Suit") against the Defendants, NVIDIA Corporation ("NVIDIA"), Old Micro Inc. ("Old Micro"), and Velocity Holdings LLC

("Velocity") (collectively, "Defendants"). The Patents-in-Suit relate to a method of building computer chips, systems which control a computer's operations, and a display adaptor linking a computer with an analog display. The parties have offered thirteen claims and one preamble for construction.

DISCUSSION

I. Legal Standard

The purpose of claim construction is to "determin[e] the meaning and scope of the patent claims asserted to be infringed." Markman v. Westview Instruments, Inc., 52 F.3d 967, 976 (Fed. Cir. 1995) (en banc), *aff'd*, 517 U.S. 370 (1996). The construction of a claim is a question of law. Id.

A term should be construed by the Court whenever there is an actual, legitimate dispute as to the proper scope of the claims. O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co., 521 F.3d 1351, 1360 (Fed. Cir. 2008). However, "a district court is not obligated to construe terms with ordinary meanings, lest trial courts be inundated with requests to parse the meaning of every word in the asserted claims." Id.

Furthermore, some claim terms will be so simple that "the ordinary meaning of claim language as understood by a person of skill in the art may be readily apparent even to lay judges, and claim construction in such cases involves little more than the application

of the widely accepted meaning of commonly understood words." Phillips v. AWH Corp., 415 F.3d 1303, 1314 (Fed. Cir. 2005). And, "a sound claim construction need not always purge every shred of ambiguity. The resolution of some line-drawing problems -- especially easy ones . . . -- is properly left to the trier of fact." Acumed LLC v. Stryker Corp., 483 F.3d 800, 806 (Fed. Cir. 2007). As recognized in O2 Micro, "district courts are not (and should not be) required to construe *every* limitation present in a patent's asserted claims . . . . Claim construction 'is not an obligatory exercise in redundancy.'" 521 F.3d at 1362 (quoting U.S. Surgical Corp. v. Ethicon, Inc., 103 F.3d 1554, 1568 (Fed. Cir. 1997)).

"Claim terms are generally given their plain and ordinary meanings to one of skill in the art when read in the context of the specification and prosecution history." Hill-Rom Servs, Inc. v. Stryker Corp, 755 F.3d 1367, 1371 (Fed. Cir. 2014). "There are only two exceptions to this general rule: 1) when a patentee sets out a definition and acts as his own lexicographer, or 2) when the patentee disavows the full scope of the claim term either in the specification or during prosecution." Thorner v. Sony Computer Entm't Am LLC, 669 F.3d 1362, 1365 (Fed. Cir. 2012). "[I]n interpreting an asserted claim, the court should look first to the intrinsic evidence of record, *i.e.*, the patent itself, including the claims, the specification, and, if in evidence, the prosecution history...Such

intrinsic evidence is the most significant source of the legally operative meaning of disputed claim language." Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576, 1582 (Fed. Cir. 1996). Of these sources, the words of the claim should be the Court's controlling focus. See Phillips, 415 F.3d at 1314; see also Digital Biometrics, Inc. v. Identix, Inc., 149 F.3d 1335, 1344 (Fed. Cir. 1998).

"Where the intrinsic record is ambiguous, and when necessary, [the Court may] rely on extrinsic evidence, which consists of all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises." Power Integrations, Inc. v. Fairchild Semiconductor, Intern., Inc., 711 F.3d 1348, 1360 (Fed. Cir. 2013). Extrinsic evidence, however, may not be used to contract or expand the claim language or the meanings established in the specification. Phillips, 415 F.3d at 1318-19; Vitronics, 90 F.3d at 1584. As explained in Nystrom v. Trex Co.,

> [I]n the absence of something in the written description and/or prosecution history to provide explicit or implicit notice to the public -- i.e., those of ordinary skill in the art -- that the inventor intended a disputed term to cover more than the ordinary and customary meaning revealed by the context of the intrinsic record, it is improper to read the term to encompass a broader definition simply because it may be found in a dictionary, treatise, or other extrinsic source.

424 F.3d 1136, 1145 (Fed. Cir. 2005).

II. Claim Construction

The terms tendered for construction are:

(1) "Depositing a second metal gate electrode layer onto inner sidewalls of the spacers and onto an upper surface of the patterned first metal gate electrode layer," which appears in the '675 patent;

(2) "Depositing a third metal gate electrode layer onto the second metal gate electrode layer," which appears in the '675 patent;

(3) "A gate insulating layer," which appears in the '675 patent;

(4) "Insulating spacer along a sidewall of the [second] patterned conductive layer," which appears in the '902 patent;

(5) "An insulating layer," which appears in the '902 patent;

(6) "Forming a trench in said substrate, and wherein said field isolation layer fills said trench," which appears in the '902 patent;

(7) "Request ID [value]," which appears in the '158 patent;

(8) "Controlling propagation delay time," which appears in the '602 patent;

(9) "Reference voltage," which appears in the '602 patent;

(10) "Determined/Determining," which appears in the '938 patent;

(11) "Shift register for delaying," which appears in the '938 patent;

(12) "Sending parallel digital video data," which appears in the '724 patent;

(13) "Means for generating a cable sensing signal to be sent to said first external video port over the digital cable, thereby informing the video controller of the digital cable connection state of said first external port," which appears in the '724 patent.

Additionally, the parties disagree as to whether the preamble of Claim 19 of the '938 Patent is limiting.

a) '675 Patent

Samsung asserts claims 12, 13, and 14 against Defendants in its Second Amended Complaint. Docket No. 81.

1. "Depositing a second metal gate electrode layer onto inner sidewalls of the spacers and onto an upper surface of the patterned first metal gate electrode layer"

The Defendants' proposed construction is "applying, using conformal (i.e. U-shaped) deposition, one metal gate electrode layer to the inner sidewalls of the spacers and to the upper surface of the patterned first metal gate electrode layer." Samsung's proposed construction is "creating a structure comprising one or more metal sublayers each formed by a deposition process onto inner sidewalls of the spacers and onto an upper surface of the patterned first metal gate electrode layer." The parties' dispute focuses on the whether the second metal gate electrode layer can have more than one layer and whether it must be formed using conformal deposition.

a) Words of the Claim

The term "depositing a second metal gate electrode layer onto inner sidewalls of the spacers and onto an upper surface of the patterned first metal gate electrode layer" appears in claim 6 in the '675 Patent. The language of Claim 6 of the '675 patent describes the following claim:

> A method of forming an integrated circuit device, comprising:
>
> ...
>
> depositing a second metal gate electrode layer onto inner sidewalls of the spacers and onto an upper surface of the patterned first metal date electrode layer

'675 Patent at 11:39-40, 58-60.

b) Specification and Prosecution History

The '675 Patent specification and figures consistently refer to and show the "second metal gate electrode layer" as a single layer. See, e.g. '675 Patent at Fig. 14, 5:28, 5:37[1]. However, the specification also states that the second metal gate electrode layer "may comprise a titanium nitride layer that is formed by a chemical vapor deposition (CVD) or an atomic layer deposition (ALD)" and that it "may include titanium nitride." Id. at 5:5-8, 2:2-3. The second metal gate electrode layer is also described as "'U' shaped" in the specification. Id. at 5:42-44.

Defendants argue that the prosecution history of the '675 patent support a finding that Samsung has disclaimed the use of multiple layers for the second metal gate electrode layer. In a response to the patent examiner's rejection, the '675 applicant attempted to distinguish his invention from the prior art by stating that the prior art lacked a "planar metal buffer gate electrode" and did not disclose

[1] The second metal gate electrode layer is referred to as the "first metal layer" in the '675 specification.

"patterning of a first metal gate electrode layer in advance of forming electrically insulating spacers and in advance of removing a dummy gate electrode layer." Docket No. 183-1 at 8. Rather, the prior art "merely illustrate[d] conformal deposition of multiple metal layers in sequence into pre-formed recesses in order to define composite metal gate electrodes." Id. The applicant then went on to state that the prior art was "prone to void formation when used to fabricate relatively narrow gate electrodes associated with highly integrated transistors" and that the "void formation may result from a premature closure of the recess during each conformal metal deposition step." Id. at 8-9.

c) Extrinsic Evidence

The parties do not cite to any extrinsic evidence.

d) Correct Construction

It is unnecessary to resolve Defendants' argument that the patent applicant disclaimed the use of multiple layers during the course of patent prosecution. The claim language plainly states that the second metal gate electrode layer must be deposited "onto an upper surface" of the first metal gate electrode layer. '675 Patent at 11: 58-60. Only one layer can be deposited onto the lower layer's surface. Thus, in order to comply with the claim's plain language, the second metal gate electrode layer can only consist of one layer.

Further, the Defendants have failed to support their argument that the deposition of the second metal gate electrode layer must be done conformally. That language is not found in the intrinsic evidence, and the Defendants have not adequately supported their argument that the claim's "U-shaped" language means "conformal."

Thus, the proper construction of the term "second metal gate electrode layer" is its plain and ordinary meaning. The claim language will be used.

2. "Depositing a third metal gate electrode layer onto the second metal gate electrode layer"

The Defendants' proposed construction is "applying, without using conformal deposition, a metal gate electrode layer to the one conformal metal gate electrode layer." Samsung's proposed construction is "creating a structure comprising one or more metal sublayers each formed by a deposition process onto the second metal gate electrode layer." The parties' dispute focuses on the whether the third metal gate electrode layer can have more than one layer and whether the manner in which it is formed must be non-conformal.

a) Words of the Claim

Claim 6 contains the language to be constructed. The language of Claim 6 of the '675 patent contains the following language:

> A method of forming an integrated circuit device, comprising:
>
> ...

> Depositing a third metal gate electrode layer onto the second metal gate electrode layer to thereby fill a space between the inner sidewalls of the spacers, said second and third metal gate electrode layers comprising different materials.

'675 Patent at 11:39-40; 11:61-12:3.

b) Specification and Prosecution History

The '675 Patent specification and the figures therein consistently refer to and show the "third metal gate electrode layer"[2] as a single layer. See, e.g. '675 Patent at Fig. 17, 6:4, 6:12. However, the '675 Patent specification states that the third metal gate electrode layer "may comprise at least one of aluminum, tungsten, titanium, and tantalum that is formed by a method such as PVD or CVD." '675 Patent at 5:66-6:1. Further it states that the third metal gate electrode layer "may comprise at least one of aluminum, tungsten, and titanium that are formed by PVD or CVD." Id. at 9:19-24. The CVD deposition process is expressly contemplated for both the second and third metal gate electrode layers. Id. at 9:19-24, 5:5-8.

The Defendants point again to the prosecution history and argue that the deposition must be "non-conformal" because the patent applicant made it clear that he was not using multiple conformal layers which were prone to "void formation."

[2] The "third metal gate electrode layer" is called the "second metal layer" in the specification. Docket No. 181 at 9.

c) Extrinsic Evidence

At oral argument, Samsung cited to the Thin Film Dictionary to show that "conformal" means a deposition wherein the "thickness remains the same regardless of the underlying geometrical features."

d) Correct Construction

Unlike the language requiring that the second metal gate electrode layer be "deposited onto the surface" of the underlying layer, the '675 Patent states only that the third metal gate electrode layer be "deposit[ed]...onto" the underlying layer. This less-restrictive language, in combination with the "comprising" language of the specification[3], supports the interpretation that the third metal gate electrode layer can consist of multiple sub-layers.

Additionally, the Defendants have failed to prove that the proper construction requires that the third metal gate electrode layer be applied "without using conformal deposition." The claim language does not support such a construction, as it does not limit the manner in which the third metal gate electrode layer can be applied.

Finally, the supposed disclaimer language discussed in the "second metal gate electrode" analysis does not support a finding

[3] It is well-established that the term "comprising" means "including, but not limited to." See CIAS v. Alliance Gaming Corp., 504 F.3d 1356, 1360 (Fed. Cir. 2007) ("'comprising' is well understood to mean 'including but not limited to.'").

of a disclaimer in the '975 patent. The Court requires a "clear and unambiguous disavowal of claim scope" in order to impart a limitation from the prosecution history into the language of the claim as a disclaimer. Storage Technology Corp. v. Cisco Systems, Inc., 329 F.3d 823, 833 (Fed. Cir. 2003). The correspondence provided here merely indicates that the patent applicant was distinguishing the prior art based on its absence of a "planar metal buffer gate electrode" and "patterning of a first metal gate electrode layer in advance of forming electrically insulating spacers and in advance of removing a dummy gate electrode." Docket No. 182-1 at 8. Although the applicant did note that the prior art's technique was "prone to void formation", such language does not constitute the type of "clear and unambiguous" language that the law requires for a disclaimer.

Thus, the proper construction is "depositing a third metal gate electrode layer comprised of one or more metal sublayers onto the second metal gate electrode layer."

2. "A gate insulating layer"

The Defendants propose that this term should be given its plain and ordinary meaning. Samsung's proposed construction is "a structure comprising one or more dielectric sublayers." Thus, the parties' dispute focuses on the whether the insulating layer can have more than one layer.

a) Words of the Claim

The term "gate insulating layer" appears in several claims in the '675 Patent. First, the language of Claim 1 of the '675 patent describes the following claim:

> A method of forming an insulated-gate transistor, comprising:
>
> ...
>
> forming a gate insulating layer on a substrate...

'675 Patent at 10:59-63.

Next, the language of Claim 3 of the '675 patent describes the following claim, which is dependent on Claim 1:

> The method of Claim 1, wherein the insulating-gate transistor is a PMOS transistor; and wherein the gate insulating layer comprises hafnium oxide.

'675 Patent at 11:31-33.

Next, Claim 6 of the '675 patent describes the following claim:

> A method of forming an integrated circuit device, comprising:
>
> ...
>
> forming a gate insulating layer on a substrate...

'675 Patent at 11:39-41.

Finally, Claim 15 of the '675 patent describes the following claim that is also dependent on Claim 6:

> The method of claim 6, wherein the gate insulating layer comprises a dielectric material selected from a group consisting of hafnium oxide and tantalum oxide.

'675 Patent at 12:69-61.

a) Specification and Prosecution History

The '675 Patent's specification states that the "gate insulating layer...may comprise at least one of hafnium oxide, tantalum oxide, silicon oxide and other high-k dielectric layer." '675 Patent at 6:13-5. However, the specification and figures do consistently refer to and show the "gate insulating layer" as a single layer. See, e.g. '675 Patent at Fig. 2-17 & 19-37, 3:43, 4:51.

b) Extrinsic Evidence

The parties do not present any extrinsic evidence.

c) Correct Construction

Both the claim language and the specification use the "comprising" language and thus support an interpretation that allows the gate insulating layer to be made up of multiple materials. See '675 Patent at 6:13-5, 11:31-33, and 12:69-61. While Defendants argue that this suggests that these multiple materials could be laid in one single layer in an alloy form, it is also possible that they could be laid sequentially, thus forming multiple layers in the gate insulating layer. Further, although Claim 6 does state that the gate insulating layer is to be formed "on a substrate", such language does

not require that each part of the gate insulating layer must touch the substrate - a top layer can be "on" a bottom layer without coming into direct contact with the bottom layer. Thus, the correct construction of this term is "a gate comprising one or more insulating sublayers."

b) '902 Patent

Samsung alleges infringement of claims 1, 3, 4, 5, 6, 7, 9, 10, 15, and 16 in its Second Amended Complaint. Docket No. 81.

1. "Insulating spacer along a sidewall of the [second] patterned conductive layer"

The Defendants' proposed construction is "an insulting spacer, along a sidewall of the [second] patterned conductive layer, that prevents etch damage to the field isolation layer if the contact hole is misaligned." Samsung's proposed construction is "an insulating sidewall spacer adjacent to the [second] patterned conductive layer." The parties' dispute focuses on the whether the insulating spacer must prevent etch damage and whether the phrase "spacer along a sidewall" should be rewritten. At oral argument, Samsung agreed that the claim language "spacer along a sidewall" adequately described the patent and agreed to use the claim language instead of the "spacer adjacent" language proposed in their claim construction briefs. Docket No. 214 at 6:6-7:21. Thus, the only dispute to evaluate at this point is whether the sidewall spacer must prevent etch damage.

a) Words of the Claim

The term "insulating spacer along a sidewall of the [second patterned conductive layer" appears in several claims in the '902 Patent. The term at issue is found in Claims 1, 11, 12, 15, and 18. First, the language of Claim 1 of the '902 patent describes the following claim:

> A method for forming a contact hole for a microelectronic structure, said method comprising the steps of:
>
> ...
>
> forming an etch inhibiting layer of said field isolation layer adjacent said active region of said substrate, the active region including the first patterned conductive layer wherein said etch inhibiting layer comprises a second patterned conductive layer and an insulating spacer along a sidewall of the second patterned conductive layer, wherein the second pattern conductive layer does not extend over the active region of the substrate, and wherein the second patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon.

'902 Patent at 6:48-50, 57-67.

Claim 11, Claim 12, Claim 15, and Claim 18 of the '902 patent contain the following language:

> A method for forming a microelectronic structure, said method comprising the steps of:
>
> ...
>
> forming a second patterned layer on said field isolation layer adjacent said active region of

> said substrate, the active region including the first patterned layer wherein said second patterned layer comprises a patterned conductive layer and an insulating spacer along a sidewall of the patterned conductive layer, wherein the patterned conductive layer does not extend over the active region of the substrate, and wherein the patterned conductive layer is a dummy pattern electrically isolated from the substrate and circuits thereon.[4]

'902 Patent at 7:40-41, 49-58; 8:1-2, 9-18; 8:33-34, 42-51; 8:66-67, 9:7-16.

b) Specification and Prosecution History

The specification of the '902 Patent describes the function of the claim. Specifically, it states that "if the contact hole extends beyond the active region of the substrate encroaching into the field region a second patterned conductive layer...reduces the likelihood that a well will be formed in the field isolation layer...In particular, the second patterned conductive lawyer...can act as an etch stop if needed when etching the insulating layer." Id. at 4:43-49. Additionally, the specification states that "the second patterned conductive layer and associated spacers protect the field isolation layer from the etch used to form the contact hole. Accordingly, even with a misalignment of the contact hole mask over the field region and over etching to insure exposure of the active region, the field isolation layer is not damaged." Id. at 6:8-13.

[4] These claims are identical to Claim 1 except for that the word "second" has been removed from "insulating spacer along a sidewall of the second patterned conductive layer.

The Defendants argue that Samsung's correspondence with the patent examiner during prosecution supports the proposed functional limitation. During prosecution of the '902 Patent, the patent examiner rejected the patent applicant's application as obvious in light of the prior art. Docket No. 183-2 at 6. The prior art - referred to as the Michihiro patent— had disclosed the use of dummy gates to prevent damage to the field isolation layer, but had not incorporated the use of sidewall spacers to assist in that process. Id. at 6-7. The patent examiner had thought that it was obvious to combine the dummy gates of the Michihiro patent with sidewall spacers found in the Chen patent, and thus denied Samsung's application.

The patent applicant responded to this denial and argued that its claims were patentable over the prior art. Docket No. 183-3. The patent applicant argued that it had no motivation to combine the Michihiro dummy gates with the Chen sidewall spacers. Id. at 18 ("[T]here is no clear and particular evidence of a motivation for modifying Michihiro in view of Chen.") Attempting to further distinguish its application from the Michihiro patent, the patent applicant stated that "there is simply no mention in Michihiro that it is desirable to prevent damage to the field oxide layer...There is nothing in Michihiro which suggests that there is need to include spacers that would prevent damage to the field oxide layer in the event the contact hole is misaligned." Id. a 19.

The patent examiner responded and allowed the patent applicant's claims. He stated in his "reasons for allowance" that "the prior art of record fails to disclose all the process limitations recited in the base claims, including a combination of a step of forming a dummy patterns as an etch inhibiting layer on a field isolation layer and a step of forming along the sidewalls of a dummy patterns the spacers that will prevent damage to the field oxide layer in the event the contact hole is misaligned." Docket No. 183-4 at 5. According to Defendants, this exchange supports a finding of a disclaimer of sidewall spacers which do not prevent etch damage by Samsung.

c) Extrinsic Evidence

The parties present no extrinsic evidence.

d) Correct Construction

The Court requires a "clear and unambiguous disavowal of claim scope" in order to impart a limitation from the prosecution history into the language of the claim as a disclaimer. Storage Technology Corp. v. Cisco Systems, Inc., 329 F.3d 823, 833 (Fed. Cir. 2003). The Defendants have failed to demonstrate that the exchange between the '902 patent applicant and the patent examiner constituted such a "clear and unambiguous disavowal" of sidewall spacers which did not prevent damage to the field isolation layer. There is nothing about the above exchange that supports a finding that the patent

applicant was voluntarily limiting the scope of his patent. Rather, he was attempting to illustrate to the patent examiner that his invention was not obvious in light of the Michihiro patent because the Michihiro patent did not contain any sidewall spacers. Thus, the correct construction is to retain the claim language of "insulating spacer along a sidewall."

2. "An insulating layer"

The Defendants propose that the term be given its plain and ordinary meaning. Samsung's proposed construction is "a structure comprising one or more electrically insulating layers." Thus, the parties' dispute focuses on the whether the insulating layer can have more than one layer.

a) Words of the Claim

The term "an insulating layer" appears in several claims in the '902 Patent. The term at issue is found in Claims 1, 2, 11, 12, 15, and 18. First, the language of Claim 1 of the '902 patent describes the following claim:

> A method for forming a contact hole for a microelectronic structure, said method comprising the steps of:
>
> ...
>
> forming an insulating layer on said substrate, said field isolation layer, said first patterned conductive layer, and said etch inhibiting layer; and

> forming a contact hole in said insulating layer exposing a portion of said active region between said etch inhibiting layer and said first patterned conductive layer

'902 Patent at 6:48-50, 7:1-6.

Next, the language of Claim 2, which is dependent on Claim 1 of the '902 Patent states:

> A method according to claim 1 wherein said insulting layer comprises nitride.

Id. at 7:7-8.

Additionally, the language of Claim 11, Claim 12, Claim 15, and Claim 18 state:

> A method for forming a microelectronic structure, said method comprising the steps of:
>
> ...
>
> Forming an insulating layer cover said substrate, said field isolation layer, and said first and second patterned layers; and
>
> Forming a contact hole in said insulating layer wherein said contact hole exposes a portion of said action region between said first and second patterned layers.

Id. at 7:40-41, 58-64; 8:1-2, 19-25; 8:33-34, 52-57; 8:66-67, 10:3-9.

b) Specification and Prosecution History

The '902 Patent's specification and claims serially describe and depict the insulating layer as just that – a singular layer. See '902 Patent, Fig. 4-8, 4:32, 4:37, 5:60, 5:63 (using the term

"insulating layer"). However, prior art cited by the patent applicant during prosecution describes an insulating layer that includes multiple sublayers. See U.S. Patent 5,659,202 at 4:10-14 ("An interlayer insulation film...may be, for example formed of a single-layer film or lamination of [multiple materials]); U.S. Patent 5,293,503 at 3:15-19 ("...in interlayer insulating film...consisting of a first silicon oxide film...and a second silicon oxide film...").

c) Extrinsic Evidence

The parties cite to no extrinsic evidence.

d) Correct Construction

As Samsung pointed out, Claim 1 describes the method claimed, which includes the use of "an insulating layer." Dependent Claim 2, which describes and must be narrower than Claim 1, states that the insulating layer comprises nitride. It is well-established, as discussed above, that the term "comprising" is open-ended and permits for additional elements. Claim 2, therefore, allows for multiple materials to be used in forming the insulating layer. While these materials could be combined to form an alloy, they also could be laid down separately and thus form more than one insulating layer. Thus, multiple layers are cognizable within the language of the patent, and the term is correctly defined as a "structure comprising one or more electrical insulating layers."

3. "Forming a trench in said substrate, and wherein said field isolation layer fills said trench"

The Defendants propose that the term be given its plain and ordinary meaning. Samsung's proposed construction is "etching a recess into said substrate and subsequently filling said recess with a field isolation layer." Samsung proposes that a construction in order to make it clear that it does not claim the LOCOS method of forming a field isolation layer. At oral argument, the parties agreed that it was "clear that [Samsung did not] claim the LOCOS method" and instead claimed "the trench method." Docket No. 214 at 54:3-55:21. Thus, Samsung is no longer seeking its proposed construction and the parties agreed that the claim would be left in its original format and would be given its plain meaning.

c) '158 Patent

Samsung alleges infringement of claims 1, 15, 17, 18, 21, and 22 in its Second Amended Complaint. Docket No. 81.

1. "Request ID [value]"

The Defendants' proposed construction is "a numerical value assigned by the cache controller." Samsung's proposed construction is "an identifier assigned to each cache request that distinguishes it from other cache requests." The parties dispute whether the request ID values must be assigned by the cache controller and whether the request ID value has to be assigned to each and every request.

a) Words of the Claim

The term "request ID value/ request ID" appears in several claims in the '158 Patent and is included in claims 1, 15, and 18. First, the language of Claim 1 of the '158 patent describes the following claim:

> A method for controlling a cache, the cache being coupled to a device, the method comprising:
>
> receiving by a cache controller a first cache request from the device;
>
> providing by the cache controller a first request ID value corresponding to the first cache request to the device after receiving the first cache request;
>
> initiating processing of the first cache request after receiving the first cache request;
>
> receiving by the cache controller a second cache request from the device after receiving the first cache request;
>
> providing by the cache controller a second request ID value corresponding to the second cache request to the device after receiving the second cache request...

'158 Patent at 37:1-16.

The language of Claim 15 of the '158 patent describes the following claim:

> A method for controlling a cache, the cache being coupled to at least one device, the method comprising:

> receiving by a cache controller a first cache request from a first device of the at least one device [sic];
>
> providing by the cache controller a first request ID value corresponding to the first cache request to the first device after receiving the first cache request;
>
> initiating processing of the first cache request after receiving the first cache request;
>
> receiving by the cache controller a second cache request from a second device of the at least one device [sic] after receiving the first cache request;
>
> providing by the cache controller a second request ID value corresponding to the second cache request to the second device after receiving the second cache request...

Id. at 39:56-40:3.

The language of Claim 18 of the '158 patent describes the following claim:

> A method of controlling a cache, the cache coupled to a cache controller and a cache accessing device, the method comprising:
>
> a first step of receiving a first cache request from the cache accessing device by the cache controller;
>
> a second step of providing a first request ID to the cache accessing device by the cache controller after the first step;
>
> a third step of storing the first request ID by the cache accessing device after the second step;

> a fourth step of receiving a second cache request from the cache accessing device by the cache controller after the first step;
>
> a fifth step of providing a second request ID, to the cache accessing device by the cache controller after the fourth step;
>
> a sixth step of storing the second request ID by the cache accessing device after the fifth step...

Id. at 40:26-43.

b) Specification and Prosecution History

The '158 Patent's preferred embodiment describes the process of generating a request ID as follows:

> Cache control unit will grant the request by driving a grant signal and assigning a request identification number to the granted request. In the preferred embodiment, a ten bit request ID is driven to the requester. If the upper 4 bits of the request ID match the unit ID of the requester, the request is granted. The requester should latch the lower 6 bits of the request ID since it is the transaction ID associated with the request. If a request is granted, the requester should drive address and other control information such as data type to [the] cache control unit.

Id. at 13:20-29. In an alternative embodiment, the specification states that the request ID can be formed "by a device identification code...and an address of the requested memory location." Id. at 8:38-40. Because "each unit has a distinct device ID...[the] cache system can prioritize the requests based on the device ID of the unit

making the request." Id. at 40-42. Then, when the data at the requested address becomes available, [the] cache system responds with the device ID, a transaction [ID]...the address, and the requested data." Id. at 42-45.

Additionally, the Summary of the Invention states that the novelty of the patent is that "it has been discovered that accesses to a cache by multiple devices may be managed by a cache control unit that includes transaction identification logic to identify cache accesses." Id. at 2:9-12.

c) Extrinsic Evidence

The parties cite no extrinsic evidence.

d) Correct Construction

The parties agreed at oral argument that every request ID must be a numerical value because computers communicate only in binary terms. Docket No. 215 at 140:24-25; 164:6-13.

The claim language of the '158 Patent supports a finding that the cache controller must assign the request ID because it states that the request IDs are "provid[ed] by the cache controller." Further, the '158 Patent's specification states that the "cache control unit will grant the request by...assigning a request identification number to the granted request." '158 Patent at 13:20-22.

Although Samsung argues that other text in the specification

supports a finding that the cache controller does not have to perform the assigning on its own, there is no support for that argument in the text. Samsung argues that the statement that the "request ID is driven to the requester" allows for an inference that something other than the cache controller is doing the driving. However, Samsung has overlooked the fact that the sentence immediately preceding that language states that the "cache control unit will grant the request by...assigning a request identification number."

Additionally, Samsung's argument that the Defendants' proposed construction would read out a preferred embodiment is incorrect. While the specification does state that the requesting device can supply the cache controller with its device ID and that said device ID can be combined with a cache controller-generated transaction ID to form the request ID, this language still contemplates that the cache controller will provide the final request ID to the requesting device.

Finally, the claim language contemplates only a first and second request ID. Samsung has provided inadequate support for the argument that such language supports an interpretation requiring that every request be assigned a request ID. Thus, the proper construction of "request ID" is "numerical value assigned by the cache controller."

d) '602 Patent

Samsung alleges infringement of claims 1, 3, 26, 27, 28, and 29 against Defendants in its Second Amended Complaint. Docket No. 81.

1. "Controlling propagation delay time"

The Defendants' proposed construction is "selectively delaying a signal as it passes through a circuit." Samsung proposes that the term be given its plain and ordinary meaning. The parties dispute whether all signals must be delayed.

a) Words of the Claim

The term "controlling propagation delay time" appears in claim 26. The language of Claim 26 of the '602 patent describes the following claim:

> A method of controlling propagation delay time of a semiconductor memory, comprising:
>
> receiving an inverse data strobe signal or a reference voltage, respectively, depending on a level of a control signal;
>
> receiving a data strobe signal; and
>
> amplifying and outputting at least two different differentially amplified data strobe signals.

'602 Patent, 18:38-15.

b) Specification and Prosecution History

Samsung argues that the '602 Patent specification contains an

embodiment that "includes a compensating circuit that consists of a dummy load that inserts a constant delay into the circuit." Docket No. 181 at 31 (citing '602 Patent at 3:61-64). This embodiment would delay all signals rather than selectively delay them. However, the Defendants urge that "every embodiment that controls delay time does so by selectively delaying one of the signals as it passes through a circuit." Docket No. 183 at 18 (citing '602 Patent at Figs. 7, 9, 11, 12).

Samsung specifically points to Figure 11 and argues that it proposes an embodiment that does not require the signals to be selectively delayed. Rather, "a gain of a first of the at least two differential amplifiers is substantially different from a gain of a second of the at least two differential amplifiers so that each of at least two differential output signals have substantially the same delay time." '602 Patent at 5:33-38.

The parties have agreed that the preamble to claim 26 - which reads "a method of controlling propagation delay time of a semiconductor memory" - is limiting. However, they disagree as to whether that control must happen within the semiconductor memory, or whether the control must only be exerted over the semiconductor memory. The specification contains at least one example in which a data strobe signal is "input into a semiconductor memory device and output from a semiconductor memory device as data." Docket No.

188 at 22. The specification states that "a DDR synchronous DRAM uses a data strobe signal when the DRAM receives data from a memory controller or sends data to the memory controller," thus teaching that at least some of the process could be performed outside the semiconductor memory. Id. at 1:38-45.

c) Extrinsic Evidence

Samsung cites to a scientific dictionary which defined "propagation delay" as "[t]he time from when the input logic level to a device is hanged until the resultant output change is produced by that device." Dictionary of Computer Science, Engineering, and Technology (2001).

The Defendants cite to two technical definitions of "propagation delay." Docket No. 183 at 19. The first defines "propagation delay" as "[t]he amount of time between when a signal is impressed on the input of a circuit and when it is received or detected at the output." IEEE 100: The Authoritative Dictionary of IEEE Standards and Terms (Seventh ed. 2000). The second defines "propagation delay" as "[t]he time requires for a signal to pass through a given complete operating circuit..." McGraw Hill Dictionary of Scientific and Technical Terms (Sixth ed. 2000).

d) Correct Construction

The parties agreed at oral argument that the term "controlling" could be readily understood by a jury without construction and that

the proper construction of the term "propagation delay time" was "time from input to output of a signal." Docket No. 214 at 203:21-204:11.

The Defendants have failed to prove that the '602 Patent requires that signals are selectively delayed as they pass through the circuit. Rather, the patent appears to contemplate and allow for delays of all signals that pass through the circuit. Additionally, while the parties have agreed that the preamble to claim 26 is limiting, that preamble does not establish the limitation that the Defendants urge. The preamble states only that the method must control "propagation delay time of a semiconductor memory" - there is no requirement that such control must happen within the semiconductor memory. Thus, the term is properly construed as "controlling the time from input to output of a signal of a semiconductor memory."

2. "Reference Voltage"

The Defendants' proposed construction is "constant, known voltage level for comparison." Samsung proposes that the term be given its plain and ordinary meaning. The parties dispute whether the voltage level can ever vary and whether it must be a known value.

a) Words of the Claim

The term "reference voltage" appears in several claims in the '602 Patent. The term "reference voltage" appears in claim 1, 3,

26, and 27. The language of Claim 1 of the '602 patent describes the following claim:

> A data strobe input buffer, comprising:
>
> a differential amplifier circuit including at least two switches for passing an inverse data strobe signal or a reference voltage, respectively, depending on a level of a control signal, and a differential amplifier for receiving a data strobe signal and either the inverse data strobe signal or the reference voltage and outputting a differentially amplified signal.

'602 Patent at 16:7-14.

The language of Claim 3 of the '602 patent describes the following claim:

> The data strobe input buffer of claim 1, wherein the data strobe input buffer is operable in both a single mode and a dual mode, wherein in said single mode, the reference voltage is applied to a first of the at least two switches and in said dual mode, the inverse data strobe signal is provided to a second of the at least two switches and the level of the control signal is a second logic state.

Id. at 16:19-26.

The language of Claim 26 of the '602 patent describes the following claim:

> A method of controlling propagation delay time of a semiconductor memory, comprising:
>
> receiving an inverse data strobe signal or a reference voltage, respectively, depending on a level of a control signal;

> receiving a data strobe signal; and
>
> amplifying and outputting at least two different differentially amplified data strobe signals.

Id. at 18:38-15.

Finally, the language of Claim 27 of the '602 patent describes the following claim:

> The method of claim 26, wherein in a single mode, the reference voltage is received and a level of the control signal is a first logic state and in a dual mode, the inverse data strobe signal is received and the level of the control signal is a second logic state.

Id. at 18:46-50.

b) Specification and Prosecution History

One patent cited by the examiner during the prosecution history of this patent, U.S. Patent No. 6,512,704, states that a reference voltage could have multiple values. Specifically, it states that "the first input of the first comparator...could be coupled with a 1.25 volt or a 1.5 volt reference." '704 Patent at 2:57-62.

Another patent cited during the course of the '602 prosecution, U.S. Patent 6,414,517 states that a "typical input buffer circuit...compares an input signal...to a predetermined reference voltage." '517 Patent at 1:21-23. Additionally, Figure 2 of the '602 Patent depicts the reference voltage as a constant, steady line.

c) Extrinsic Evidence

The term "reference voltage" is defined in an electrical

engineering dictionary as a "voltage level whose steady value serves as a basis for comparison or operation." The Wiley Electrical and Electronics Engineering Dictionary (2004). Both parties cite to this definition in their claim construction briefing. Docket No. 183 at 19; Docket No. 181 at 28.

d) Correct Construction

The parties have agreed that the reference voltage must remain constant while it is being used for comparison. Docket No. 214 at 176:19-177:6. Additionally, the parties both cite the definition provided by The Wiley Electrical Engineering Dictionary as an acceptable construction of the term. Thus, the Court will adopt the construction provided by both parties and the term will be construed as "a voltage level whose steady value serves as a basis for comparison."

e) '938 Patent

Samsung asserts claims 17, 18, 19, 21, 23, and 24 against Defendants in its Second Amended Complaint. Docket No. 81.

1. Preamble of Claim 19

The parties dispute whether the preamble of Claim 19 is limiting. Defendants propose that the preamble does limit the claim. Samsung proposes that it does not. A preamble limits a claim "if it recites an essential structure, or if it is necessary to give life, meaning, and vitality to the claim." Catalina Mktg. Int'l v.

Coolsavings.com, Inc., 289 F.3d 801, 808 (Fed. Cir. 2002) (citation omitted).

a) Words of the Claim

Claim 19 reads:

> A synchronous DRAM (SDRAM), comprising:
>
> a memory bank having a plurality of memory cells arranged in rows and columns; and
>
> a decoder for selecting one of the memory cells based on a column address and a row address,
>
> wherein RL_{min} is the minimum number of clock cycles of the clock signal required from the application of a row access command to the output of the data of the selected memory cell,
>
> wherein Cl_{min} is the minimum number of clock cycles of the clock signal required from the application of arrow access command to the output of the data of the selected memory cell,
>
> wherein RCL is the number of clock cycles of the clock signal from the application of a row access command to the application of a column access command with respect to the memory bank, and
>
> wherein a CAS latency, which is the number of clock cycles of the clock signal required from the application of the column access command to the output of data, is determined to be (RL_{min}-RCL) when RCL is less than (RL_{min} - Cl_{min}) and is determined to be Cl_{min} when RCL is not less than (RL_{min} - Cl_{min}).

'938 Patent at 16:9-33.

b) Specification and Prosecution History

Several parts of the '938 Patent discuss an SDRAM. For example,

the '938 Patent is titled "Synchronous DRAM having posted CAS latency and method for controlling CAS latency." '938 Patent at 1. The Abstract states that the invention is intended to "perform a posted CAS latency operation and a general CAS latency operation by the SDRAM." '938 Patent at Abstract. Additionally, the Summary of the Invention states that "[i]t is the object of the present invention to provide a synchronous DRAM (SDRAM) by which it is possible to perform a posted column access strobe (CAS) command." Id. at 2:2-4. The Specification states that,"[a]ccording to the SDRAM and the method for controlling the CAS latency of the present invention, a posted CAS latency operation...can be appropriately performed by the SDRAM." Id. at 6:1-4.

The '938 Patent contains several embodiments of the invention as well. For example, Figure 4 illustrates "the SDRAM in a posted CAS command mode" and is "a timing diagram of a posted CAS command in the main terminal of the SDRAM." Id. at 6:21-22; 9:60-61.

c) Extrinsic Evidence

The parties do not present any extrinsic evidence.

d) Correct Construction

The Defendants have failed to establish that the preamble to claim 19 is limiting. The preamble does not add structure or steps and the claim body describes a structurally complete invention, such that the deletion of the preamble phrase does not affect the structure

or steps of the claimed invention. Thus, the claim does not depend on the preamble for an antecedent basis and it is not essential to understanding the limitations or terms in the claim body. Thus, the preamble of claim 19 is construed as not limiting.

2. "Determined/Determining"

The Defendants' proposed construction is "comput[ed/ing] by the SDRAM." Samsung proposes that the term be given its plain and ordinary meaning. The parties dispute whether the SDRAM must perform the action and whether "computed" is equivalent to "determined."

a) Words of the Claim

The term "determined/determining" appears in several claims in the '938 Patent. The term "determined/determining" language appears in claims 18, 21, 23, and 24. The language of Claim 18 of the '938 patent describes the following claim:

> A synchronous DRAM (SDRAM) synchronized with a clock signal after predetermined column access strobe (CAS) latency has lapsed from a column access command, the SDRAM comprising:
>
> ...
>
> wherein the CAS latency is determined by the number of clock cycles of the clock signal from the application of a row access command to the application of a column access command with respect to the memory bank.

'938 Patent, 15:64-67, 16:5-8.

The language of Claim 21 of the '938 patent describes the

following claim:

> A synchronous DRAM (SDRAM) operating in synchronization with a clock signal, the SDRAM comprising:
>
> ...
>
> wherein a CAS latency, which is the number of clock cycles of the clock signal required from the application of the column access command to the output of data, is determined by the difference between RCL and SAE.

Id. at 16: 36-37, 61-64.

The language of Claim 23 of the '938 patent describes the following claim:

> A method of controlling CAS latency of an SDRAM, synchronized with a clock signal, that includes a memory bank having a plurality of memory cells arranged in rows and columns and outputs the data of a selected memory cell, the method comprising:
>
> ...
>
> Determining CAS latency, which is the number of clock cycles of the clock signal required from the application of the column access command to the output of the data to be (RLmin - RCL) when RCL is less than (RL_{min} - CL_{min}); and
>
> Determining the CAS latency to be CL_{min} when RCL is no less than (RL_{min} - CL_{min}).

Id. at 17: 5-9, 24-30.

The language of Claim 24 of the '938 patent describes the following claim:

> A method of controlling CAS latency of an SDRAM which includes a bank having a plurality of

> memory cells arranged in rows and columns that outputs the data of a selected memory cell in synchronization with the clock signal, the method comprising:
>
> ...
>
> Determining CAS latency, which is the number of clock cycles of the clock signal required from the application of the column access command to the output of the data, to be (RL_{min} – RCL) when RCL is less than SAE and the difference between RCL and SAE is not less than a predetermined number of reference clock cycles; and
>
> Determining the CAS latency to be Clmin when RCL is not less than SAE or the difference between RCL and SAE is less than the predetermined number of reference clock cycles...

Id. at 17:31-32, 18:1-2, 13-24.

b) Specification and Prosecution History

The '938 Patent specification does not speak directly to what must perform the "determining" function. Instead, it contains more generalized statements and preferred embodiments that say, for example, that, "when [A] is less than [C], [D] is determined to be [F]. When [A] is not less than [C], [D] is determined to be [E]." Id. at 10:10-15. Samsung argues that this embodiment "illustrates an example of 'determining' as a simple assignment when certain conditions are met...[and t]here is no computation of the value D." Docket No. 181 at 25. Further, it argues that this statement illustrates that the patent does not limit where the determination must take place.

During the course of patent prosecution, the patentee stated, when addressing claim 1, that he did "not intend to restrict how the first number of delay clock cycles [were] determined except to require that it be determined in response to the [difference] between [A and B]." Docket No. 181-11. He also stated that the "arguments similar to those...for claim 1 are applicable to claims 6, 7, 19, 21, and 22." Id.

However, the patentee defended the patentability of his invention during the course of prosecution, stating that "nothing in [the prior art] discloses or suggests measuring RCL...much less comparing [its] value to generate...a first number of delay clock cycles." Docket No. 183-20 at 10. He also clarified the process of his invention, stating that the "first number of delay clock cycles is determined in response to information on the difference between RCL and [RCL_{min}]. Id. at 4. The Defendants argue that this description requires that "the SDRAM perform mathematical operations." Docket No. 183 at 24.

c) Extrinsic Evidence

Defendants cite to several dictionaries which "equate 'compute' with 'determine.'" See, e.g. The American Heritage Dictionary of the English Language (3d ed. 1992) at 389 (defining "compute", in part, as "to determine by mathematics, especially by numerical methods... to determine by use of a computer"); Webster's New World

College Dictionary (4th ed. 1999) at 300 (defining "compute", in part, as "to determine (a number, amount, etc.) by arithmetic; calculate...to determine or calculate by using a computer.").

Samsung also cites to a dictionary definition which defines "determine", but does not reference computers or computations of any form. The American Heritage College Dictionary (1993) at 379.

d) Correct Construction

The Defendants have failed to prove that the determination described in the '938 Patent must take place in the SDRAM. There is no limitation in the language of the claims or in the specification that requires the determination to be made by the SDRAM. To the contrary, the patentee specifically stated that he did not intend to limit how the determination was made. Further, there is no evidence establishing that "determination" is synonymous and means "computation." Thus, the term will be correctly construed according to its plain and ordinary meaning.

3. "Shift register for delaying"

The Defendants' proposed construction is "a register that moves its contents to the left or right for delaying." Samsung's proposed construction is "a circuit including a register for delaying."

a) Words of the Claim

The term "shift register for delaying" appears in Claim 8 in the '938 Patent, on which claim 17 depends. Claim 8 states:

> A synchronous DRAM (SDRAM) operating in synchronization with a clock signal, the SDRAM comprising:
>
> ...
>
> A first shift register for delaying the column address by a first number of delay clock cycles between the column address input port and the column decoder...

'938 Patent, 14:22-23, 33-35.

b) Specification and Prosecution History

The '938 Patent's specification contains a preferred embodiment which states that the "first shift register may comprise a plurality of registers serially coupled to each other, for continuously transmitting the column address every clock signal, and a multiplexer for selectively providing one signal among the output signals of the registers to the column decoder in response to the difference between RCL and SAE." Id. at 3:30-36; see also Figure 1. Samsung argues that this embodiment "can perform one of many different operations" and is not restricted from moving its contents left or right. Docket No. 181 at 24. Specifically, Samsung argues that "the shift register may shift data (if the input signal containing the column address is directed to one or more of the three registers), or is may not (if the input signal is directed straight to the multiplexer.)" Docket No. 188 at 15. The Defendants respond that either of those options involve the "shift" of data, and thus their proposed definition does not read out a preferred embodiment. Docket No. 187

at 20-22.

The specification also describes the invention by stating that, "[i]n operation, the column address is transmitted to the next register every clock cycles of the clock signal." '938 Patent at 7:45-47.

c) Extrinsic Evidence

Samsung cites to the Microsoft Computer Dictionary, which defines a "register" as something which is "used as a holding area [for]...pieces of data or information...[such as] to hold the results of an addition operation or to hold the address of a particular location in the computer's memory." Microsoft Computer Dictionary, 334 (2d ed. 1994).

The Defendants cite to The Authoritative Dictionary of IEEE Standards Terms (2000), which defines a "shift register" as "(1) A register in which the stored data can be moved to the right or left. (2) A register in which the data bits can be shifted in one direction or both." Id. at 327.

d) Correct Construction

The Defendants have failed to produce any intrinsic evidence which requires that the shift register disclosed in the '938 Patent requires that its contents are moved to the left or to the right in every instance. On the contrary, Figure 1 discloses a scenario in which the data is not delayed or shifted. The Defendants admit as

much in their response brief when they state: "Samsung relies on the fact that [the Column Address] may be output to the column decoder without being shifted or delayed. It is true that shift register...has such capability." Docket No. 187 at 21. Thus, based on the language of the '938 Patent and the Defendants' admissions, the proper construction of the term is "a circuit including a register for delaying."

f) '724 Patent

Samsung alleges infringement of claims 6, 7, and 8 in its Second Amended Complaint. Docket No. 81.

1. "Sending parallel digital video data"

The Defendants' proposed construction is "simultaneously transmitting all bits of a given byte of the video data." Samsung proposes to give the term its plain and ordinary meaning.

a) Words of the Claim

The term "sending parallel digital video data" appears in several claims in the '724 Patent. The "sending parallel digital video data" language appears in claims 6 and 9. The language of Claim 6 of the '724 patent describes the following claim:

> A portable computer system, comprising:
>
> ...
>
> a digital transmitter sending parallel digital video data to said external digital monitor, said digital monitor comprises a means for generating a cable sensing signal to be sent to

> said first external video port over the digital cable, thereby informing the video controller of the digital cable connection state of said first external port, said system further comprising a monitor power sensor detecting a presence of power applied to the external digital monitor, whereby a display enable signal is generated in the video controller and is sent to the transmitter to enable the digital video signals to be sent to the external digital monitor when the presence of power applied to the external digital monitor is detected.

'724 Patent, 11:58, 11:66-12:12.

The language of Claim 9 of the '724 patent describes the following claim:

> A portable computer system, comprising:
>
> ...
>
> a digital transmitter sending parallel digital video data to said external digital monitor, said digital monitor, the video controller further generates analog video signals to be sent to a second external video port and then to an external analog monitor...

Id. at 12:26, 12:33-38..

b) Specification and Prosecution History

The specification describes one type of transmitter called a "TMDS" transmitter. '724 Patent at 6:14-19. These transmitters have three data channels and one clock signal, thus making only a three-bit parallel transmission possible. Id.; Docket No. 181-17 at 396. Because the Defendants' construction would require simultaneous transmission of eight bits (a "parallel transmission"),

Samsung argues that the Defendants' definition excludes the only type of transmission process the '724 Patent describes. Docket No. 181 at 32.

The '724 specification further states that the "transmitter...receives parallel digital video data" from the video controller and "encodes and serializes the parallel input data by the use of an internal PLL circuit. The serialized data is then transmitted to...the LCD monitor...over four low voltage differential channels." '724 Patent at 6:3-12.

c) Extrinsic Evidence

The Defendants cite to The IEEE Standard Dictionary of Electrical and Electronics Terms (6th ed.), which defines "parallel transmission" as "simultaneous transmission of the bits making up a character, either over separate channels or on different carrier frequencies on one channel" and "[i]n data communications, the simultaneous transmission of all bits making up a character or byte where each bit travels on a different path. Contrast: serial transmission."

d) Correct Construction

The parties are in agreement that the term "sending parallel digital video data" should be interpreted at "transmitting all bits of a given character of video data." Docket No. 214 at 273:23-25. The parties disagreed, however, as to whether that transmission had

to be simultaneous. If this Court interpreted the term as Defendants suggest, it would exclude, in effect, all embodiments contained in the Patent. To do that, there must be highly persuasive evidence, which was not presented here. See Vitronics, 90 F.3d at 1583 ("Indeed, if 'solder reflow temperature' were defined to mean liquidus temperature, a preferred (and indeed only) embodiments in the specification would not fall within the scope of the patent claim. Such an interpretation is rarely, if ever, correct and would require highly persuasive evidentiary support..."). As the Court construes the term, "parallel" is an adjective describing the digital video data and is not meant as a parallel transmission. Thus, the proper construction of the term presented is "transmitting all bits of a given character of the video data."

2. "Means for generating a cable sensing signal to be sent to said first external video port over the digital cable, thereby informing the video controller of the digital cable connection state of said first external port"

This term is a means-plus-function limitation.[5] Thus, to construe the term, "the court must determine the claimed function [and then] the court must identify the corresponding structure in the written description of the patent that performs the function." Noah Sys., Inc. v. Intuit Inc., 675 F.3d 1302, 1311 (Fed. Cir. 2012) (citation omitted). Both parties have proposed a function and a

5 Means-plus-function terms are governed by 35 U.S.C. §112(6).

structure for this term. The Defendants' proposed function construction is "generating a cable sensing signal to be sent to said first external video port over the digital cable, thereby informing the video controller of the digital cable connection state of said first external port." The Defendants propose the Monitor Cable Sensing Circuit 527, as described in Figure 14 and at 7:31-8:16, as the proper structure. Samsung's proposed function construction is "generating a cable sensing signal." Samsung proposes the DVCC and resistor R1, as depicted in Figure 14, as the proper structure.

a) Words of the Claim

The term "means for generating a cable sensing signal to be sent to said first external video port over the digital cable, thereby informing the video controller of the digital cable connection state of said first external port" appears in claim 6. The language of Claim 6 of the '724 patent describes the following claim:

> A portable computer system, comprising:
>
> ...
>
> a digital transmitter sending parallel digital video data to said external digital monitor, said digital monitor comprises a means for generating a cable sensing signal to be sent to said first external video port over the digital cable, thereby informing the video controller of the digital cable connection state of said first external port, said system further comprising a monitor power sensor detecting a presence of power applied to the external digital monitor, whereby a display enable signal is generated in the video controller and

> is sent to the transmitter to enable the digital video signals to be sent to the external digital monitor when the presence of power applied to the external digital monitor is detected.

'724 Patent, 11:58, 11:66-12:12.

b) Specification and Prosecution History

Figure 14 depicts the entirety of the cable sensing circuit, including components of the video port. The Patent's specification describes Figure 14, in part, as "a detailed diagram showing the LCD monitor cable sensing circuit." '724 Patent at 4:1-2.

The '724 Patent Abstract states that "the digital monitor generates a signal being sent to the second video port over the monitor cable, thereby informing the video controller of the monitor cable connection state." '724 Patent at Abstract.

c) Extrinsic Evidence

The parties cite to no extrinsic evidence.

d) Correct Construction

According to Lockheed Martin Corp. v. Space Sys./Loral, Inc., 324 F.3d 1308, 1319 (Fed Cir. 2003), "the function is properly identified as the language after the 'means for' clause and before the 'whereby' clause, [when a] whereby clause...merely states the result of the limitations in the claim adds nothing to the substance of the claim."[6] Here, the thereby clause merely states the result of the limitations in the claim and adds nothing to the claim's

[6] The parties agree that "thereby" and "whereby" mean the same thing.

substance. The Defendants have failed to establish that the thereby clause states a condition that is material to patentability and that, if left off, would change the substance of the invention.

Thus, the function is properly construed as "generating a cable sensing signal to be sent to first external video port over the digital cable." The means are properly construed as the DVCC and resistor R1 depicted in Figure 14 of the '724 Patent.

CONCLUSION

For the reasons set forth above, the disputed claim terms in the Patents-in-Suit are to be construed as reflected herein.

/s/ REP
Robert E. Payne
Senior United States District Judge

Richmond, Virginia
Date: July 30, 2015