UNITED STATES DISTRICT COURT
WESTERN DISTRICT OF WASHINGTON
AT SEATTLE

MICROSOFT CORPORATION,

Plaintiff,

v.

MOTOROLA INC., et al.,

Defendants.

MOTOROLA MOBILITY, INC., et al.,

Plaintiffs,

v.

MICROSOFT CORPORATION,

Defendant.

CASE NO. C10-1823JLR

ORDER GRANTING MICROSOFT'S MOTION FOR PARTIAL SUMMARY JUDGMENT THAT MEANS-PLUS-FUNCTION CLAIMS ARE INDEFINITE

I. INTRODUCTION

In this action, Plaintiffs Motorola Mobility, Inc. and General Instrument Corporation (collectively, "Motorola") sued Defendant Microsoft Corporation ("Microsoft") for infringement of claims 8-18 of United States Patent No. 7,310,374 ("the '374 Patent"), claims 6-11, 13, 14, 16, and 17 of United States Patent No. 7,310,375 ("the '375 Patent"), and claims 14-15, 18-20, 22, 23, 26-28, and 30 of United States Patent No. 7,310,376 ("the '376 Patent") (collectively, the "Patents-in-Suit").[1] Before the court is Microsoft's motion for partial summary judgment that the "means for decoding" and the "means for using" elements of the Patents-in-Suit are invalid as indefinite under 35 U.S.C. § 112. The court has considered Microsoft's motion (Mot. (Dkt. # 205)), Motorola's response (Resp. (Dkt. # 251)), Microsoft's reply (Reply (Dkt. # 266)), Motorola's sur-reply (Sur-Reply (Dkt. # 296)), Microsoft's response to Motorola's sur-reply (Sur-Reply Resp. (Dkt. # 299)), all papers filed in support and opposition to the motion, the balance of the record, and the governing law. In addition, the court heard oral argument from the parties on January 28, 2013. Being fully advised, the court GRANTS Microsoft's motion (Dkt. # 205).

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[1] This matter has a complex procedural history. Originally, the parties were involved in two separate actions, one in which Microsoft was the plaintiff, No. C10-1823JLR, and one in which Motorola was the Plaintiff, No. C11-0343JLR. On June 1, 2011, the court consolidated the two cases under Cause No. C10-1823JLR. (Dkt. # 66 at 12.) There are additional patents at issue in the consolidated action, but the court addresses only the three patents, subject of Microsoft's motion, listed above in this order. Because the patents at issue here are asserted by Motorola, for purposes of this order, the court refers to Motorola as the plaintiff and Microsoft as the defendant.

II. BACKGROUND

Motorola is the sole assignee of each of the Patents-in-Suit. (*See* '374 Patent; '375 Patent; '376 Patent.) Each of the Patents-in-Suit shares a common specification.[2] (*See id.*) Motorola contends that each Microsoft Windows 7 operating system and each Microsoft Internet Explorer 9 that are made, used, sold, or offered for sale in the United States or imported into the United States by Microsoft infringe the asserted claims of the Patents-in-Suit. (Jt. Claim Constr. Statement (Dkt. # 170) at 5.) Motorola asserts that Microsoft's products infringe the Patents-in-Suit both directly and indirectly. (*Id.*)

At a high level, the Patents-in-Suit disclose systems and methods for encoding and decoding a bitstream (or sequence) of digital video data.[3] (*See generally* '374 Patent; '375 Patent; '376 Patent.) The Patents-in-Suit explain that a picture in a digital video sequence can either be encoded as a "frame," comprising consecutives lines of the picture, or as two "fields," with the top field comprising the odd-numbered lines of the picture and the bottom field comprising the even-numbered lines of the picture. ('374 Patent at 1:42-58.) While encoding a picture in frame or field mode was done in prior art on a picture-by-picture basis (*id.* at 4:17-34), the summary of the invention states, "[t]he method entails encoding and decoding each of the *macroblocks* in each picture in said

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[2] For consistency and ease of reference, the court cites to the specification of the '374 Patent throughout this order.

[3] A more detailed explanation of the technology of the Patents-in-Suit is found in the court's Markman Order (Dkt. # 258).

stream of pictures in either frame mode or in field mode." (*Id.* at 2:58-60 (emphasis added).)

Thus, the systems and methods disclosed in Patents-in-Suit divide individual pictures into "macroblocks" which can be divided even further into "blocks" for efficient encoding and decoding. (*See* '374 Patent at 5:59-64.) Figure 2 of the '374 Patent shown below illustrates an entire picture divided into macroblocks, which are shown as number 201:

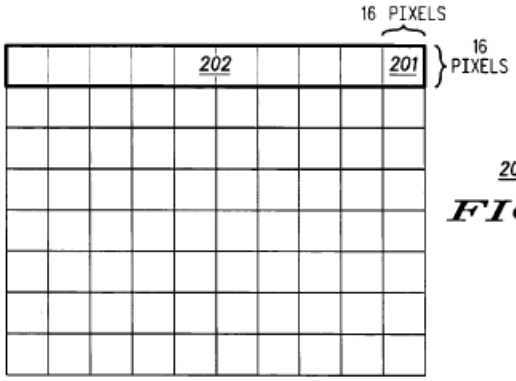

FIG. 2

('374 Patent at Figure 2.) According to the Patents-in-Suit, encoding a data stream of picture frames at a macroblock level can further optimize the compression of data if an encoder determines whether to encode an individual macroblock in field mode or in frame mode. The Patents-in-Suit refer to this encoding methodology as "adaptive frame/field" coding ("AFF Coding"). ('374 Patent at 6:49-55.) At a macroblock level, in "field mode," the lines of each macroblock are arranged to put even lines and odd lines together. (*Id.* at 7:54-67.) The even lines and odd lines are then encoded separately from one another. (*Id.* at 7:57-58.) In "frame mode," the even and odd lines remain together and are encoded together. (*Id.* at 7:46-50.) As explained by the specification, "[t]he

present invention extends the concept of picture level AFF to macroblocks." (*Id.* at 4:20-21.)

Once encoded by frame mode or field mode, the macroblock can be further divided into smaller blocks for use in a prediction algorithm, which further processes the data. (*See id.* at 7:1-3.) In a prediction algorithm, to take advantage of redundancies between picture frames and within an individual picture frame, only some smaller blocks will be fully encoded whereas other blocks will be predicted/encoded based on already encoded blocks. (*Id.* at 2:26-41.) Utilization of such a prediction algorithm further increases compression.

The Patents-in-Suit disclose two types of prediction algorithms for encoding macroblocks and smaller blocks within the macroblocks: intra and inter coding. In inter coding, the macroblock (or block) is encoded based a reference macroblock (or block) that has already been encoded. The reference macroblock (or block) may be in either the forward or backward temporal direction in relation to the macroblock (or block) being encoded. ('374 Patent at 5:4-21.) During encoding, predicted macroblocks (or blocks) are represented by a vector estimating the amount of temporal motion of the image(s) with respect to the reference macroblock. (*Id.* at 6:25-31.) Figure 4 below illustrates the use of a motion vector, numbered 406, to indicate the motion of an image, numbered 402 as it moves from picture frame to picture frame:

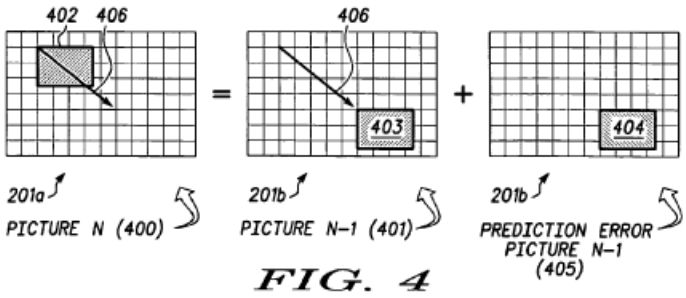

FIG. 4

('374 Patent at Figure 4.) The Patents-in-Suit also disclose that the motion vectors themselves may be encoded by referencing other motion vectors. (*Id.* at 9:38-45.)

In "intra coding," macroblocks (or blocks) are predicted based on neighboring macroblocks (or blocks) within the same picture frame, as opposed to using temporally distinct picture frames as reference macroblocks. (*Id.*)

To perform the encoding and decoding of the bitstream of data, the common specification of the Patents-in-Suit provides that an "encoder encodes the pictures and the decoder decodes the pictures." (*Id.* at 4:57-59.) Describing the encoder and decoder further, the specification explains:

> The encoder or decoder can be a processor, application specific integrated circuit (ASIC), field programmable gate array (FPGA), coder/decoder (CO-DEC), digital signal processor (DSP), or some other electronic device that is capable of encoding the stream of pictures. However, as used hereafter and in the appended claims, unless otherwise specification denoted, the term "encoder" will be used to refer expansively to all electronic devices that encode digital video content comprising a stream of pictures. The term "decoder" will be used to refer expansively to all electronic devices that decode digital video content comprising a stream of pictures.

(*Id.* at 4:59-5:3.)

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B. Claims at Issue in Microsoft's Invalidity Motion

There are three independent, apparatus claims at issue in Microsoft's motion: claim 14 of the '374 Patent, claim 13 of the '375 Patent, and claim 22 of the '376 Patent (collectively, the "Claims-at-Issue"). (Mot. at 5.) Moreover, claims 15-18 of the '374 Patent, claims 14 and 16 of the '375 Patent, and claims 23 and 26-28 of the '376 Patent are dependent on the three independent claims. The independent Claims-at-Issue are set forth below beginning with claim 14 of the '374 Patent, followed by claim 13 of the '375 Patent, and ending with claim 22 of the '376 Patent:

> 14. An apparatus for decoding an encoded picture from a bitstream, comprising:
>
> *means for decoding* at least one of a plurality of smaller portions at a time of the picture that is encoded in frame coding mode and at least one of said plurality of smaller portions at a time of the encoded picture in field coding mode, wherein each of said smaller portions has a size that is larger than one macroblock, wherein at least one block within at least one of said plurality of smaller portions at a time is encode in inter coding mode; and
>
> *means for using* said plurality of decoded smaller portions to construct a decoded picture.

(Claim 14, '374 Patent (emphases added).)

> 13. An apparatus for decoding an encoded picture from a bitstream, comprising:
>
> *means for selectively decoding* at least one of a plurality of smaller portions at a time of the encoded picture that is encoded in frame coding mode and at least one of said plurality of smaller portions at a time of the encoded picture in field coding mode; and
>
> *means for using* said plurality of decoded smaller portions to construct a decoded picture.

(Claim 13, '375 Patent (emphases added).)

22. An apparatus for decoding an encoded picture from a bitstream, comprising:

means for decoding at least one of a plurality of processing blocks at a time, each processing block containing a pair of macroblocks or a group of macroblocks, each macroblock containing a plurality of blocks, from said encoded picture that is encoded in frame coding mode and at least one of said plurality of processing blocks at a time that is encoded in field coding mode,

wherein said decoding is performed in a horizontal scanning path or a vertical scanning path; and

means for using said plurality of decoded processing blocks to construct a decoded picture.

(Claim 22, '376 Patent (emphases added).)

III. DISCUSSION

Microsoft contends that the "means for decoding" and "means for using" elements recited in the Claims-at-Issue are invalid as indefinite because the Patents-in-Suit do not adequately describe a corresponding structure. (Mot. at 5.) Microsoft asks the court to grant partial summary judgment of invalidity for claims of the Patents-in-Suit employing the "means for decoding" and "means for using" elements.

A. Summary Judgment Standard

Summary judgment is appropriate if the evidence, when viewed in the light most favorable to the non-moving party, demonstrates "that there is no genuine dispute as to any material fact and the movant is entitled to judgment as a matter of law." Fed. R. Civ. P. 56(a); *see Celotex Corp. v. Catrett*, 477 U.S. 317, 322 (1986); *Galen v. Cnty. of L.A.*, 477 F.3d 652, 658 (9th Cir. 2007). The moving party bears the initial burden of showing there is no genuine issue of material fact and that he or she is entitled to prevail as a matter of law. *Celotex*, 477 U.S. at 323. If the moving party meets his or her burden,

then the non-moving party "must make a showing sufficient to establish a genuine dispute of material fact regarding the existence of the essential elements of his case that he must prove at trial" in order to withstand summary judgment. *Galen*, 477 F.3d at 658.

B. Means-Plus-Function Limitations

Here, Microsoft and Motorola agree that the "means for decoding" and "means for using" elements constitute means-plus-function claim limitations. (*See* Mot. at 10-11; Resp.) A patentee may express an "element in a claim for a combination" "as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof." 35 U.S.C. § 112 ¶ 6. When a patentee invokes "means-plus-function," the "claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof." *Id.*

Means-plus-function claim limitations must satisfy the requirements of 35 U.S.C. § 112 ¶ 2. *S3 Inc. v. nVIDIA Corp.*, 259 F.3d 1364, 1367 (Fed. Cir. 2001). Paragraph 2 of section 112 of title 35 of the United States Code states, "[t]he specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention." 35 U.S.C. § 112 ¶ 2. Whether a claim complies with the definiteness requirement of 35 U.S.C. § 112 ¶ 2 "is a legal conclusion that is drawn from the court's performance of its duty as the construer of patent claims." *Personalized Media Commc'ns, LLC v. Int'l Trade Comm'n*, 161 F.3d 696, 705 (Fed. Cir. 1998); *see also nVIDIA* Corp., 259 F.3d at 1367 (citation omitted). Similarly, "[a] determination that a patent claim is invalid for failure to meet the definiteness requirement of 35 U.S.C. § 112, paragraph 2, is a legal conclusion.

Intellectual Prop. Dev., Inc. v. UA–Columbia Cablevision of Westchester, Inc., 336 F.3d 1308, 1318 (Fed. Cir. 2003) (internal quotation omitted).

Construction of a means-plus-function limitation includes two steps. "First, the court must determine the claimed function. Second, the court must identify the corresponding structure in the written description of the patent that performs the function." *Applied Med. Res. Corp. v. U.S. Surgical Corp.*, 448 F.3d 1324, 1332 (Fed. Cir. 2006) (internal citations omitted). The parties agree—aside from immaterial differences in their respective articulations—that the function of the "means for decoding" term is precisely the language of the claim following the "means for" language. For instance, in claim 14 of the '374 Patent, the parties agree that the function is "decoding at least one of a plurality of smaller portions at a time of the picture that is encoded in frame coding mode and at least one of said plurality of smaller portions at a time of the encoded picture in field coding mode, wherein each of said smaller portions has a size that is larger than one macroblock." (*See* Resp. at 14.) Thus, the parties agree that each of the "means for decoding" terms has the primary function of "decoding." Similarly, the parties agree that the function of the "means for using" terms is precisely the language following the "means for" language. Thus, the agreed function for claim 14 of the '374 Patent is "using said plurality of decoded smaller portions to construct a decoded picture." (*See id.* at 23.)

A structure disclosed in the specification qualifies as a "corresponding structure" if the specification or the prosecution history "clearly links or associates that structure to the function recited in the claim." *B. Braun Med., Inc. v. Abbott Labs.*, 124 F.3d 1419,

1424 (Fed. Cir. 1997). Even if the specification discloses a "corresponding structure," the disclosure must be adequate; the patent's specification must provide "an adequate disclosure showing what is meant by that [claim] language. If an applicant fails to set forth an adequate disclosure, the applicant has in effect failed to particularly point out and distinctly claim the invention as required by the second paragraph of section 112." *In re Donaldson Co.*, 16 F.3d 1189, 1195 (Fed. Cir. 1994) (en banc). Under 35 U.S.C. § 112 ¶ 2 and ¶ 6, therefore, "a means-plus-function clause is indefinite if a person of ordinary skill in the art would be unable to recognize the structure in the specification and associate it with the corresponding function in the claim." *AllVoice Computing PLC v. Nuance Commc'ns., Inc.*, 504 F.3d 1236, 1241 (Fed. Cir. 2007) (citing *Atmel Corp. v. Info. Storage Devices, Inc.*, 198 F.3d 1374, 1381-82 (Fed. Cir. 1999)). Here, the parties agree that the corresponding structure to both the "means for decoding" and "means for using" terms is a "decoder." (*See* Resp. at 15, 23.) The parties disagree, however, on the adequacy of the decoder disclosure pursuant to 35 U.S.C. §112 ¶ 2 and ¶ 6.

First, the parties dispute whether the common specification of the Patents-in-Suit must disclose an algorithm. Microsoft contends that it must (Reply at 5-7), whereas Motorola argues that the decoder disclosure on its own is an adequate disclosure showing what is meant by the "means for decoding" and "means for using" terms of the Claims-at-Issue. (Resp. at 6-12.) In cases involving a special purpose computer-implemented means-plus-function limitation, the Federal Circuit "has consistently required that the structure disclosed in the specification be more than simply a general purpose computer or microprocessor." *Aristocrat Techs. Austl. Pty Ltd. v. Int'l Game Tech.*, 521 F.3d 1328,

1333 (Fed. Cir. 2008). In such cases, the Federal Circuit requires that the specification "disclose an *algorithm* for performing the claimed function." *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1367 (Fed. Cir. 2008) (emphasis added); *Aristocrat*, 521 F.3d at 1333 ("[I]n a means-plus-function claim 'in which the disclosed structure is a computer, or microprocessor, programmed to carry out an algorithm, the disclosed structure is not the general purpose computer, but rather the special purpose computer programmed to perform the disclosed algorithm.'") (quoting *WMS Gaming, Inc. v. Int'l Game Tech.*, 184 F.3d 1339, 1349 (Fed. Cir. 1999)). The specification can express the algorithm "in any understandable terms including as a mathematical formula, in prose, or as a flow chart, or in any other manner that provides sufficient structure." *Finisar Corp. v. DirecTV Grp., Inc.*, 523 F.3d 1323, 1340 (Fed. Cir. 2008) (internal citation omitted). Simply disclosing software, however, "without providing some detail about the means to accomplish the function[,] is not enough." *Id.* at 1340-41 (internal citation omitted).

Motorola contends that *WMS Gaming*, and its progeny (including *Aristocrat*), do not apply to the "means for decoding" and "means for using" terms because the *WMS Gaming* line of cases applies only when the specification discloses "mere general purpose hardware as the structure." (Resp. at 10-11). According to Motorola, this case is different because the common specification discloses a "decoder," which is more definite than merely a general purpose computer and is a disclosure understood by one of ordinary skill to be a known structure. In support of its contention, Motorola submits the declaration of Dr. Timothy Drabik who explains that from reading the patents he would

understand the disclosed decoder to be a well-known class of digital video decoders that decode encoded digital video content. (Drabik Decl. (Dkt. # 252) ¶¶ 18-21.)

The court is not persuaded by Motorola. As a starting point, Motorola appears to misstate the law. Disclosure of an algorithm is required when the "disclosed structure is a computer, or microprocessor, *programmed to carry out an algorithm*," *WMS Gaming*, 184 F.3d at 1349 (emphasis added), and not as Motorola suggests only when the disclosed structure is "mere general purpose hardware as the structure" (Resp. at 10-11). The distinction is important because Motorola's recitation of the law is more limiting in circumstances where algorithm disclosure is required to provide structure to a means-plus-function limitation. In *WMS Gaming*, the Federal Circuit criticized the district court, which had determined that the structure disclosed in the specification to perform the claimed function was "an algorithm executed by a computer." *WMS Gaming*, 184 F.3d at 1348. The Federal Circuit found that the district court erred "by failing to limit the claim to the algorithm disclosed in the specification." *Id.* Thus, *WMS Gaming* clearly required disclosure of an algorithm even when the specification disclosed a computer executing an algorithm, and not merely general purpose hardware.

In a later case, the Federal Circuit made the same point, stating that a "computer-implemented means-plus-function term is limited to the corresponding structure disclosed in the specification and equivalents thereof, and the corresponding structure is the algorithm." *Harris Corp. v. Ericsson Inc.*, 417 F.3d 1241, 1253 (Fed. Cir. 2005). The *Harris* court characterized the rule of *WMS Gaming* as follows: "[T]he corresponding structure for a § 112 ¶ 6 claim for a computer-implemented *function* is the algorithm

disclosed in the specification." 417 F.3d at 1249 (emphasis added). Accordingly, where the disclosed structure corresponding to a means-plus-function element is a computer-implemented algorithm, the algorithmic structure must be disclosed.

In *Aristocrat*, the Federal Circuit explained the rationale behind the algorithm requirement:

> For a patentee to claim a means for performing a particular function and then to disclose only a general purpose computer as the structure designed to perform that function amounts to pure functional claiming. Because general purpose computers can be programmed to perform very different tasks in very different ways, simply disclosing a computer as the structure designated to perform a particular function does not limit the scope of the claim to "the corresponding structure, material, or acts" that perform the function, as required by section 112 paragraph 6.

Aristocrat, 521 F.3d at 1333.

Here, the only portion of the specification concerning the structure of the identified decoder lists several examples: an application specific integrated circuit ("ASIC"), a field programmable gate array ("FPGA"), a coder/decoder ("CO-DEC"), or a digital signal processor ("DSP"). From reading the patent, the parties' briefing, and the expert report of Timothy Drabik, it is the court's understanding that each of these devices amounts to a chip programmed to execute the agreed-to function of the "means for decoding" and "means for using" elements. Indeed, Motorola's expert, Mr. Drabik, states that each of the listed decoder examples must be programmed by a person of ordinary skill in the art to perform the function of "means for decoding" and "means for using" limitations. (Drabik Decl. ¶ 25 ("A person of ordinary skill in the art would have understood how to write Verilog code for the well-known decoder and that, for example,

a single Verilog description of a decoder could be effectively 'cast into different target technologies, such as ASIC, FPGA, DSP, etc.").) Nowhere in his declaration does Mr. Drabik assert that any device in existence may perform the patented invention without further programming. (*See generally* Drabik Decl.) For its part, Microsoft provides substantial evidence by way of citations to technical journals and dictionaries that each of the examples is nothing more than a computer chip that must be programmed or designed to perform the desired function. (Mot. at 8-9.) Hence, based on the record before the court, the disclosed examples of the decoder in the specification amount to general purpose devices programmed to perform the function of the claimed means limitation, and therefore, are indistinguishable from the general purpose computer in *WMS Gaming* and *Aristocrat*. *See In re Aoyama*, 656 F.3d 1293, 1299 (Fed. Cir. 2011) (holding patent application invalid as indefinite because patent application failed to disclose an algorithm despite patent specification's explanation that each component of the invention could be implemented in hardware or software that included ASICs and FPGAs as examples of such hardware).

The court finds the disclosure of a decoder on its own to be insufficient structure for another reason: the decoder is defined functionally by the specification. Although the specification provides the previously discussed examples of a decoder (ASIC, FPGA, CO-DEC, and DSP), in the very same sentence, the specification states that the decoder may also be "some other electronic device that is capable of encoding the stream of pictures." ('374 Patent at 4:62-64.) Indeed, in the only place the specification affirmatively defines the decoder it states: "The term 'decoder' will be used to refer

expansively to all electronic devices that decode digital video content comprising a stream of pictures." (*Id.* at 1-3.) Through this language, the specification clearly defines the identified decoder structure in a functional manner. Without more, a decoder—defined as all electronic devices that decode video content—cannot be said to provide sufficient structure for the function of "decoding" portions of an encoded picture, as required by the Claims-at-Issue. Because neither the examples of a decoder, nor the definition of a decoder, identified in the specification amount to anything more than a programmed general computer or a functional description, the court requires disclosure of an algorithm corresponding to the "means for decoding" and "means for using" limitations.

A disclosed structure or algorithm corresponds to a means element "only if the specification or the prosecution history clearly links or associates that structure to the function recited in the claim." *B. Braun Med., Inc. v. Abbott Labs*, 124 F.3d 1419, 1424 (Fed. Cir. 1997). For each of the "means for decoding" and "means for using" terms, Motorola sets forth a proposed algorithm and identifies passages and figures in the specification as those that disclose this algorithm. (Resp. at 14-25.) None suffice to disclose a sufficient algorithm for the "means for decoding" limitations.[4]

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[4] Because the court concludes that the common specification of the Patents-in-Suit provides no algorithm (and therefore no structure) for the "means for decoding" limitation, the court declines to examine the common specification for the existence of structure corresponding to the "means for using" limitation.

1. "Means for Decoding" Limitation of Claim 14 of the '374 Patent

The relevant portion of the "means for decoding" limitation of claim 14 of the '374 Patent reads:

> *means for decoding* at least one of a plurality of smaller portions at a time of the encoded picture that is encoded in frame coding mode and at least one of said plurality of smaller portions at a time of the encoded picture in field coding mode, wherein each of said smaller portions has a size that is larger than one macroblock, wherein at least one block within at least one of said plurality of smaller portions at a time is encoded in *inter coding mode* . . . .

(Claim 14, '374 Patent (emphases added).) Motorola proposes the following algorithm, which Motorola contends corresponds to the "means for decoding" limitation found in claim 14:

> (1) receives from a bitstream information including pairs of macroblocks and a frame/field flag before each macroblock pair that indicates which mode, frame mode or field mode, is used in coding the macroblock pairs; and (2) performs inter prediction on blocks of the macroblock pairs in frame mode and field mode using at least one of the median, average, weighted average, "yes/no method," "always method," "selective method," "alt selective method," or directional segmentation prediction.

(Resp. at 14.)

In support of its proposed algorithm, Motorola identifies several passages and figures from the specification, but the identified passages and figures describe only various methods of encoding video data, but do not relate to decoding. As an initial matter, as explained by the common specification of the Patents-in-Suit, encoding and decoding are entirely distinct functions. Thus, a portion of the specification related to encoding is in no way relevant to decoding, and thus an algorithm for encoding cannot be said to be "clearly linked" to a decoding function.

Motorola cites to the '374 Patent at 8:46-65, which describes a field/frame flag, but this passage clearly relates to encoding and not decoding: "In AFF coding at the macroblock level, a frame/field flag bit is preferably included in a picture's bitstream to indicate which mode, frame mode or field mode, is used in the *encoding* of each macroblock." (Resp. at 11; '374 Patent at 8:46-49 (emphasis added).) Next, Motorola cites to Figure 11, but there is no indication that Figure 11 is linked to decoding. (Resp. at 11.) Motorola also cites to Figure 7 (*id.*), which is described in the specification as relating to encoding. ('374 Patent at 7:44-58.) Additionally, Motorola cites to the specification from columns 9:9 through 12:56, as well as Figure 12, as allegedly providing an algorithm. (Resp. at 12.) Throughout these portions of the specification, encoding (not decoding) is exclusively described. ('374 Patent at 3:62-65 ("FIG. 12 shows a block that is to be *encoded* . . . .") (emphasis added).)

2. "Means for Decoding" Limitation of Claim 13 of the '375 Patent

The relevant portion of the "means for decoding" limitation of claim 13 of the '375 Patent states:

> *means for selectively decoding* at least one of a plurality of smaller portions at a time of the encoded picture that is encoded in frame coding mode and at least one of said plurality of smaller portions at a time of the encoded picture in field coding mode, wherein each of said smaller portions has a size that is larger than one macroblock, wherein at least one block within at least one of said plurality of smaller portions is encoded in *intra coding mode* at a time . . . .

(Claim 13, '375 Patent (emphases added).) Motorola proposes the following algorithm, which Motorola contends corresponds to the "means for decoding" limitation found in claim 13:

> (1) receives from a bitstream information including pairs of macroblocks and a frame/field flag before each macroblock pair that indicates which mode, frame mode or field mode, is used in coding the macroblock pairs; and (2) performs intra prediction on blocks of the macroblock pairs in at least of the vertical, horizontal, DC prediction, diagonal down/left, diagonal down/right, vertical-left, horizontal-down, vertical-right, horizontal-up, or plane prediction modes, using neighboring blocks determined by at least one of Rule 1, Rule 2, Rule, 3 or Rule 4.

(Resp. at 18.)

Essentially, Motorola proposes an algorithm related to decoding a bitstream of video data employing intra prediction—use of neighboring blocks within the same picture frame to compress digital video data. (Resp. at 18.) As with the Motorola's proposed algorithm for claim 14 of the '374 Patent, Motorola's algorithm incorporates a frame/field flag, and Motorola refers to the same portions of the specification in an effort to demonstrate that the specification provides a description of a field/frame flag in the context of decoding. As explained, Motorola's citations to the specification for the frame/field flag expressly relate to encoding and not decoding.

Motorola's algorithm also incorporates nine possible prediction modes and states that the algorithm will employ "at least one of" those prediction modes. The prediction modes listed in Motorola's proposed algorithm are found in the specification entirely within the context of encoding, not decoding. Indeed, the paragraph preceding the list of nine "prediction modes" explains that the predictions modes are used for "coding" (a word used interchangeably with "encoding" in the common specification) blocks to achieve "more compression" (compression being the result of encoding, whereas decompression is the result of encoding). ('374 Patent at 14:37-45.) Nowhere does the

specification discuss any of the nine prediction modes in the context of decoding, and thus, it cannot be said that the specification clearly links the nine prediction modes found in Motorola's proposed algorithm to the function of decoding.

Finally, Motorola's proposed decoding algorithm includes "using neighboring blocks" as determined by one of four "Rules." Motorola directs the court to the specification at 15:52-16:63 to support this inclusion as proposed structure for the function of decoding. (Resp. at 18.) Although the identified portion of the specification does in fact relate to decoding, no portion of the specification actually explains *how* decoding would be performed. *In re Aoyama*, 656 F.3d at 1298 ("This court agrees with the Board's conclusion that Figure 8 'fails to describe, even at a high level, how a computer could be programmed to produce the structure that provides the results described in the boxes.'"). Instead, the identified portion of the specification explains which blocks of a pair of macroblocks would be considered for purposes of decoding in various block configurations. (*See, e.g.*, '374 Patent at 16:12-18 ("If the above macroblock pair (170) is decoded in field mode, then for blocks number 0, 1, 4, and 5 in the top-field macroblock (173), blocks numbered 10, 11, 14 and 15 respectively in the top-field macroblock (173) of the above macroblock pair (170) *shall be considered as the above neighboring blocks to the current macroblock pair* (171) as shown in FIG. 17a.") (emphasis added).) Although the specification describes how one of skill in the art would ascertain what blocks to consider when decoding, the specification provides no guidance as to how one of ordinary skill would actually decode the considered blocks. Thus, the court concludes that the specification contains no disclosure that supports Motorola's

proposed algorithm (or any other algorithm) for corresponding structure to the decoding function required by the "means for selectively decoding" limitation of claim 13 of the '375 Patent.

3. "Means for Decoding" Limitation of Claim 22 of the '376 Patent

The relevant portion of the "means for decoding" limitation of claim 13 of the '375 Patent states:

> *means for decoding* at least one of a plurality of processing blocks at a time, each processing block containing a pair of macroblocks or a group of macroblocks, each macroblock containing a plurality of blocks, from said encoded picture that is encoded in frame coding mode and at least one of said plurality of processing blocks at a time that is encoded in field coding mode,
>
> wherein said decoding is performed in a horizontal scanning path or a vertical scanning path . . . .

(Claim 22, '376 Patent (emphases added).) Motorola proposes the following algorithm, which Motorola contends corresponds to the "means for decoding" limitation found in claim 22:

> (1) receives from a bitstream information including pairs of macroblocks and a frame/field flag before each macroblock pair that indicates which mode, frame mode or field mode, is used in coding the macroblock pairs; and (2) decodes the macroblock pairs of a picture from left to right and from top to bottom, as shown in FIG. 9 path 900, or from top to bottom and from left to right, as shown in FIG 9 path 901; and (3) within each frame macroblock pair decodes the top macroblock of the macroblock pair first, followed by the bottom macroblock, and within each field macroblock pair decodes the top field macroblock of the macroblock pair first, followed by the bottom field macroblock.

(Resp. at 20-21.)

As with claim 14 of the '374 Patent and claim 13 of the '375 Patent, Motorola's citations in support of its three-part proposed algorithm relate to encoding, not decoding.

The first part of Motorola's proposed algorithm again incorporates a frame/field flag, but again, Motorola's citation to the specification only describes encoding, not decoding.

With respect to the second part of Motorola's algorithm, Motorola cites to Figure 9 of the specification, as well as the language of the specification at 7:44-48. (Resp. at 21-22.) Figure 9 illustrates the horizontal and vertical scanning paths for macroblock coding, and the specification describes Figure 9 in terms of encoding, not decoding. (*See, e.g.*, '374 Patent at 8:7-10 ("In the horizontal scanning path (900), the macroblock pairs (700) of a picture (200) are *coded* from left to right and from top to bottom, as shown in FIG. 9") (emphases added).) Similarly, the passage at 7:44-48 only references encoding, not decoding. (*Id.* at 7:44-46 ("FIG. 7 illustrates an exemplary pair of macroblocks (700) that can be used in AFF coding on a pair of macroblocks according to an embodiment of the present invention.").)

Finally, the third part of Motorola's algorithm recites decoding in a particular order. Motorola directs the court again to Figure 9, which as previously explained is described by the specification in terms of encoding, not decoding. Motorola also cites to the specification at 8:14-18 (Resp. at 22), but this passage of the specification expressly describes encoding: "For frame mode coding, the top macroblock of a macroblock pair (700) is *coded* first, followed by the bottom macroblock. For field mode coding, the top field macroblock of a macroblock pair is *coded* first followed by the bottom field macroblock." ('374 Patent at 8:14-18 (emphases added).) Because each of Motorola's identified portions of the specification relate exclusively to encoding, it cannot be said that the identified portions are clearly linked to a proposed algorithm for decoding.

Accordingly, claim 22 of the '376 Patent (as well as all claims dependent thereon) is invalid for failure to provide structure to the "means for decoding" limitation.

C. Motorola's Expert

Through its expert, Dr. Drabik, Motorola contends that a person of ordinary skill in the art would understand the specification to connote a known class of video decoder structures corresponding to the "means for decoding" and "means for using" limitations. (Resp. at 8-9; Drabik Decl. ¶¶ 49-51.) Motorola asserts that because one of ordinary skill in the art would understand the structure and boundaries of the "means for decoding" and "means for using" limitations, it has satisfied the indefiniteness requirement of 35 U.S.C. § 112, ¶ 2. In support of its argument, Motorola directs the court to numerous cases, which Motorola contends stand for the proposition that expert testimony that a person of skill in the art would understand the structure corresponding to the function saves a patent from invalidity due to indefiniteness. (Resp. at 8-9.[5])

The cases cited by Motorola are distinguishable for generally the same reason: in each of the cited cases the specification disclosed a structure that would in fact perform the claimed function without modification. For example, in *Via Techs*, the patent at issue related to a new standard, promulgated by Intel, for the electronic interface and signal protocols by which devices in a computer system communicate. *Via Techs*, 319 F.3d at 1359. "Fast Write" was the name of an optional protocol in the new standard, and the

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[5] During oral argument, Motorola emphasized the following cases for the court's consideration: *Intel Corp. v. Via Techs. Inc.*, 319 F.3d 1357 (Fed. Cir. 2003); *Tech. Licensing Corp. v. Videotek, Inc.*, 545 F.3d 1316 (Fed. Cir. 2008); *S3 Inc. v. nVIDIA Corp.*, 259 F.3d 1364 (Fed. Cir. 2001); and *Telcordia Techs., Inc. v. Cisco Sys., Inc.*, 612 F.3d 1365 (Fed. Cir. 2010).

specification of the patent-in-suit described the Fast Write protocol through three diagrams, 35 signal charts and a detailed written description. *Id.* at 1366. The Federal Circuit held that the disclosed structure of "core logic of a computer modified to perform Fast Write" was not inadequate structure for the means-plus-function limitations of "an element adapted to selectively write data directly to said peripheral device" and "a selection device adapted to determine whether data is able to be written directly to said peripheral device." *Id.* at 1366-67.

This case is different from *Via Techs*. There, the specification described the Fast Write protocol, which modified the core logic of a computer to provide sufficient structure to perform the claimed functions. *Id.* at 1366. Here, the claimed functions require decoding an encoded picture, and the parties have agreed that a decoder will perform the function, but there is nothing in the specification to explain how the decoding is to be accomplished. In other words, the analogous Fast Write description of how to modify the core logic of a computer in *Via Techs* is missing from the common specification of the Patents-in-Suit. Instead, the decoder is defined broadly and functionally to mean anything that can decode.

For similar reasons, the *Telcordia* case, also cited by Motorola, is inapposite. In *Telcordia*, the patents at issue claimed methods and systems for transmission of data in a telecommunications network. *Telcordia*, 612 F.3d at 1367. The Federal Circuit found that "circuitry at a controller that determines if a defect exists with the multiplexed subrate communications" was adequate corresponding structure for performing the claimed term "monitoring means," a term which was construed to require the function of

"evaluating the integrity of the multiplexed subrate communications on the first ring and the second ring." *Id.* at 1376-77. Unlike the specification of the Patents-in-Suit, the specification of the patents in *Telcordia* disclosed a description of the structure:

> Each node continuously monitors and evaluates the integrity of the multiplexed subrate signals arriving at the node. Illustratively, this could be accomplished by detecting the absence of a carrier signal in an analog signal environment, or the lack of any incoming signal in a digital environment. When node 1 recognizes major line fault 122 in ring 100, controller 118 inserts an error signal onto the six subrate channels. This could illustratively be accomplished by inserting a string of 1's on each channel in a digital environment. Node 4 performs the identical activity by similarly placing an error signal on the six subrate channels of ring 101.

Id. at 1376. The specification of the Patents-in-Suit lack this type of disclosure (and in fact provide no disclosure at all) providing structure to the claimed decoding function.

Motorola also directs the court to *S3 Inc. v. nVIDIA Corp.*, 259 F.3d 1364. In *nVIDIA*, the Federal Circuit held that a "selector" was adequate corresponding structure for performing the "selectively receiving" (either video information data or video display information data) function, even though the corresponding electronic circuitry was not contained in the specification. *nVIDIA Corp.*, 259 F.3d at 1371. The patentee's expert testified that one of ordinary skill in the field would readily recognize that the selector in the specification as an electronic device known as a multiplexer, thereby limiting the structure to multiplexers and equivalents thereof. *Id.* at 1370. The expert further testified that the well-known multiplexer would perform the recited function. *Id.* at 1370-72.

Motorola contends that similar to the patentee's expert in *nVIDIA*, Dr. Drabik has testified that a decoder is a well-known structure for decoding encoded video data and this alone is sufficient to satisfy the definiteness requirement of § 112, ¶ 2. (Resp. at 8-9;

Drabik Decl. ¶¶ 49-52.) The distinction between *nVIDIA* and the present case is that whereas the multiplexer structure in *nVIDIA* would in fact perform the stated function of "selectively receiving," Dr. Drabik does not contend that identified structure of a video decoder could perform, without modification, the function of decoding as claimed by the Patents-in-Suit. During oral argument, Microsoft explained, and Motorola did not contest, that the general video decoder identified by Dr. Drabik could not perform the decoding function claimed by the Patents-in-Suit, but must be modified to do so.[6] Dr. Drabik admits this much by testifying through his declaration that a person of ordinary skill would understand how to write Verilog code to program the decoder to perform the claimed function. (Drabik Decl. ¶25.) As explained above, the specification's lack of disclosure of how to make this modification renders the claims incorporating the "means for decoding" limitations indefinite.[7]

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[6] In fact, Motorola could not contest such a contention. The novelty of the Patents-in-Suit is their encoding and decoding methodology. Thus, were Dr. Drabik to testify that a decoder in existence at the time of filing of the original patent application could decode in the manner prescribed by the claims, the Patents-in-Suit would be rendered invalid on other grounds, such as obviousness or anticipation.

[7] For much the same reason that *nVIDIA* does not control this case, neither does *Videotek*, another case cited by Motorola. The patents in Videotek related to the separation of synchronization signals from video signals in the transmission of data to a television set. *Videotek*, 545 F.3d at 1320. In *Videotek*, the Federal Circuit found that a "video standard detector" provided sufficient corresponding structure for performing the means-plus-function limitation that read: "circuitry to provide a format signal changeable in response to the format of said video type signal." *Id.* at 1337-39. The patentee's expert in *Videotek* testified that the "video standard detector" structure to perform the claimed function was available and known to a person skilled in the art at the time the original patent application was filed. *Id.* at 1339. Similar to *nVIDIA*, and unlike this case, the identified structure would perform the claimed function without modification.

Here, Motorola employed "means-plus-function" claiming and then defined the corresponding structure as anything that performs the claimed function. Simply put, this amounts to an unbounded claim encompassing all means for performing the decoding function. While it is undisputed that the question of whether a claim is indefinite is based on how the claim limitation would be understood by one of skill in the art, "the testimony of one of ordinary skill in the art cannot supplant the total absence of structure from the specification." *Default Proof Credit Card Sys., Inc. v. Home Depot U.S.A., Inc.*, 412 F.3d 1291, 1302 (Fed. Cir. 2005); *see also Biomedino, LLC v. Waters Techs. Corp.*, 490 F.3d 946, 950-53 (Fed. Cir. 2007). The prohibition against using expert testimony in this manner is a direct consequence of the requirement that the specification itself adequately disclose the corresponding structure. *AllVoice Computing*, 504 F.3d at 1240 ("The test for definiteness asks whether one skilled in the art would understand the bounds of the claim when read in light of the specification.") (citation omitted).

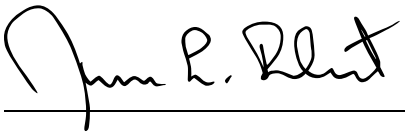
Finally, as stated, decoding and encoding are entirely different functions. Thus, even were a person of ordinary skill in the art able to devise an algorithm for decoding the function from the disclosed encoding description, that alone does not rescue the disputed means limitations from indefiniteness. Were that the case, any means-plus-function limitation could be saved from indefiniteness by an expert's testimony that he or she could have written computer code to perform the recited function based on unrelated disclosures in the specification. The specification needs to provide a decoding algorithm from which to base the understanding of one skilled in the art, and the court can find no such algorithm within the specification. Instead, the "means for decoding" limitations

claim all corresponding structure under the sun by expansively defining the function in the specification as anything that decodes digital data. This definition renders the "means for decoding" limitation invalid for indefiniteness.

IV. CONCLUSION

Based on the foregoing, the court GRANTS Microsoft's motion (Dkt. # 205) for partial summary judgment that the "means for decoding" limitations of the Patents-in-Suit are invalid as indefinite under 35 U.S.C. § 112. Accordingly, the court declares the following claims invalid: claims 14-18 of U.S. Patent No. 7,310,374; claims 13, 14, and 16 of U.S. Patent No. 7,310,375; and claims 22, 23, and 26-28 of U.S. Patent No. 7,310,376.

Dated this 6th day of February, 2013.



JAMES L. ROBART
United States District Judge