Exhibit 30

Nokia’s Counterclaims and Demand for Trial by Jury dated May 23, 2007.

IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF WISCONSIN

QUALCOMM INCORPORATED,

Plaintiff,

v. CASE NO. 07 C 0187 C

NOKIA CORPORATION and NOKIA, INC.,

Defendants.

**COUNTERCLAIMS OF NOKIA CORPORATION AND NOKIA, INC.
AND DEMAND FOR TRIAL BY JURY**

Defendants and Counterclaimants Nokia Corporation and Nokia, Inc., for their counterclaims against Plaintiff and Counterclaim Defendant QUALCOMM Incorporated ("Qualcomm"), allege the following:

THE PARTIES

1. Defendant and Counterclaimant Nokia Corporation is a Finnish corporation having its principal place of business at Keilalahdentie 4, P.O. Box 226, FIN-00045 Espoo, Finland. Nokia Corporation owns by assignment the entire right, title, and interest in and to each of the Asserted Patents.

2. Defendant and Counterclaimant Nokia, Inc. is a corporation organized under the laws of Delaware and headquartered in Irving, Texas. Nokia, Inc. is a subsidiary of Nokia Corporation.

3. Defendant Qualcomm is a corporation existing under the laws of the state of Delaware, with its principal place of business at 5775 Morehouse Drive, San Diego, California, 92121.

JURISDICTION AND VENUE

4. This Court has subject matter jurisdiction over the Counterclaims of Nokia Corporation and Nokia, Inc. under the patent laws of the United States, Title 35, United States Code, §§ 1 et seq. This Court has subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338(a) because this case arises out of the federal patent laws.

5. By filing its Complaint, Qualcomm has consented to the personal jurisdiction of this Court. Nokia Corporation and Nokia, Inc. are also informed and believe and thereon allege that Qualcomm is doing business in Wisconsin and in this district.

6. Venue is proper in this District pursuant to 28 U.S.C. §§ 1391(b) and 1391(c) and/or 28 U.S.C. § 1400(b).

THE PATENTS-IN-SUIT

7. On April 18, 2006, U.S. Patent No. 7,031,687 (the "'687 Patent"), entitled "Balanced Circuit Arrangement and Method for Linearizing Such an Arrangement," was duly and legally issued to the inventors Kalle Kivekäs and Aarno Pärssinen and is assigned to Nokia Corporation. A true and correct copy of the '687 Patent is attached hereto as Exhibit A.

8. On December 19, 2006, U.S. Patent No. 7,151,915 (the "'915 Patent"), entitled "Dual Mode Voltage Controlled Oscillator Having Controllable Bias Modes and Power Consumption," was duly and legally issued to the inventors Jarmo Heinonen, Vesa Viitaniemi, Kai Leino, and Jyrki Koljonen and is assigned to Nokia Corporation. A true and correct copy of the '915 Patent is attached hereto as Exhibit B.

9. On September 5, 2000, U.S. Patent No. 6,115,593 (the "'593 Patent'), entitled "Elimination of D.C. Offset and Spurious AM Suppression in a Direct Conversion Receiver," was duly and lawfully issued to the inventors Petteri Alinikula, Hans-Otto Scheck,

and Kari-Pekka Estola and is assigned to Nokia Corporation. A true and correct copy of the '593 Patent is attached hereto as Exhibit C.

10. On September 18, 2001, U.S. Patent No. 6,292,474 (the "'474 Patent"), entitled "Multi-Frequency Band Multi-Mode Radio Receiver and Associated Method Having Shared Circuit Elements," was duly and lawfully issued to the inventors Fazal Ali, Thomas C. Wakeham, and Konstantina A. Rovos and is assigned to Nokia Corporation. A true and correct copy of the '474 Patent is attached hereto as Exhibit D.

11. On March 30, 2004, U.S. Patent No. 6,714,091 (the "'091 Patent"), entitled "VCO with Programmable Output Power," was duly and lawfully issued to the inventors Soren Norskov, Carsten Rasmussen, and Niels Thomas Hedegaard Povlsen and is assigned to Nokia Corporation. A true and correct copy of the '091 Patent is attached hereto as Exhibit E.

12. On April 27, 1999, U.S. Patent No. 5,898,740 (the "'740 Patent"), entitled "Power Control Method in a Cellular Communication System, and a Receiver," was duly and lawfully issued to the inventors Timo Laakso and Hannu Hakkinen and is assigned to Nokia Corporation. A true and correct copy of the '740 Patent is attached hereto as Exhibit F.

13. The '687, '915, '593, '474, '091, and '740 Patents described in paragraphs 7 through 12 above, are herein referred to collectively as "Nokia's Patents-in-Suit." Nokia's Patents-in-Suit relate generally to technology used, for example, to reduce the battery consumption, size and cost of and to improve the performance and efficiency of wireless communication devices.

QUALCOMM'S INFRINGEMENT OF NOKIA'S PATENTS-IN-SUIT

14. On information and belief, Qualcomm manufactures, uses, sells, offers for sale in the United States, and/or imports into the United States chipsets and/or other products that practice one or more of the claims of Nokia's Patents-in-Suit ("Qualcomm Products").

15. On information and belief, Qualcomm directly or indirectly infringes, literally and/or under the doctrine of equivalents, Nokia's Patents-in-Suit, pursuant to 35 U.S.C. §§ 271(a), (b), (c) and/or (f), by making, using, selling, offering for sale, and/or importing to the United States Qualcomm Products that practice one or more of the claims of Nokia's Patents-in-Suit and/or by practicing one or more of the claimed methods of Nokia's Patents-in-Suit.

FIRST COUNTERCLAIM (OF NOKIA CORPORATION)

(INFRINGEMENT OF THE '687 PATENT)

16. Nokia Corporation realleges and incorporates by reference each and every allegation contained in paragraphs 1 through 15 as if fully set forth herein.

17. On information and belief, Qualcomm makes, uses, sells, or offers for sale in the United States, and/or imports into the United States Qualcomm devices, including but not limited to at least one of the following Qualcomm devices: RFR6120, RFR6122, RFR6125, RFR6185, RFR6220, RFR6250, RFR6275, RFR6500, QTP-6800, TM7200 and/or TM6280 that, alone and/or in combination with other devices, directly and/or indirectly infringes and is continuing to infringe, literally and/or under the doctrine of equivalents, the '687 Patent directly or indirectly in violation of 35 U.S.C. § 271.

18. On information and belief, Qualcomm has infringed and is continuing to infringe the '687 Patent by contributing to and/or inducing the infringement by others of claims of the '687 Patent in violation of 35 U.S.C. § 271.

19. As a result of Qualcomm's direct and/or indirect infringement of the '687 Patent, Nokia Corporation has suffered and continues to suffer injury to its business, property, and patent rights, for which Nokia Corporation is entitled to damages pursuant to 35 U.S.C. § 284 in an amount to be proved at trial.

20. Unless Qualcomm is enjoined by this Court from continuing its infringement of the '687 Patent, Nokia Corporation will suffer additional irreparable harm and impairment of the value of its patent rights for which there is no adequate remedy at law. Thus, Nokia Corporation is entitled to an injunction against further infringement of the '687 Patent pursuant to 35 U.S.C. § 283.

21. Qualcomm's acts of infringement of the '687 Patent have been and continue to be willful, entitling Nokia Corporation to treble damages pursuant to 35 U.S.C. § 284. In addition, Qualcomm's willful infringement qualifies this case as an exceptional case pursuant to 35 U.S.C. § 285.

SECOND COUNTERCLAIM (OF NOKIA CORPORATION)

(INFRINGEMENT OF THE '915 PATENT)

22. Nokia Corporation realleges and incorporates by reference each and every allegation contained in paragraphs 1 through 21 as if fully set forth herein.

23. On information and belief, Qualcomm makes, uses, sells, or offers for sale in the United States, and/or imports into the United States Qualcomm devices, including but not limited to at least one of the following Qualcomm devices: RFR6500, RTR6250, RFT6150, QTP6800 and/or TM7200 that, alone and/or in combination with other devices, directly and/or indirectly infringes and is continuing to infringe, literally and/or under the doctrine of equivalents, the '915 Patent directly or indirectly in violation of 35 U.S.C. § 271.

24. On information and belief, Qualcomm has infringed and is continuing to infringe the '915 Patent by contributing to and/or inducing the infringement by others of claims of the '915 Patent in violation of 35 U.S.C. § 271.

25. As a result of Qualcomm's direct and/or indirect infringement of the '915 Patent, Nokia Corporation has suffered and continues to suffer injury to its business, property,

and patent rights, for which Nokia Corporation is entitled to damages pursuant to 35 U.S.C. § 284 in an amount to be proved at trial.

26. Unless Qualcomm is enjoined by this Court from continuing its infringement of the '915 Patent, Nokia Corporation will suffer additional irreparable harm and impairment of the value of its patent rights for which there is no adequate remedy at law. Thus, Nokia Corporation is entitled to an injunction against further infringement of the '915 Patent pursuant to 35 U.S.C. § 283.

27. Qualcomm's acts of infringement of the '915 Patent have been and continue to be willful, entitling Nokia Corporation to treble damages pursuant to 35 U.S.C. § 284. In addition, Qualcomm's willful infringement qualifies this case as an exceptional case pursuant to 35 U.S.C. § 285.

THIRD COUNTERCLAIM (OF NOKIA CORPORATION)

(INFRINGEMENT OF THE '593 PATENT)

28. Nokia Corporation realleges and incorporates by reference each and every allegation contained in paragraphs 1 through 27 as if fully set forth herein.

29. On information and belief, Qualcomm makes, uses, sells, or offers for sale in the United States, and/or imports into the United States Qualcomm devices, including but not limited to at least one of the following Qualcomm devices: RFR6185, RFR6275, RFR6250, RFR6500, QTP-6800, TM7200 and/or TM6280 that, alone and/or in combination with other devices, directly and/or indirectly infringes and is continuing to infringe, literally and/or under the doctrine of equivalents, the '593 Patent directly or indirectly in violation of 35 U.S.C. § 271.

30. On information and belief, Qualcomm has infringed and is continuing to infringe the '593 Patent by contributing to and/or inducing the infringement by others of the '593 Patent in violation of 35 U.S.C. § 271.

31. As a result of Qualcomm's direct and/or indirect infringement of the '593 Patent, Nokia Corporation has suffered and continues to suffer injury to its business, property, and patent rights, for which Nokia Corporation is entitled to damages pursuant to 35 U.S.C. § 284 in an amount to be proved at trial.

32. Unless Qualcomm is enjoined by this Court from continuing its infringement of the '593 Patent, Nokia Corporation will suffer additional irreparable harm and impairment of the value of its patent rights for which there is no adequate remedy at law. Thus, Nokia Corporation is entitled to an injunction against further infringement of the '593 Patent pursuant to 35 U.S.C. § 283.

33. Qualcomm's acts of infringement of the '593 Patent have been and continue to be willful, entitling Nokia Corporation to treble damages pursuant to 35 U.S.C. § 284. In addition, Qualcomm's willful infringement qualifies this case as an exceptional case pursuant to 35 U.S.C. § 285.

FOURTH COUNTERCLAIM (OF NOKIA CORPORATION)

(INFRINGEMENT OF THE '474 PATENT)

34. Nokia Corporation realleges and incorporates by reference each and every allegation contained in paragraphs 1 through 33 as if fully set forth herein.

35. On information and belief, Qualcomm makes, uses, sells, or offers for sale in the United States, and/or imports into the United States Qualcomm devices, including but not limited to at least one of the following Qualcomm devices: RFR6185, RFR6275, RFR6250, RFR6500, RTR6250, RTR6300, QTP-6800, TM7200 and/or TM6280 that, alone and/or in combination with other devices, directly and/or indirectly infringes and is continuing to infringe, literally and/or under the doctrine of equivalents, the '474 Patent directly or indirectly in violation of 35 U.S.C. § 271.

36. On information and belief, Qualcomm has infringed and is continuing to infringe the '474 Patent by contributing to and/or inducing the infringement by others of the '474 Patent in violation of 35 U.S.C. § 271.

37. As a result of Qualcomm's direct and/or indirect infringement of the '474 Patent, Nokia Corporation has suffered and continues to suffer injury to its business, property, and patent rights, for which Nokia Corporation is entitled to damages pursuant to 35 U.S.C. § 284 in an amount to be proved at trial.

38. Unless Qualcomm is enjoined by this Court from continuing its infringement of the '474 Patent, Nokia Corporation will suffer additional irreparable harm and impairment of the value of its patent rights for which there is no adequate remedy at law. Thus, Nokia Corporation is entitled to an injunction against further infringement of the '474 Patent pursuant to 35 U.S.C. § 283.

39. Qualcomm's acts of infringement of the '474 Patent have been and continue to be willful, entitling Nokia Corporation to treble damages pursuant to 35 U.S.C. § 284. In addition, Qualcomm's willful infringement qualifies this case as an exceptional case pursuant to 35 U.S.C. § 285.

FIFTH COUNTERCLAIM (OF NOKIA CORPORATION)

(INFRINGEMENT OF THE '091 PATENT)

40. Nokia Corporation realleges and incorporates by reference each and every allegation contained in paragraphs 1 through 39 as if fully set forth herein.

41. On information and belief, Qualcomm makes, uses, sells, or offers for sale in the United States, and/or imports into the United States Qualcomm devices, including but not limited to at least one of the following Qualcomm devices: RFR6120, RFR6125, RFR6220, RFR6250, RFR6500, RTR6250, RTR6300, RFT6150, QTP-6800, and/or TM7200 that, alone

and/or in combination with other devices, directly and/or indirectly infringes and is continuing to infringe, literally and/or under the doctrine of equivalents, the '091 Patent directly or indirectly in violation of 35 U.S.C. § 271.

42. On information and belief, Qualcomm has infringed and is continuing to infringe the '091 Patent by contributing to and/or inducing the infringement by others of the '091 Patent in violation of 35 U.S.C. § 271.

43. As a result of Qualcomm's direct and/or indirect infringement of the '091 Patent, Nokia Corporation has suffered and continues to suffer injury to its business, property, and patent rights, for which Nokia Corporation is entitled to damages pursuant to 35 U.S.C. § 284 in an amount to be proved at trial.

44. Unless Qualcomm is enjoined by this Court from continuing its infringement of the '091 Patent, Nokia Corporation will suffer additional irreparable harm and impairment of the value of its patent rights for which there is no adequate remedy at law. Thus, Nokia Corporation is entitled to an injunction against further infringement of the '091 Patent pursuant to 35 U.S.C. § 283.

45. Qualcomm's acts of infringement of the '901 Patent have been and continue to be willful, entitling Nokia Corporation to treble damages pursuant to 35 U.S.C. § 284. In addition, Qualcomm's willful infringement qualifies this case as an exceptional case pursuant to 35 U.S.C. § 285.

SIXTH COUNTERCLAIM (OF NOKIA CORPORATION)

(INFRINGEMENT OF THE '740 PATENT)

46. Nokia Corporation realleges and incorporates by reference each and every allegation contained in paragraphs 1 through 45 as if fully set forth herein.

47. On information and belief, Qualcomm makes, uses, sells, or offers for sale in the United States, and/or imports into the United States Qualcomm devices, including but not limited to at least one of the following Qualcomm devices: QSC1100, QSC6055, QSC6075, QSC6065, MSM6800, CSM6800 and/or QTP-6800, that alone and/or in combination with other devices, directly and/or indirectly infringes and is continuing to infringe, literally and/or under the doctrine of equivalents, the '740 Patent directly or indirectly in violation of 35 U.S.C. § 271.

48. On information and belief, Qualcomm has infringed and is continuing to infringe the '740 Patent by contributing to and/or inducing the infringement by others of the '740 Patent in violation of 35 U.S.C. § 271.

49. As a result of Qualcomm's direct and/or indirect infringement of the '740 Patent, Nokia Corporation has suffered and continues to suffer injury to its business, property, and patent rights, for which Nokia Corporation is entitled to damages pursuant to 35 U.S.C. § 284 in an amount to be proved at trial.

50. Unless Qualcomm is enjoined by this Court from continuing its infringement of the '740 Patent, Nokia Corporation will suffer additional irreparable harm and impairment of the value of its patent rights for which there is no adequate remedy at law. Thus, Nokia Corporation is entitled to an injunction against further infringement of the '740 Patent pursuant to 35 U.S.C. § 283.

51. Qualcomm's acts of infringement of the '740 Patent have been and continue to be willful, entitling Nokia Corporation to treble damages pursuant to 35 U.S.C. § 284. In addition, Qualcomm's willful infringement qualifies this case as an exceptional case pursuant to 35 U.S.C. § 285.

SEVENTH COUNTERCLAIM (OF NOKIA CORPORATION AND NOKIA, INC.)

(DECLARATORY JUDGMENT OF INVALIDITY, NON-INFRINGEMENT, AND UNENFORCEABILITY OF THE '954 AND '130 PATENTS)

52. Nokia Corporation and Nokia, Inc. reallege and incorporate by reference each and every allegation contained in paragraphs 1 through 51 as if fully set forth herein.

53. Qualcomm claims to be the assignee and owner of the entire right, title, and interest in and to United States Patent No. 7,184,954 (the "'954 Patent") and United States Patent No. 6,205,130 (the "'130 Patent") and that the '954 and '130 Patents were duly and lawfully issued. Qualcomm also alleges that Nokia Corporation and Nokia, Inc. are infringing, have infringed, and will continue to infringe the '954 and '130 Patents. These allegations have caused an actual, substantial, and continuing justiciable controversy between Nokia Corporation and Nokia, Inc., on the one hand, and Qualcomm, on the other hand, as to the infringement, validity, and unenforceability of the '954 and '130 Patents. This Court has subject matter jurisdiction over the Counterclaims of Nokia Corporation and Nokia, Inc. under the Declaratory Judgment Act, 28 U.S.C. §§ 2201-2202.

54. Nokia Corporation and Nokia, Inc. deny Qualcomm's allegations of infringement. Neither Nokia Corporation nor Nokia, Inc. have infringed, contributed to the infringement of, induced the infringement of, or otherwise directly, indirectly, or under the doctrine of equivalents, infringed any valid claim of the '954 and '130 Patents.

55. The '954 and '130 Patents are invalid and unenforceable under one or more provisions of 35 U.S.C. §§ 102, 103, and/or 112, and/or are otherwise unenforceable.

56. Nokia Corporation and Nokia, Inc. are therefore entitled to a declaratory judgment that each does not infringe and has not infringed the '954 and '130 Patents and/or that the '954 and '130 Patents are invalid and/or unenforceable.

PRAYER FOR RELIEF

WHEREFORE, Nokia Corporation prays for judgment in its favor and against Qualcomm with respect to Nokia Corporation's counterclaims as follows:

(a) for judgment that Qualcomm has infringed, directly or indirectly, one or more of Nokia's Patents-in-Suit;

(b) awarding damages to Nokia Corporation in an amount to be proved at trial, including prejudgment and post-judgment interest, for Qualcomm's infringement of one or more of Nokia's Patents-in-Suit pursuant to 35 U.S.C. § 284;

(c) awarding treble damages to Nokia Corporation pursuant to 35 U.S.C. § 284 for Qualcomm's willful infringement of one or more of Nokia's Patents-in-Suit;

(d) enjoining Qualcomm, its officers, agents, servants, employees, and those persons acting in active concert or in participation with them, from directly or indirectly further infringing one or more of Nokia's Patents-in-Suit pursuant to 35 U.S.C. § 283; and

WHEREFORE, Nokia Corporation and Nokia, Inc. each pray for judgment in its favor and against Qualcomm with respect to Nokia Corporation's and Nokia, Inc.'s counterclaims as follows:

(e) declaring that Nokia Corporation does not and has not directly or indirectly infringed the '954 and '130 Patents, and that Nokia, Inc. does not and has not directly or indirectly infringed the '954 and '130 Patents;

(f) declaring that each claim of the '954 and '130 Patents is invalid;

(g) declaring that each claim of the '954 and '130 Patents is unenforceable;

(h) declaring this case exceptional pursuant to 35 U.S.C. § 285, and awarding Nokia Corporation and Nokia, Inc. its reasonable attorneys' fees, expenses, and costs incurred in this action; and

(i) granting such other and additional relief as the Court deems just and proper.

DEMAND FOR JURY TRIAL

Pursuant to Rule 38 of the Federal Rules of Civil Procedure, Nokia Corporation and Nokia, Inc. hereby demand a trial by jury as to all issues so triable.

Dated: May 23, 2007	/s/ Allen Arntsen _____ Allen Arntsen FOLEY & LARDNER LLP 150 East Gilman Street Verex Plaza Madison, Wisconsin 53703 Telephone: 608-258-4293 Facsimile: 608-258-4258 G. Peter Albert, Jr. FOLEY & LARDNER LLP 11250 El Camino Real, Suite 200 San Diego, California 92130 Telephone: 858-847-6735 Facsimile: 858-792-6773 Attorneys for Defendants Nokia Corporation and Nokia, Inc.
OF COUNSEL: A. William Urquhart (CA Bar No. 140996) Marshall M. Searcy III (CA Bar No. 169269) Erica P. Taggart (CA Bar No. 215817) Ryan S. Goldstein (CA Bar No. 208444) QUINN EMANUEL URQUHART OLIVER & HEDGES, LLP 865 South Figueroa Street, 10th Floor Los Angeles, California 90017-2543 Telephone: (213) 443-3000 Facsimile: (213) 443-3100 Charles K. Verhoeven (CA Bar No. 170151) QUINN EMANUEL URQUHART OLIVER & HEDGES, LLP 50 California Street, 22nd Floor San Francisco, California 9411 Telephone: (415) 875-6600 Facsimile: (415) 875-6700 Keith E. Broyles (GA Bar No. 090152) Alan L. Whitehurst (DC Bar No. 484873) John D. Haynes (GA Bar No. 340599) ALSTON & BIRD LLP One Atlantic Center 1201 West Peachtree Street Atlanta, Georgia 30309-3424 Telephone: (404) 881-7000 Facsimile: (404) 881-7777 Attorneys for Defendants Nokia Corporation and Nokia, Inc.	

PROOF OF SERVICE

I am employed in the County of Los Angeles, State of California. I am over the age of eighteen years and not a party to the within action; my business address is 865 South Figueroa Street, 10th Floor, Los Angeles, California 90017-2543.

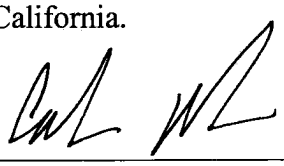
On May 23, 2007, I served true copies of the following document(s) described as **COUNTERCLAIMS OF NOKIA CORPORATION AND NOKIA, INC. AND DEMAND FOR TRIAL BY JURY** on the parties in this action as follows:

SEE ATTACHED LIST

BY ELECTRONIC MAIL TRANSMISSION: By electronic mail transmission from cashrowden@quinnemanuel.com on May 23, 2007, by transmitting a PDF format copy of such document(s) to each such person at the e-mail address listed below their address(es). The document(s) was/were transmitted by electronic transmission and such transmission was reported as complete and without error.

I declare that I am employed in the office of a member of the bar of this Court at whose direction the service was made.

Executed on May 23, 2007, at Los Angeles, California.



Cash Rowden

SERVICE LIST
Qualcomm Incorporated v. Nokia Corporation and Nokia, Inc.
In The United States District Court
For the Western District of Wisconsin
Case No. 07 C 0187 C

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EXHIBIT A

US007031687B2

(12) **United States Patent**
Kivekäs et al.

(10) **Patent No.: US 7,031,687 B2**
(45) **Date of Patent: Apr. 18, 2006**

(54) **BALANCED CIRCUIT ARRANGEMENT AND METHOD FOR LINEARIZING SUCH AN ARRANGEMENT**

(75) Inventors: **Kalle Kivekäs**, Espoo (FI); **Aarno Pärssinen**, Espoo (FI)

(73) Assignee: **Nokia Corporation**, Espoo (FI)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 215 days.

(21) Appl. No.: **10/474,848**

(22) PCT Filed: **Apr. 18, 2001**

(86) PCT No.: **PCT/EP01/04414**

§ 371 (c)(1),
(2), (4) Date: **Oct. 15, 2003**

(87) PCT Pub. No.: **WO02/084859**

PCT Pub. Date: **Oct. 24, 2002**

(65) **Prior Publication Data**

US 2004/0137870 A1 Jul. 15, 2004

(51) **Int. Cl.**
H04B 1/26 (2006.01)

(52) **U.S. Cl.** **455/313**; 455/334; 455/333; 455/226.1; 327/358

(58) **Field of Classification Search** 455/313, 455/323, 333, 326, 334, 317, 226.4, 67.11; 327/356, 357, 358, 359, 113, 355
See application file for complete search history.

(56) **References Cited**

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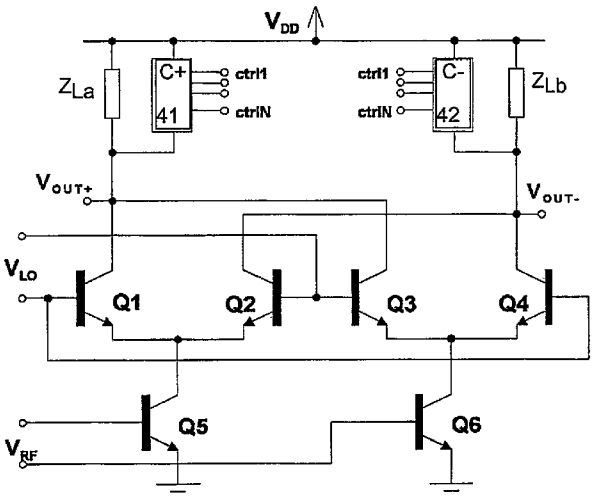
* cited by examiner

Primary Examiner—Lana Le
(74) *Attorney, Agent, or Firm*—Squire, Sanders & Dempsey, L.L.P.

(57) **ABSTRACT**

The present invention relates to a balanced circuit arrangement and methods for linearizing and calibrating such a circuit arrangement wherein linearization is obtained by introducing a load imbalance between the output branches of the balanced circuit arrangement. Thus, a controllable extraneous imbalance is created between the output loads of the balanced circuit arrangement to thereby obtain a linearization by means of even-order non-linearity.

19 Claims, 5 Drawing Sheets



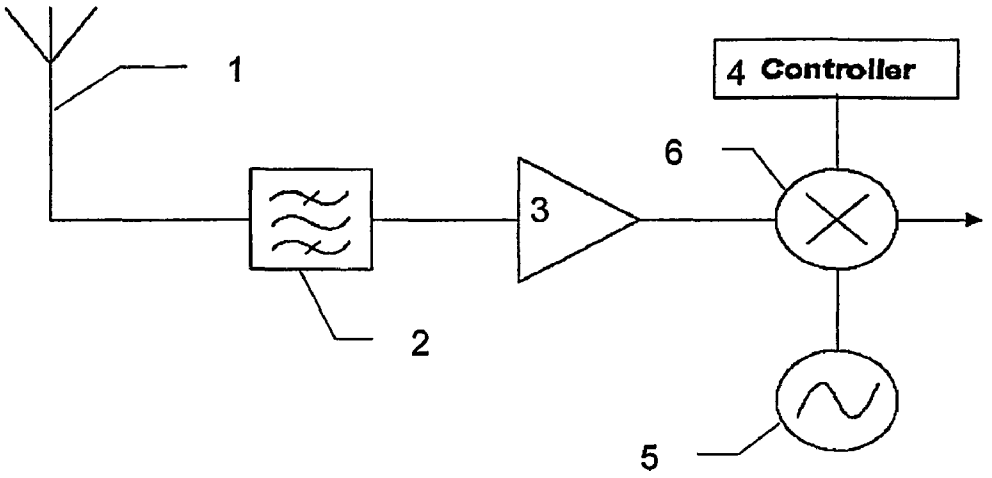

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Fig. 1

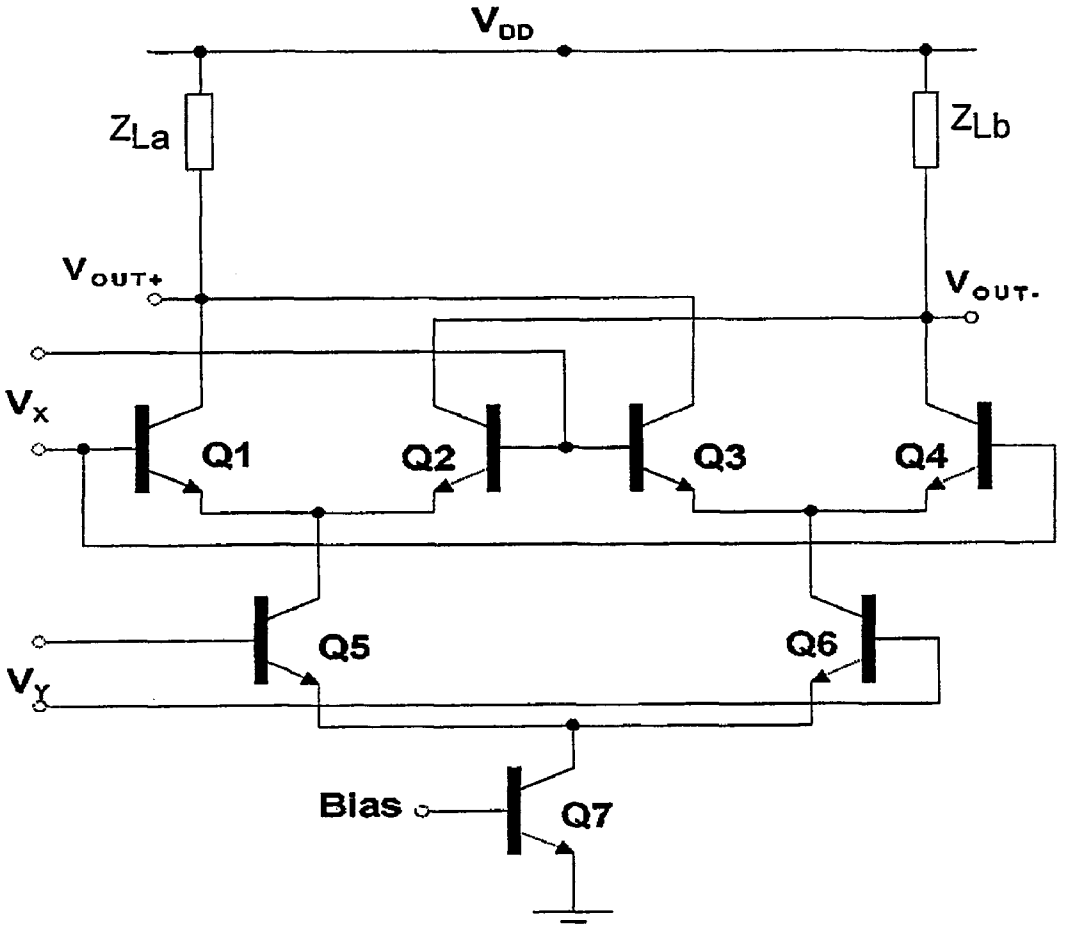
V_{DD}
Z_{La}
Z_{Lb}
V_{OUT+}
V_{OUT-}
V_X
Q1
Q2
Q3
Q4
Q5
Q6
V_Y
Bias
Q7

Fig. 2

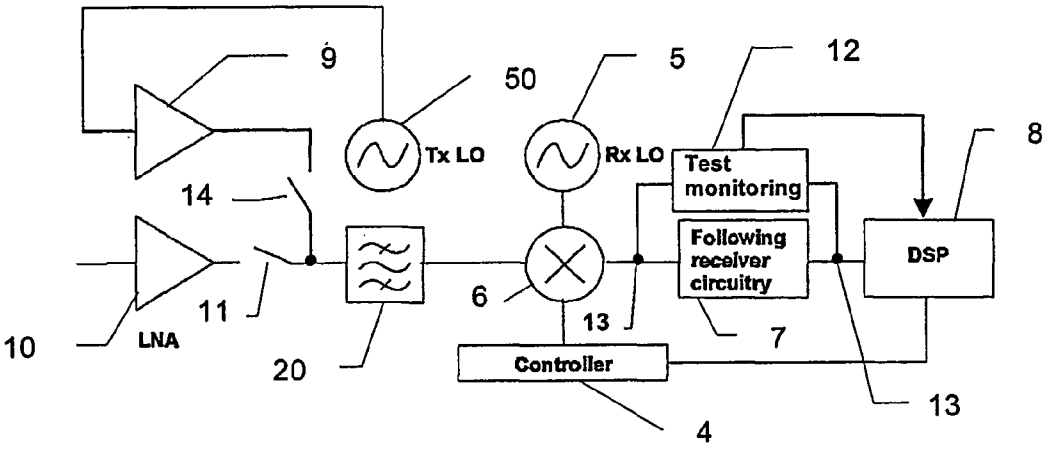
9
50
5
12
8
Tx LO
Rx LO
Test monitoring
14
Following receiver circuitry
DSP
11
6
13
7
10
LNA
20
Controller
13
4

Fig. 3

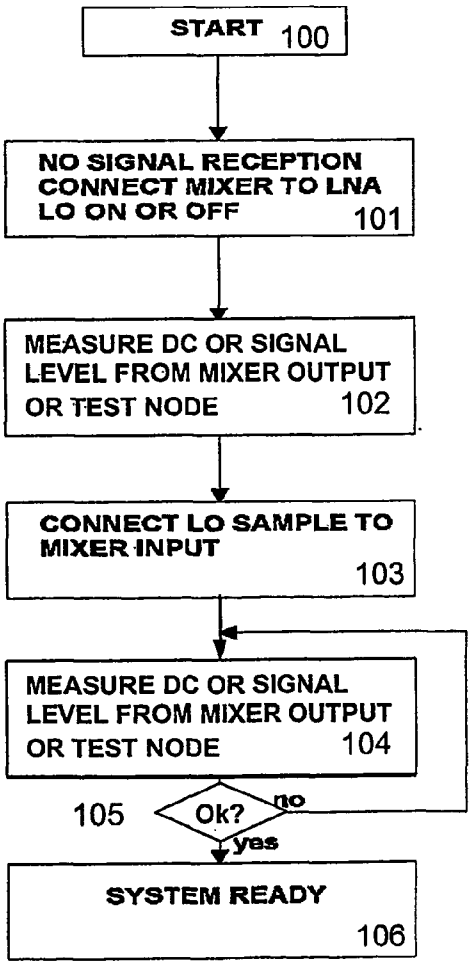
START 100
NO SIGNAL RECEPTION
CONNECT MIXER TO LNA
LO ON OR OFF 101
MEASURE DC OR SIGNAL
LEVEL FROM MIXER OUTPUT
OR TEST NODE 102
CONNECT LO SAMPLE TO
MIXER INPUT 103
MEASURE DC OR SIGNAL
LEVEL FROM MIXER OUTPUT
OR TEST NODE 104
105
Ok?
no
yes
SYSTEM READY 106

Fig. 4

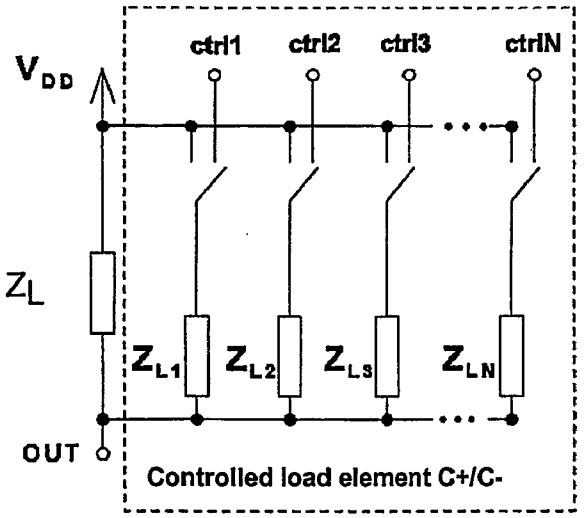
ctrl1
ctrl2
ctrl3
ctrlN
V_{DD}
Z_L
Z_{L1}
Z_{L2}
Z_{LS}
Z_{LN}
OUT
Controlled load element C+/C-

Fig. 5

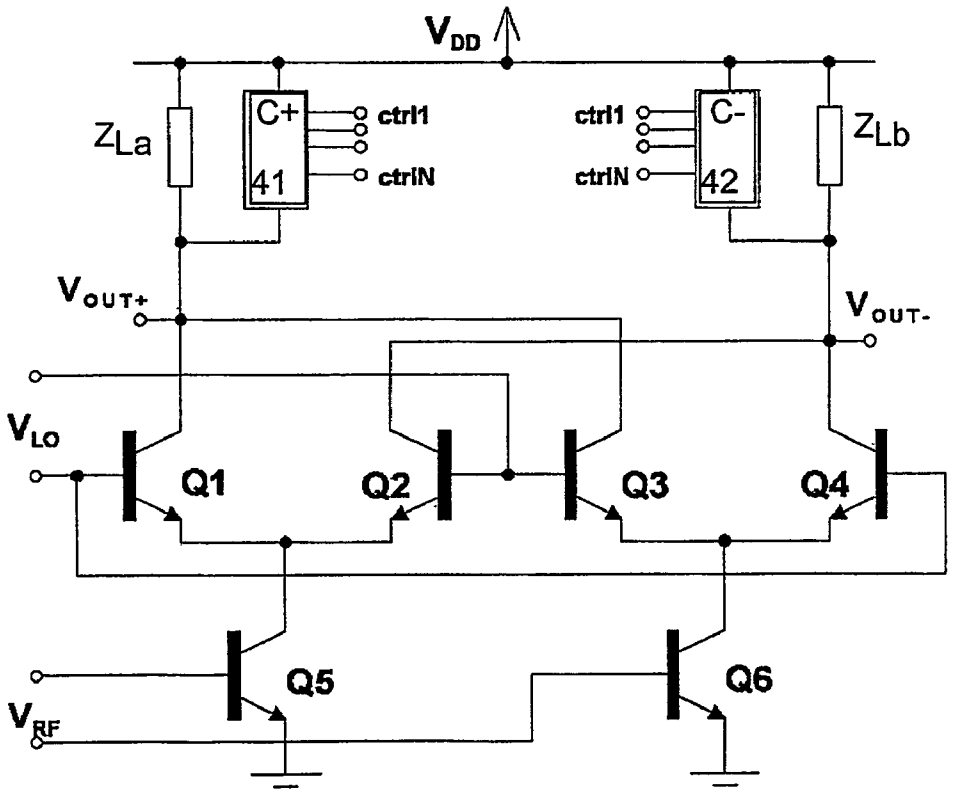
V_{DD}
Z_{La}
C+
41
ctrl1
ctrlN
ctrl1
ctrlN
C-
42
Z_{Lb}
V_{OUT+}
V_{OUT-}
V_{LO}
Q1
Q2
Q3
Q4
Q5
Q6
V_{RF}

Fig. 6

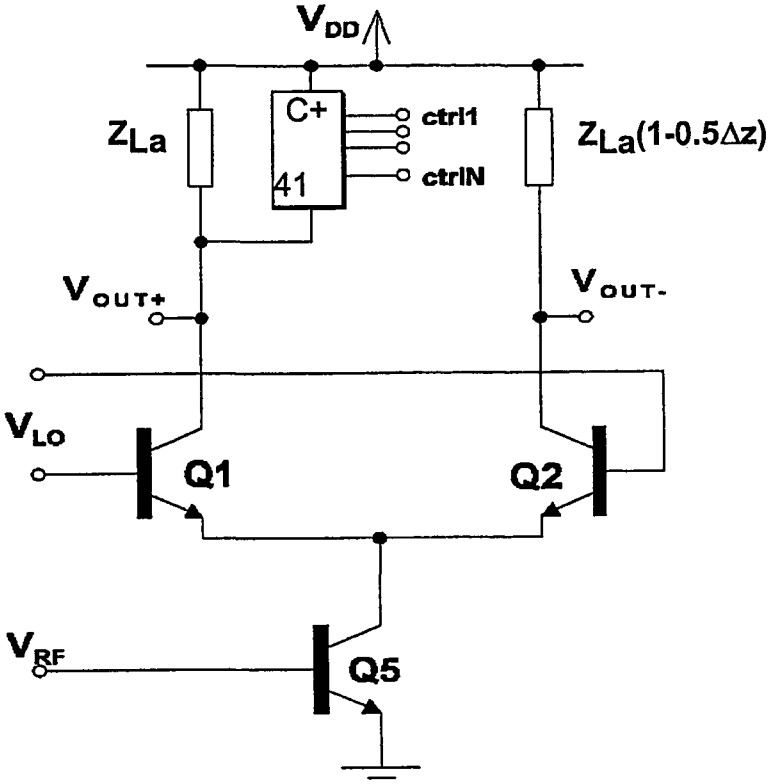
V_{DD}
C+
41
ctrl1
ctrlN
Z_{La}
$Z_{La}(1-0.5\Delta z)$
V_{OUT+}
V_{OUT-}
V_{LO}
Q1
Q2
V_{RF}
Q5

Fig. 7

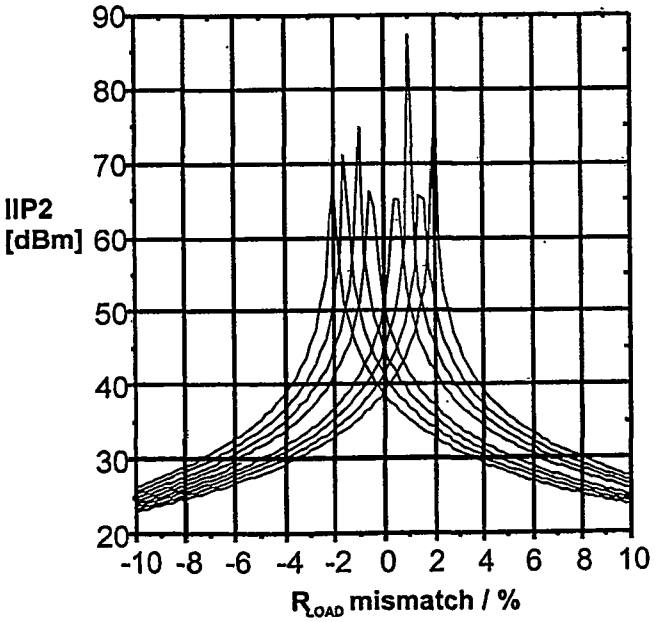
IIP2 [dBm]
90
80
70
60
50
40
30
20
-10 -8 -6 -4 -2 0 2 4 6 8 10
R_{LOAD} mismatch / %

Fig. 8

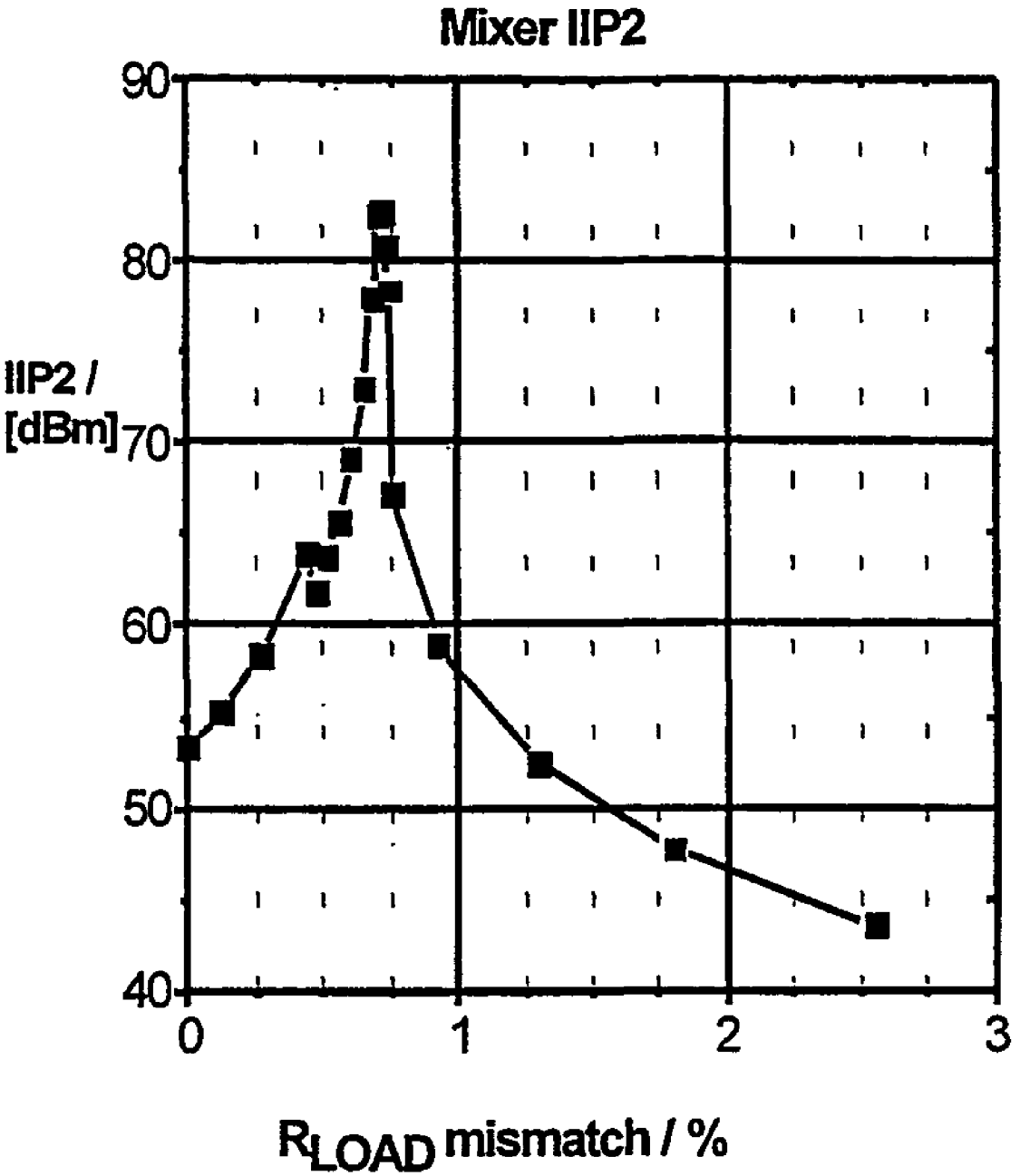

Fig. 9

BALANCED CIRCUIT ARRANGEMENT AND METHOD FOR LINEARIZING SUCH AN ARRANGEMENT

FIELD OF THE INVENTION

The present invention relates to a balanced circuit arrangement such as a balanced or double-balanced amplifier or multiplier and to a method for linearizing such an arrangement e.g. in order to attenuate spurious signals and envelope distortions in radio receivers and transmitters.

BACKGROUND OF THE INVENTION

In radio reception, the linearity of the receiver is an essential requirement. The linearity performance of a receiver, in general, is usually dominated by the down-conversion mixer circuits. Such mixer circuits are used to translate or convert received high frequency signals down to a lower or intermediate frequency (IF). This conversion is achieved by mixing the received signals with a locally generated oscillator signal. By choosing the local oscillator signal to be a constant amount away from a selected or wanted signal in a first frequency band, the selected or wanted signal always appears at the same frequency in the intermediate frequency band. Thereby, selection of the selected or wanted signal may be facilitated by a fixed-tuned IF filter.

In homodyne or direct conversion receivers, the chosen intermediate frequency band is DC or zero frequency. The local oscillator then has a zero frequency separation from the selected or wanted signal. Any modulation on the selected or wanted signal that causes spectral components both above and below the nominal signal frequency becomes folded at the mixer output, as a component below the signal frequency or above the signal frequency will appear at the intermediate frequency above the nominal of zero. To allow for resolution of such folded components, two mixers are provided in a direct conversion receiver using local oscillator signals that are phase offset by 90 degrees. The components above and below the nominal signal frequency then appear folded as a sum signal at one mixer output and a difference signal at the other mixer output where they may be separated if desired. Such direct conversion receiver operations are described in more detail in document U.S. Pat. No. 5,241,702.

However, due to non-linearities, spurious responses will be generated in the direct conversion receiver, the worst being modulation-frequency interference at the receiver's mixer output caused by a strong amplitude-modulated signal of another transceiver. This will appear even if the frequency of the interfering signal considerably deviates from the receiving frequency. These interferences are mainly caused by the second-order distortion component which contains a variable-level DC component proportional to the amplitude of the interference-causing signal. The variable amplitude signal produces at the mixer output a signal which comprises a variable DC component and the frequency of which is identical with the variation of the amplitude. The spurious frequencies may corrupt the radio reception by blocking the following signal processing stages or deteriorating the detection of the desired signal which is overwhelmed by distortion.

The spurious frequencies can be categorized to exist due to the odd- and even-order non-linearities. The even-order mixing results are suppressed by using balanced or double-balanced mixer topologies. Ideally, the even-order spurious frequencies are cancelled in balanced and double-balanced

constructions. However, in practice, the canceling is imperfect. The reason is the imperfect balance due to the mismatch of respective components in the differential branches, i.e. manufacturing tolerances.

In radio receivers utilizing a direct conversion architecture or a significantly low IF, the spurious signals cannot be removed by selecting an optimal IF. Due to the existence of the even-order distortions and imbalance in the circuitry, a variable DC component proportional to the signal level and amplitude modulation depth of the interfering signal occurs. Moreover, envelope distortions are detected, the amplitude of which is also proportional to the amplitude modulation depth of the interfering signal, and the frequency of which equals to the variation of the amplitude. Thus, not only a DC offset but also a low frequency disturbance may be generated to corrupt the desired reception band. This is a particular concern in down-conversion mixers of direct conversion receivers.

Several solutions for reducing distortions in radio receivers with low IF have been proposed. Document U.S. Pat. No. 5,749,051 suggests compensating unwanted terms caused by second-order intermodulation by feeding instantaneous power measurements to a signal processing unit along with the complex baseband signals. The signal processing unit then determines a complex compensation coefficient by correlating the power signal with the complex baseband signals. The complex compensation co-efficient is then employed to subtract a weighted amount of the power signal from the complex baseband signal in order to cancel the unwanted second-order intermodulation distortion terms. Furthermore, document EP 0 951 138 discloses a method for attenuating spurious signals in mixer circuits by setting variable-level bias voltages and/or currents to transistors in the mixer circuits. Additionally, document GB 2 346 777 suggests switching a DC offset correction in or out of the circuitry according to the received signal strength or signal-to-noise ratio.

Furthermore, the use of a dynamic matching procedure is described by E. Bautista et al., "Improved Mixer IIP2 through Dynamic Matching", in the Digest of ISSCC 2000, pp. 376-377. According to this procedure, any undesirable second-order intermodulation distortion product generated in the mixer circuit is modulated to a frequency where it can easily be filtered off. This can be achieved by applying a periodic signal to input switches of the mixer circuit in order to modulate the received input signal. If the periodic signal is replaced by a pseudo-random signal, the undesirable second-order intermodulation distortion products can be spread over a wide range of frequencies to achieve a desired second-order input intercept point (IIP2) performance.

The second-order distortion phenomena itself and its undesired products, i.e. DC offset and envelope distortions, have not been thoroughly investigated so far. Due to lack of proper analysis of this topic, most of the solutions have been focused on the removal of the DC offset. However, even if the DC offset at the output of the mixer circuit is reduced to zero, the circuit may still be in an imbalanced condition, due to the fact that the envelope distortion itself causes a DC term which is related to other DC offsets in a complex manner.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a balanced circuit arrangement and method for linearizing

such an arrangement, by means of which spurious signals and envelope distortions in radio receivers and transmitters can be reduced.

This object is achieved by a balanced circuit arrangement comprising: first transistor means coupled via first load means to a power source; second transistor means coupled via second load means to said power source; and linearity control means for linearizing the balanced circuit arrangement by adjusting the first and second load means into a load imbalance.

Furthermore, the above object is achieved by a method for linearizing a balanced circuit arrangement, comprising the steps of:

providing a controllable load means in at least one output branch of the balanced circuit arrangement; and

adjusting the load of the controllable load means to obtain a linearizing load imbalance in the output branches of the balanced circuit arrangement.

Additionally, the above object is achieved by a method for calibrating a balanced circuit arrangement, comprising the steps of:

measuring a DC output level or a lowpass filtered signal level of said balanced circuit arrangement when no input signal is applied or when input signal changes have only a weak effect on the measured signal;

supplying a test signal to the input of said balanced circuit arrangement and measuring the DC output level;

determining a difference between said measured DC levels; and

adjusting a load means in at least one output branch of said balanced circuit arrangement until said determined difference is minimized.

The input signal can be either connected or disconnected from the mixer input. In the former case, it should be assumed that the average level of the AM distortion in the input signal varies only a little during the calibration.

Accordingly, envelope distortions and even-order spurious signals are controlled by controlling or changing DC offset balance errors in the balanced circuit arrangement. The balance errors occur due to the mismatch of components, i.e. component manufacturing tolerances. Thereby, the balanced circuit arrangement can be linearized in terms of even-order non-linearity by introducing a controlled imbalance in the load of the balanced circuit arrangement. In particular, the invention can be applied to any balanced circuit arrangement in radio receivers and/or transmitters requiring even-order linearity, such as in mobile communications devices.

Thus, the second-order input intercept point (IIP2) can be maximized by adjusting the loads of balanced circuit arrangement into a slight imbalance. This can be achieved by creating a controllable extraneous imbalance between the output loads of the balanced circuit arrangement. According to the measurements and simulations, the IIP2 performance of the balanced circuit arrangement can be enhanced up to 30 dB. The imbalance in the DC voltage or lowpass filtered and averaged signal, generated between the output branches can then be cancelled at a later stage after the signals causing envelope or other distortions have been filtered out. The effect on other significant performance parameters is negligible due to the fact that the required artificial mismatch is relatively small compared to the absolute values of the load components.

According to an advantageous development, the linearity control means may be arranged to perform the adjustment by selectively switching load elements to at least one of the first and second load means. Preferably, the load elements may be weighted load elements. Thereby, the amount of load imbalance may easily be controlled by a switching control function based on corresponding control inputs. In case of a use of weighted load elements, a control based on binary control words can be implemented. Thus, the linearity control means may comprise at least one input terminal for inputting a control signal.

The balanced circuit arrangement may be a single- or double-balanced circuit arrangement. In general, the present invention is applicable to any mixer circuit comprising a balanced circuit arrangement, e.g. a Gilbert-cell multiplier. Furthermore, the present invention may be applied to any modulator and/or demodulator circuit, such as an IQ modulator and/or demodulator, or to any receiver and/or transmitter circuit comprising e.g. a direct conversion receiver, in which a balanced circuit arrangement can be used.

According to another advantageous development, the adjusting step may be performed by selectively switching load elements of the controllable load means.

Furthermore, the adjusting step of the calibrating method may be an iterative step and the difference may be monitored by an analog or by a digital signal processing routine.

BRIEF DESCRIPTION OF THE DRAWINGS

In the following, the present invention will be described in greater detail based on preferred embodiments with reference to the accompanying drawings, in which:

FIG. **1** shows a schematic block diagram of a receiver in which the present invention can be applied;

FIG. **2** shows a circuit diagram of a Gilbert-cell multiplier as an example for a balanced circuit arrangement in which the present invention can be applied;

FIG. **3** shows a schematic block diagram of a calibration technique according to a preferred embodiment of the present invention;

FIG. **4** shows a flow diagram of a calibration procedure according to the preferred embodiment of the present invention;

FIG. **5** shows a circuit diagram of a load controller which can be used in the preferred embodiment;

FIG. **6** shows a double-balanced mixer as a preferred embodiment of a doublebalanced circuit arrangement;

FIG. **7** shows a circuit diagram of a single-balanced mixer as a preferred embodiment of a single-balanced circuit arrangement;

FIG. **8** shows simulated IIP2 performance characteristics for different fixed imbalances between the output branches; and

FIG. **9** shows a measured trimming performance of an implemented integrated direct conversion receiver.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The present invention will now be described on the basis of a single-balanced and double-balanced mixer circuit, as an examples for a balanced circuit arrangement according to the present invention, which may be used in a direct conversion receiver for WCDMA (Wideband Code Division Multiple Access) base station applications in 3rd generation mobile communication networks.

FIG. **1** shows a block diagram of those parts of the receiver which are essential to the present invention. The receiver comprises an antenna **1** from which a signal is received and filtered by a bandpass filter **2** and amplified by an amplifier **3**. The amplified signal at the radio reception

frequency is then mixed to the (zero) intermediate frequency in a balanced mixer **6** according to the preferred embodiments of the present invention. A local oscillator **5** feeds a predetermined frequency to the mixer **6**, such that the radio reception frequency is mixed with the determined frequency of the local oscillator **5** to obtained the (zero) intermediate frequency. The linearity of the mixer **6** is controlled by a controller **4** by adjusting the load imbalance between the output branches of the mixer **6**.

FIG. **2** shows a known Gilbert-cell used as a balanced circuit arrangement in amplifiers, multipliers and mixers, such as the mixer **6** of FIG. **1**. In the Gilbert-cell, two input voltages V_X and V_Y are multiplied into one output voltage V_{OUT}, i.e. the voltage difference at the outputs V_{OUT+} and V_{OUT-} corresponds to the product or multiplication of the input voltages. The first input voltage V_X is applied between the base terminals of transistors Q**1**, Q**2** and Q**3**, Q**4**, respectively. The second input voltage V_Y is amplified by transistors Q**5** and Q**6**. The transistors Q**5** and Q**6** are connected at their emitter terminals to a transistor Q**7** which is controlled by a bias voltage and coupled to known potential. The output branches of the circuit are coupled to a positive operating voltage through load impedances Z_{La} and Z_{Lb}. The transistors Q**1** and Q**4** amplify the first input voltage V_X in a first polarity direction, and the transistors Q**2** and Q**3** amplify the first input voltage V_X in a second polarity direction opposite to the first polarity direction. The amplified voltages are coupled and cross-coupled, respectively, to the outputs V_{OUT+} and V_{OUT-}.

According to the present invention, the load values of the load impedances Z_{La} and/or Z_{Lb} are controlled by the controller **4** so as to introduced a load imbalance required to maximize the IIP2 performance of the multiplier or mixer circuit. It is noted that the load impedances Z_{La} and Z_{Lb} may be any load means or circuitry which provides a mechanism for adjusting the effective load value introduced into the respective output branch. Thereby, the IIP2 performance of the mixer circuit can be improved, since the DC and low-frequency effects of the envelope distortions can be compensated by the introduced load imbalance.

In general, any transceiver, receiver or transmitter circuit can be calibrated by properly adjusting the load imbalance of an included balanced circuit arrangement. A corresponding calibration method is described in the following.

FIG. **3** shows an arrangement by means of which the calibration technique can be implemented. In particular, FIG. **3** shows a direct conversion receiver arrangement comprising a low noise amplifier (LNA) **10** which is connected to an antenna (not shown) for receiving radio frequency signals. A received radio frequency signal is supplied to a bandpass filter **20** (optional) via a switching element or switch **11**. The "bandpass" filter can be a simple ac-coupling device as well. Input signal can be also switched on and off by biasing of the preceding LNA **10**, instead of switch **11**. After the received signal has been filtered in the bandpass filter **20**, it is supplied to the mixer **6**, where it is mixed with a receiving local oscillator (Rx LO) **5** of a predetermined frequency related to the radio reception frequency. The signal converted to the IF or zero frequency is supplied to a following receiver circuitry **7**, comprising a test monitoring circuitry **12**, where the signal is detected at one of the test nodes **13** and distortions are extracted to obtain a measurement for the second-order non-linearity performance (i.e. IIP2 performance) of the receiving or mixer circuitry. A control signal corresponding to the IIP2 performance is supplied by the test monitoring circuitry **12** to a digital signal processor (DSP) **8** which evaluates the performance and supplies a corresponding control signal or control information to the controller **4** arranged to control the load imbalance in the output branches of the mixer **6**. The procedure can be done independently in both inphase (I) and quadrature (Q) branches, e.g., in a direct conversion receiver. However, only one signal and one control path is drawn in FIG. **3**.

To obtain a reference or test signal, a transmission local oscillator (Tx LO) **50** is connected via an amplifier circuit **9** and a second switching element **14** to the input of the mixer **6**. Thus, either a received radio signal or the generated test signal or both can be switched to the bandpass filter **20**. The test signal can be any locally or externally generated signal.

FIG. **4** shows a flow diagram of a calibration method according to a preferred embodiment. This calibration method is used to adjust or set the load values in the output branches of the mixer **6** by the controller **4** in order to obtain a maximum linearization of the mixer **6** by the means of even-order linearity. This calibration method can be used to calibrate the receiver circuit during a stand-by period or during relatively stable reception conditions, i.e. when input signal changes have only a weak effect on the measured signal.

After the start of the method in step S**100**, the switching element **11** is closed to connect the LNA **10** while no input signal is supplied to the mixer **6**. In step S**101**, it may be considered or checked whether the receiving local oscillator **5** is switched on or off, since this may lead to different measuring results. Then, the output DC or lowpass filtered signal level of the mixer **6** is measured in step S**102** by the test monitoring circuitry **12** at the respective one of the test nodes **13** and the measuring result is supplied to the DSP **8** where it may be stored. In step S**103**, the second switching element **14** is closed to connect to the output terminal of the amplifier circuit **9** so as to supply a sample of the test signal, e.g. the signal from the transmission local oscillator **50** in a receiver calibration, to the mixer **6**, wherein the amplifier circuit **9** is arranged to provide an interface equivalent to that of the LNA **10**. Alternatively, an attenuated test signal can be connected directly to the input of the LNA **10**, while the second switching element **14** remains open or can be dispensed with. Due to the second-order non-linearity and imbalance in the mixer **6**, a DC error voltage is generated at the output of the mixer **6**. This DC error is proportional to the amplitude of the even-order spurious signal, and is measured and may be stored in the DSP **8**.

Based on the measured DC outputs, the DSP **8** provides a control to the controller **4** so as to adjust the load imbalance and thereby minimize the increment or increase in the DC voltage or in the lowpass filtered output signal at the output of the mixer **6** due to the DC error. Thus, the receiver circuit can be linearized by this DC level set control. According to FIG. **4**, the calibration process may be an iterative process and the DC error can be monitored by the routines of the DSP **8** e.g. via A/D converters (not shown). After each iteration, a check is performed in step **105** as to whether a satisfactory result has been achieved, i.e. whether the circuit has been linearized to a sufficient extent. If not, step **104** is repeated. When a satisfactory result is determined in step **105**, the flow proceeds to step **106** where the user or a system is informed of the system ready state.

Thus, an automatically controlled calibration of receiver, transmitter or transceiver circuits can be provided.

FIG. **5** shows a controllable adjustment block or circuitry for controlling the load value of the load elements Z_{La}. The same adjustment circuitry may be provided at the other load element Z_{Lb}. According to FIG. **5**, the load adjustment or

control arrangement comprises a plurality of load elements Z_{L1} to Z_{Ln} which can be switched to be connected in parallel to the load element Z_{La} so as to decrease or increase the total load based on binary control signals provided to the control terminals ctrl**1** to ctrlN. As an example, a logical signal "1" may be used to close the respective switch and to connect the respective load element in parallel to the load element Z_{La}. Thus, the load value generated by the load adjustment circuitry corresponds to the binary digits of the binary control word applied to the control terminals ctrl**1** to ctrln.

The load elements Z_{L1} to Z_{Ln} may be arranged to provide weighted loads i.e. their load values may be generated by multiplying a basic load value with an integer number. As an example, the load value of an individual load element may be generated based on the following equation:

$$Z_{Li}=2^{(i-1)}\cdot k\cdot Z_L$$

wherein Z_L denotes a basic load value or unit load value, and k denotes an integer (1 . . . n) selected according to the desired tuning range. Due to the fact that the above equation corresponds to the weighting of a dual number system, a direct relation between the binary control word applied to the control terminals ctrl**1** to ctrlN and the generated load value can be obtained, while the control terminal ctrl**1** corresponds to the most significant bit (MSB) and the control terminal ctrlN corresponds to the least significant bit (LSB). The adjustment circuitry comprises weighted fingers of load elements connected in parallel to a basic or original load. Each finger can be selected using the respective switch. Thus, in case resistor loads are used, the control terminal ctrlN connects the largest parallel resistor finger in parallel to the basic load Z_L to thereby obtain a minimum load change. The resolution of the load adjustment control can be selected to achieve a desirable range, e.g. the resolution may be 0.1%. As determined on the basis of simulations and measurements, the total tuning range should preferably cover a range of ±5% of the basic or original load value.

In complex receiver, transmitter or transceiver arrangements, each mixer, modulator or other balanced circuit arrangement can be adjusted separately. The calibration sequence may include counting of digital codes for adjusting the load imbalance, wherein measurements are swapped until the accepted level is reached.

FIG. **6** shows a double-balanced multiplier mixer circuit similar to the Gilbert-cell shown in FIG. **2**, wherein the bias adjusting transistor Q**7** has been removed. Nevertheless, the circuitry of FIG. **6** may as well include the bias adjusting transistor Q**7**.

According to the embodiment of FIG. **6**, both loads Z_{La} and Z_{Lb} can be adjusted by respective load adjustment circuits C+ **41** and C− **42** respectively, connected in parallel to the respective load in the respective output branch. Thus, an individual or branch-selective load adjustment can be performed by the controller **4**. Both load adjustment circuits **41** and **42** may be arranged as shown in FIG. **5**.

As can be gathered from FIG. **6**, a local oscillator voltage V_{LO} generated by the receiving local oscillator **5** is applied between the base terminals of the transistors Q**1** and Q**2** and between the base terminals of transistors Q**3** and Q**4**, while a radio reception frequency voltage V_{RF} obtained from the LNA **10** is supplied between the base terminals of the transistors Q**5** and Q**6**. Thereby, the output voltage V_{OUT} between the collector terminals of the transistors Q**1** and Q**3** and the transistors Q**2** and Q**4** corresponds to a multiplication of the local oscillator voltage V_{LO} and the radio reception frequency voltage V_{RF}. The load value can be trimmed in both output branches to obtain a desired load imbalance.

FIG. **7** shows an embodiment of a single-balanced mixer or multiplier circuit, where the load of only one output branch can be adjusted by the controller **4**. In particular, a load adjustment or control circuit C+ **41** is connected in parallel to the load Z_{La} of one output branch. Thus, load trimming is performed in one output branch. In this case, the load value of the other load Z_{Lb} should be selected according to the following equation:

$$Z_{Lb}=Z_{La}\cdot(1-0.5\ \Delta z),$$

wherein Δz indicates the tuning range of the load adjustment circuit **41** in percentages relative to the actual load. Thereby, an adjustment of the load imbalance is possible by the same amount in both directions.

It is noted that both single-balanced and double-balanced mixers can be linearized by trimming in either both output branches or one of the branches

FIG. **8** shows characteristics of a simulated IIP2 performance of a mixer circuit versus the mismatch in the load values or resistances, achieved by the load adjustment circuits **41** and/or **42**. The different characteristics have been obtained for different fixed imbalances in the mixer circuit. The behavior is similar and repeatable for both single-balanced and double-balanced mixer circuits or other balanced circuit arrangements. As can be gathered from FIG. **8**, depending on the initial fixed imbalances, which may be the result of component mismatches, the performance peaks of the IIP2 performance are located at different percentual load mismatch values. Thus, if the corresponding load mismatch value is introduced into the mixer circuit, an optimized IIP2 performance can be achieved.

FIG. **9** shows a measured trimming performance of an implemented integrated direct conversion receiver. According to FIG. **9**, the measuring results correspond to the simulated characteristics shown in FIG. **8**. In particular, a sharp peak in the IIP2 performance of the direct conversion receiver is obtained at a load mismatch of approximately 0.7%. Thus, the iterative calibration procedure will lead to a load adjustment to achieve this optimal load mismatch.

It is noted that the present invention is not restricted to the concrete circuit arrangements described in the preferred embodiments. The load adjustment may be performed by any control means or elements which are suitable to change or control load values in at least one of the respective output branches. In particular, the load adjustment may be realized by active elements such as bipolar or unipolar transistors, diodes or other semiconductor elements. Furthermore, the balanced circuit arrangement may be provided in IQ modulators, multi-carrier or multi-frequency receiver and/or transmitter systems. Furthermore, the calibration signals used for adjusting the load adjustment circuit can be obtained by using modulated carriers to allow for a greater flexibility of calibration. The measuring of the DC level or the lowpass filtered test signal may be performed solely by the DSP **8**, such that the test monitoring circuitry **12** can be dispensed with. The above preferred embodiments may thus vary within the scope of the attached claims.

The invention claimed is:

1. A balanced circuit arrangement comprising:

a) first transistor means coupled via first load means to a power source;

b) second transistor means coupled via second load means to said power source; and

c) linearity control means for linearizing said balanced circuit arrangement by adjusting said first and second load means into a load imbalance.

2. A circuit arrangement according to claim **1**, wherein said linearity control means are arranged to perform said adjustment by selectively switching load elements to at least one of said first and second load means.

3. A circuit arrangement according to claim **2**, wherein said load elements are weighted load elements.

4. A circuit arrangement according to claim **1**, wherein said linearity control mean comprise at least one input terminal for inputting a control signal.

5. A circuit arrangement according to claim **1**, wherein said balanced circuit arrangement is a double-balanced circuit arrangement.

6. A mixer circuit comprising a balanced circuit arrangement as claimed in claim **1**.

7. A mixer circuit according to claim **6**, wherein said mixer circuit is a Gilbert-cell multiplier.

8. A modulator and/or demodulator circuit comprising a balanced circuit arrangement as claimed in claim **1**.

9. A modulator and/or demodulator circuit according to claim **8**, wherein said modulator and/or demodulator circuit is an IQ modulator and/or demodulator.

10. A receiver and/or transmitter circuit comprising a balanced circuit arrangement as claimed in claim **1**.

11. A receiver and/or transmitter circuit according to claim **10**, wherein said receiver and/or transmitter circuit comprises a direct conversion receiver.

12. A method for linearizing a balanced circuit arrangement, comprising the steps of:

a) providing a controllable load means in at least one output branch of said balanced circuit arrangement; and

b) adjusting the load of said controllable load means to obtain a linearizing load imbalance in the output branches of said balanced circuit arrangement.

13. A method according to claim **12**, further comprising the step of canceling a DC voltage or lowpass filtered and averaged signal imbalance between said output branches after other distortion signals have been filtered out.

14. A method according to claim **12**, wherein said adjustment step is performed by selectively switching load elements of said controllable load means.

15. A method according to claim **14**, further comprising the step of providing said load elements with weighted load values.

16. A method for calibrating a balanced circuit arrangement, comprising the steps of:

a) measuring a DC output level or lowpass filtered level of said balanced circuit arrangement when no input signal is applied or when input signal changes have only a weak effect on the measured signal;

b) supplying a test signal to the input of said balanced circuit arrangement and measuring the DC output level;

c) determining a difference between said measured DC levels; and

d) adjusting a load means in at least one output branch of said balanced circuit arrangement until said determined difference is minimized.

17. A method according to claim **16**, wherein said adjusting step is an iterative step and said difference is monitored by a digital signal processing routine.

18. A method according to claim **16**, wherein said adjusting step is performed by selectively switching load elements of said load means.

19. A method according to claim **16**, wherein said calibrating method is used to calibrate a mixer circuit or modulator of a direct conversion receiver.

* * * * *

EXHIBIT B

US007151915B2

(12) **United States Patent**
Heinonen et al.

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(45) **Date of Patent: Dec. 19, 2006**

(54) **DUAL MODE VOLTAGE CONTROLLED OSCILLATOR HAVING CONTROLLABLE BIAS MODES AND POWER CONSUMPTION**

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H04B 1/06 (2006.01)

(52) **U.S. Cl.** **455/255**; 455/265; 455/76

(58) **Field of Classification Search** 455/265, 455/76, 112, 180.3, 183.1, 188.2, 147, 255, 455/264; 331/2, 34, 17, 18
See application file for complete search history.

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2001/0029172	A1 *	10/2001	Lee et al.	455/234.1

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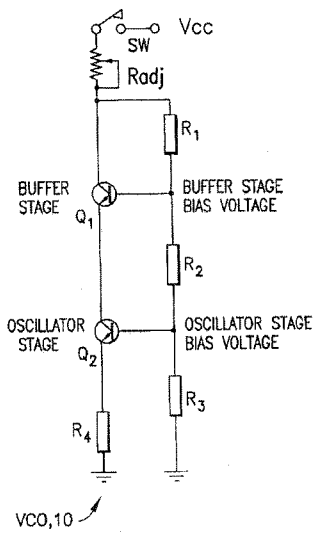
(57) **ABSTRACT**

Disclosed is an oscillator circuit (**10**) for use in a local oscillator of an RF communications device (**100**) that communicates over an RF channel. The oscillator circuit includes an oscillator transistor coupled to a power supply voltage (Vcc) through a buffer transistor, and a biasing network having bias voltage outputs coupled to a control input of the oscillator transistor and to a control input of the buffer transistor. In one embodiment the bias voltage network is coupled to Vcc, while in another embodiment the bias voltage network is coupled to a separate voltage (Vbias). Circuitry is provided for setting a magnitude of Vcc and/or Vbias as a function of at least one of RF channel conditions, such as channels conditions determined from a calculation of the (SNR), or an operational mode of the RF communications device. The magnitude of Vcc (and Vbias) may be set between about zero volts (i.e., turned off) and some maximum value. The operational mode can be, for example, one of a TDMA, burst-type narrow bandwidth mode, or a CDMA, substantially continuous, wider bandwidth mode. The value of Vcc and/or Vbias maybe set so as to minimize power consumption as a function of an amount of allowable local oscillator phase noise. A broad bandwidth/narrow bandwidth dual mode RF transceiver in accordance with these teachings includes at least one phase locked loop (PLL) that includes a voltage controlled oscillator (VCO) providing a local oscillator signal for at least one of an I/Q modulator or an I/Q demodulator; a processor responsive to an output of said I/Q demodulator for determining at least one aspect of RF channel quality; and circuitry coupled between the processor and the VCO for minimizing at least VCO power consumption as a function of an amount of allowable VCO phase noise for a current RF channel quality.

19 Claims, 7 Drawing Sheets



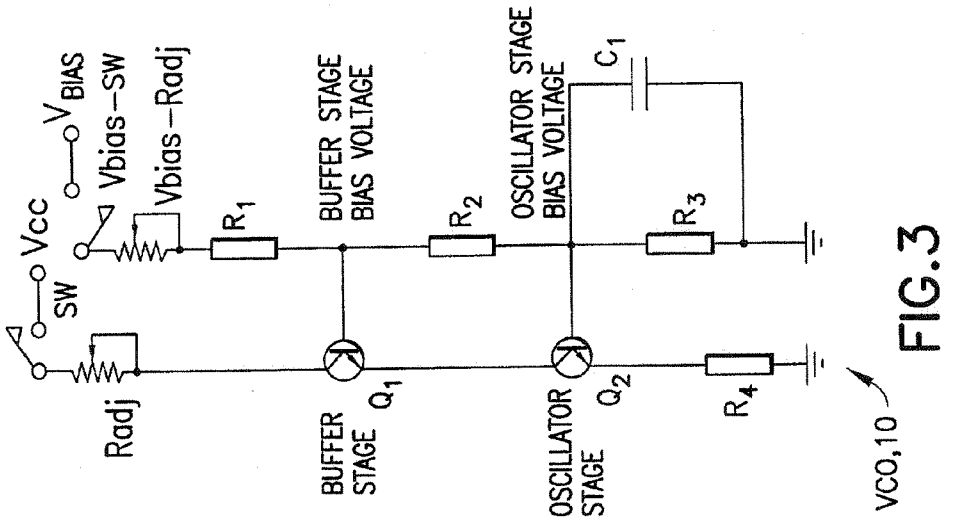


FIG.3

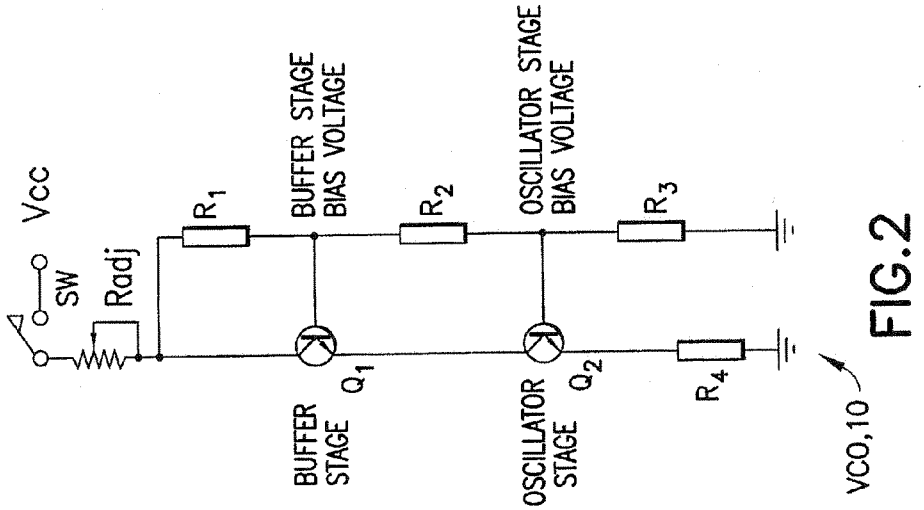


FIG.2

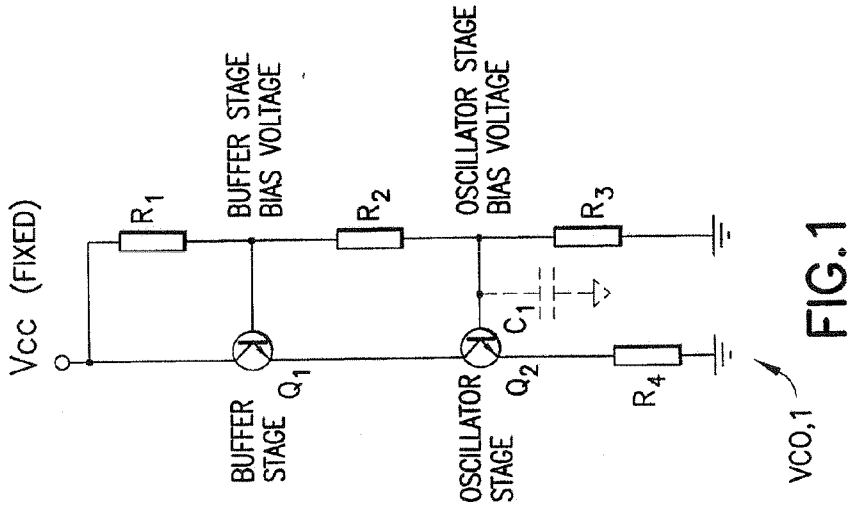


FIG.1
PRIOR ART

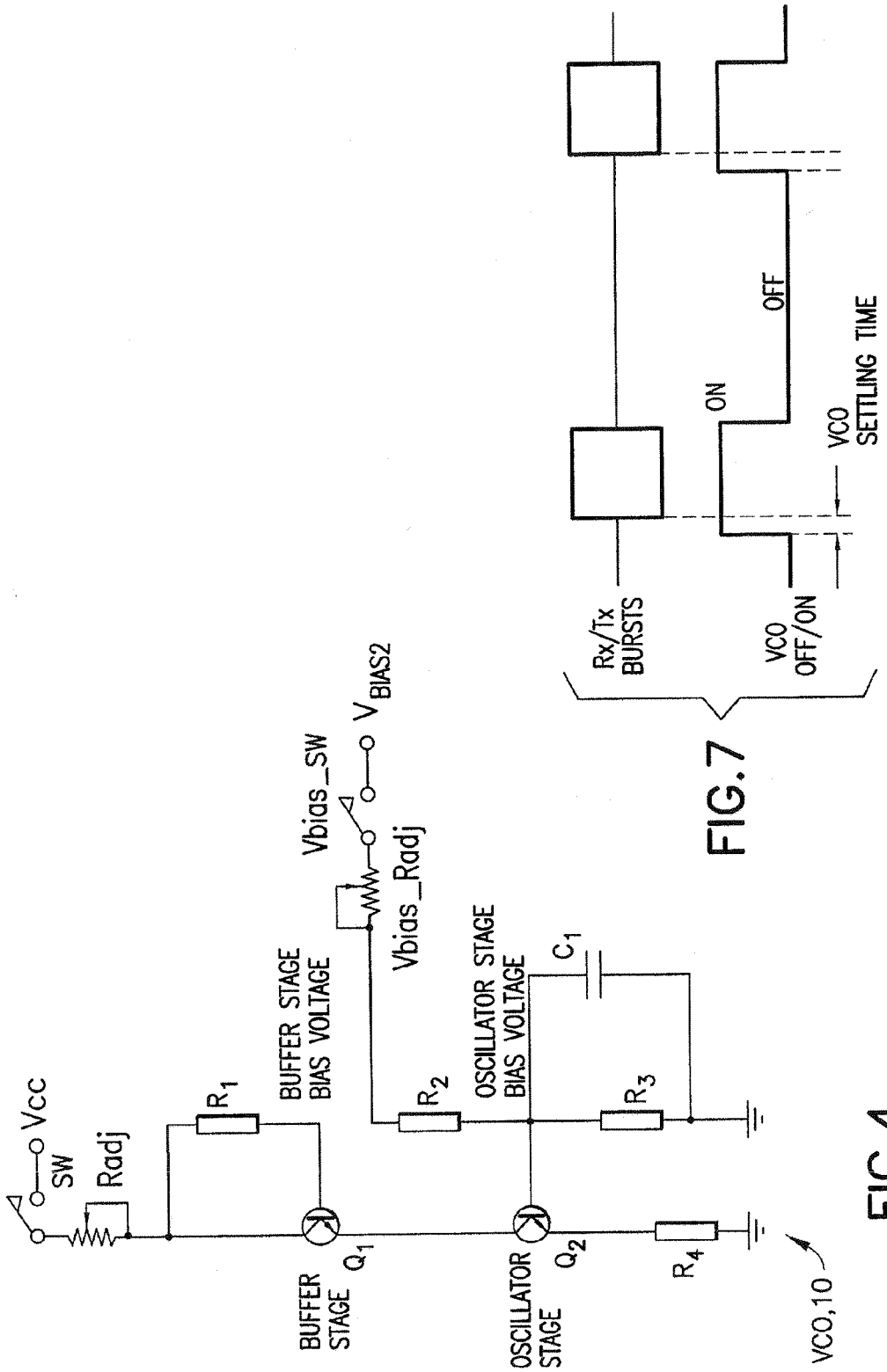

Vcc
SW
Radj
R1
BUFFER STAGE BIAS VOLTAGE
Vbias_SW
V BIAS2
Vbias_Radj
R2
OSCILLATOR STAGE BIAS VOLTAGE
C1
R3
BUFFER STAGE
Q1
OSCILLATOR STAGE
Q2
R4
VCO,10

FIG.4

Rx/Tx BURSTS
VCO OFF/ON
ON
OFF
VCO SETTLING TIME

FIG.7

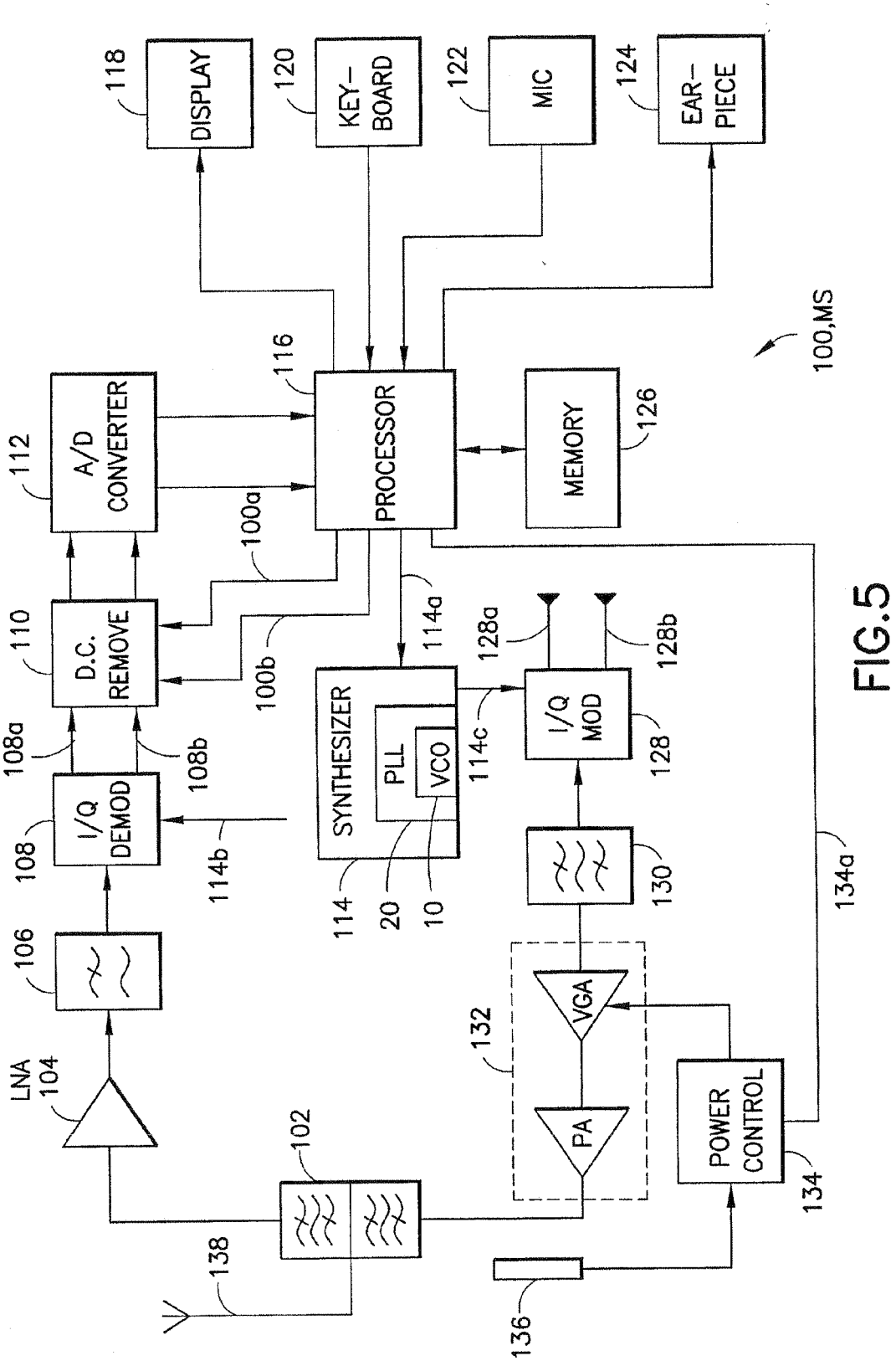

118
DISPLAY
120
KEY-BOARD
122
MIC
124
EAR-PIECE
100,MS
116
PROCESSOR
126
MEMORY
112
A/D CONVERTER
100a
110
D.C. REMOVE
100b
114a
128a
128b
108a
108b
SYNTHESIZER
PLL
VCO
114c
I/Q MOD
128
108
I/Q DEMOD
114b
114
20
10
130
134a
106
LNA
104
132
VGA
PA
POWER CONTROL
134
102
138
136

FIG.5

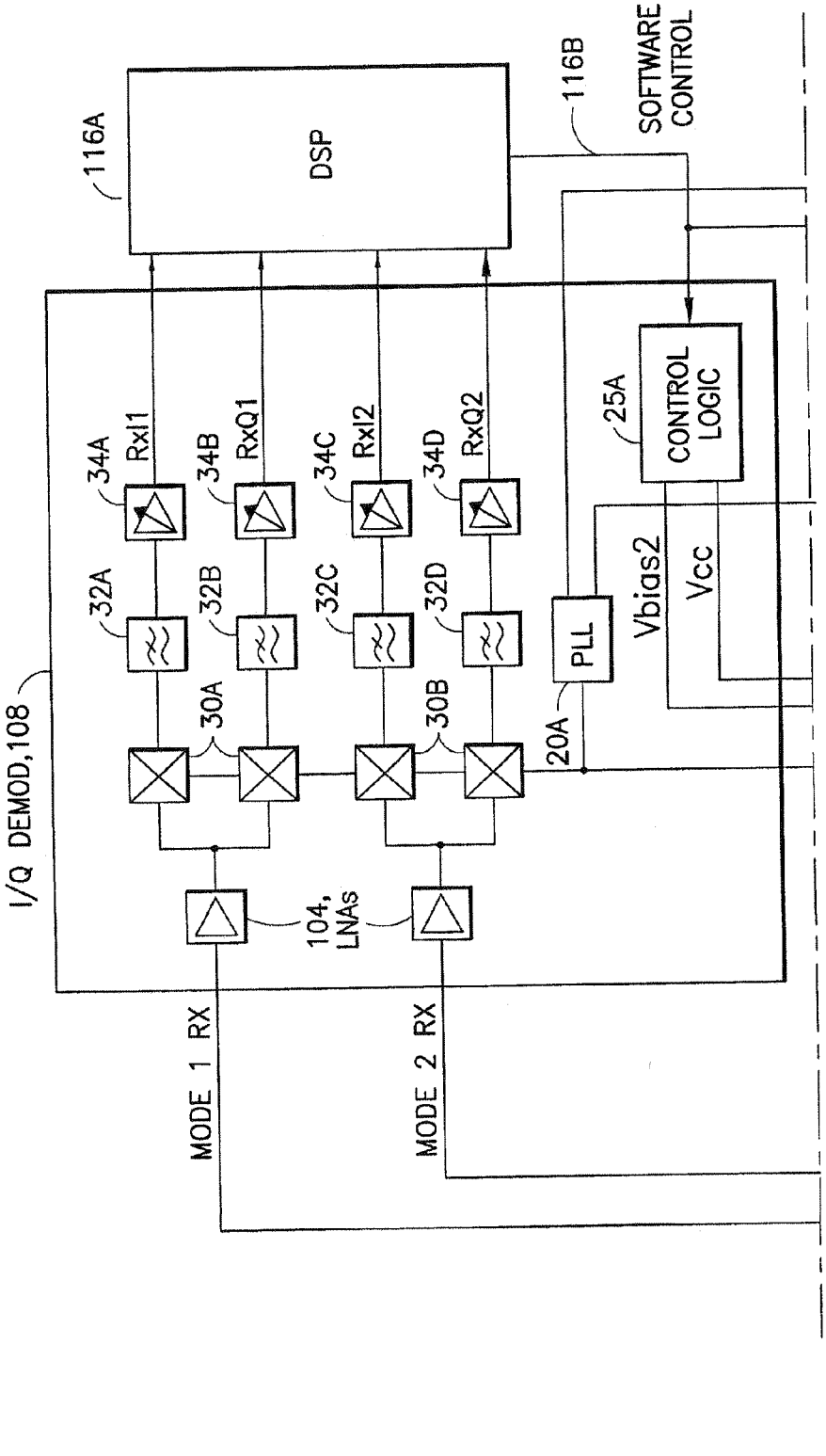


FIG.6A

FIG.6

FIG.6A
FIG.6B

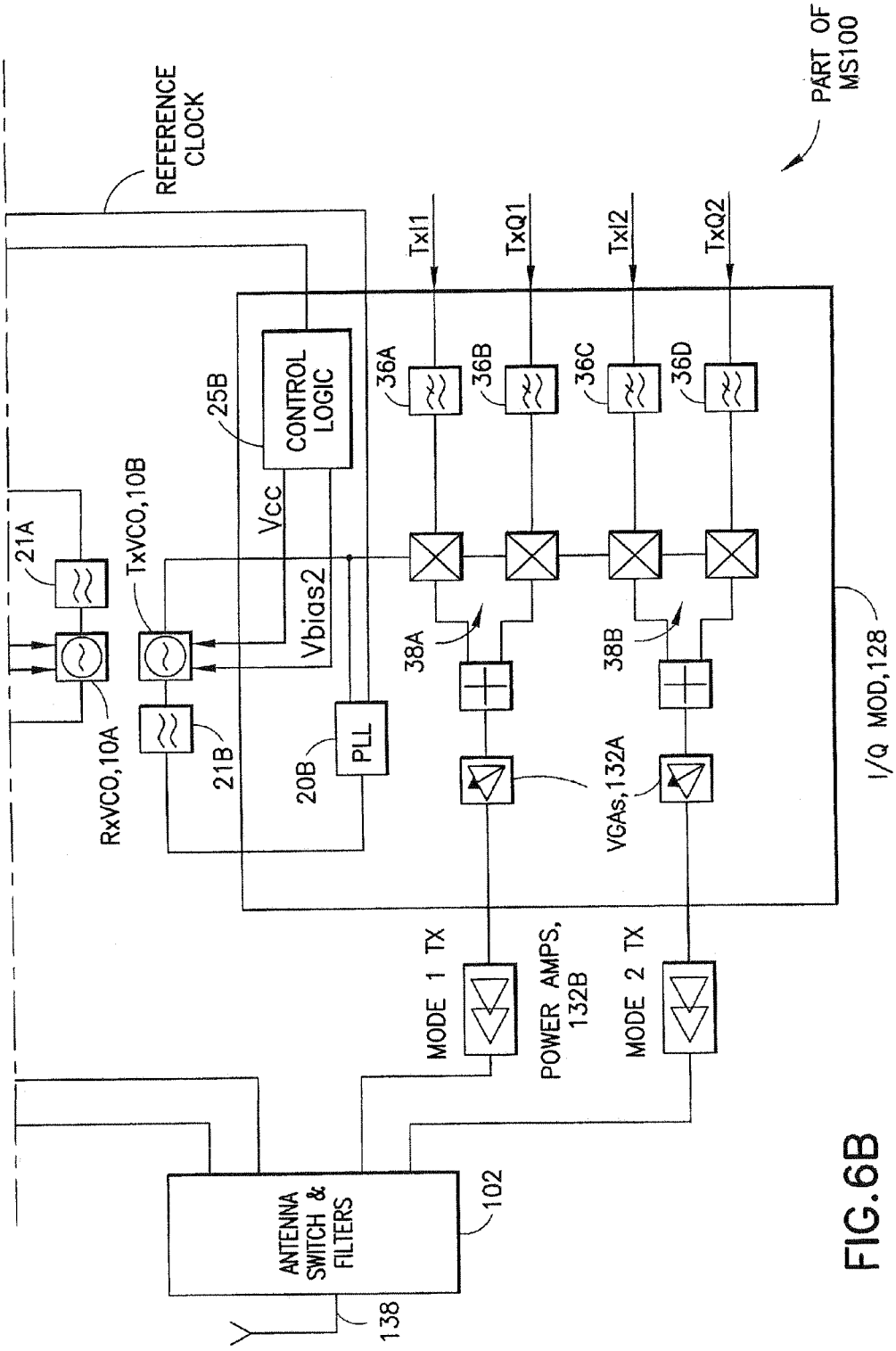

PART OF MS100
REFERENCE CLOCK
TxI1
TxQ1
TxI2
TxQ2
CONTROL LOGIC
25B
36A
36B
36C
36D
Vcc
Vbias2
TxVCO,10B
21A
RxVCO,10A
21B
PLL
20B
38A
38B
VGAs,132A
I/Q MOD,128
MODE 1 TX
POWER AMPS, 132B
MODE 2 TX
ANTENNA SWITCH & FILTERS
102
138

FIG.6B

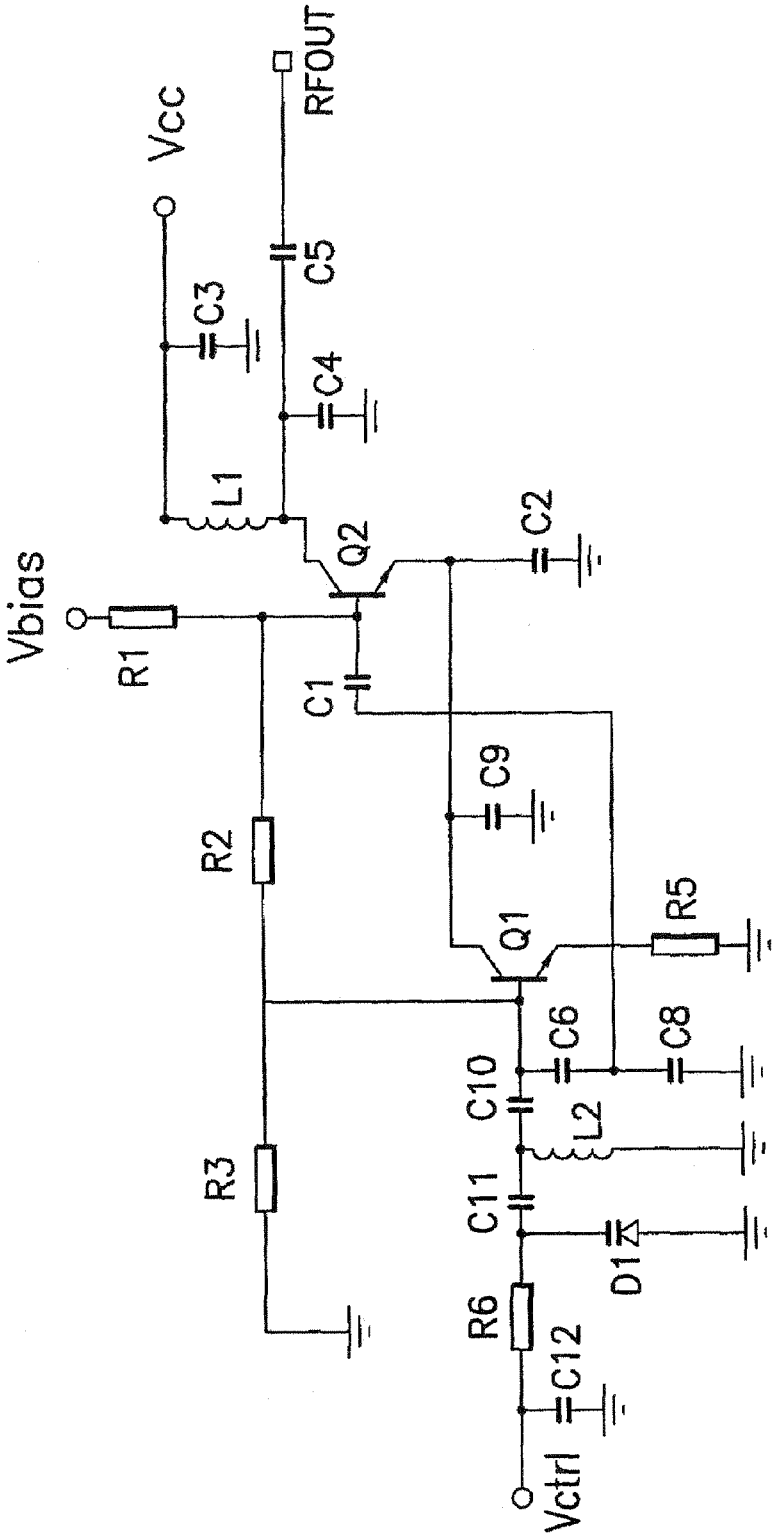

RFOUT
Vcc
C5
C3
C4
L1
Q2
C2
Vbias
R1
C1
C9
R2
Q1
R5
C6
C8
C10
L2
R3
C11
D1
R6
C12
Vctrl

FIG.8A

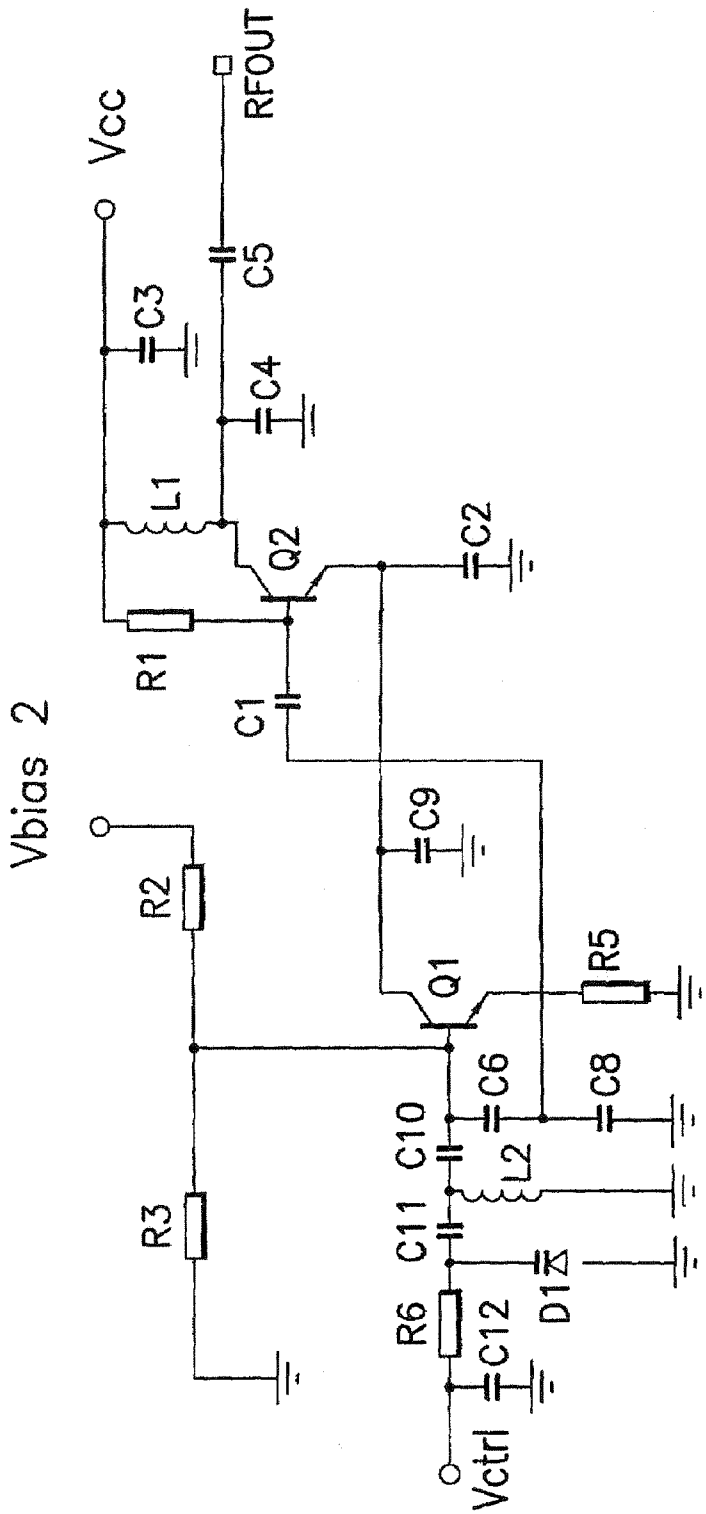

Vcc
RFOUT
C3
C5
C4
L1
Q2
C2
R1
C1
Vbias 2
C9
R2
Q1
R5
C6
C8
C10
L2
R3
C11
D1
R6
C12
Vctrl

FIG.8B

DUAL MODE VOLTAGE CONTROLLED OSCILLATOR HAVING CONTROLLABLE BIAS MODES AND POWER CONSUMPTION

TECHNICAL FIELD

These teachings relate generally to frequency sources and oscillators, and more specifically relate to voltage controlled oscillators used in mobile communication devices, in particular multi-mode mobile communication devices such as dual mode cellular telephones, also referred to herein as mobile stations.

BACKGROUND

A local oscillator (LO) signal is required for receiving and transmitting in a wireless (RF) communication device, such as a cellular telephone. A voltage controlled oscillator (VCO) is typically used in a phase-locked loop to generate the LO signal. The quality of the VCO signal, for example the phase noise, signal to noise floor, output power and environmental stability) that is required by the RF system strongly influences the current consumption. The current consumption is a very important consideration in portable, battery powered communication devices, as it impacts the duration of the talk and standby times between required battery recharging operations.

In different cellular systems different operational requirements are present, and the opportunities to reduce the power consumption thus differ as well. Also, different usage conditions and wireless network environments place different demands on the required quality of the VCO signal. For example, when no strong interference sources are present a lower quality VCO signal may be adequate.

When a mobile station is required to operate with only one cellular system, such as the Global System for Mobile Communications (GSM) system or a wideband code division multiple access (WCDMA) system, the VCO (and PLL) can be optimized for operation with that one specific system. However, in dual and higher mode mobile stations (e.g., GSM/WCDMA) the designer is faced with providing one VCO that is not entirely optimized for operation with either, or with providing multiple VCOs, one for each supported system. As can be appreciated, neither approach leads to an optimum reduced power consumption solution.

An example of the use of the multiple VCOs in a mobile station operable with different cellular networks can be found in U.S. Pat. No. 5,471,652, "Frequency Synthesizer and Multiplier Circuit Arrangement for a Radio Telephone", by Jaakko Hulkko.

Another example of a VCO used in a mobile station can be found in U.S. Pat. No. 5,926,071, "Minimization of the Power Consumption in an Oscillator", by Osmo Kukkonen. This patent presents a method for minimizing the current consumption and the operating voltage of a VCO, where the oscillator's RF output signal is detected as a DC voltage signal in a clamp/voltage multiplier circuit. The detected signal is supplied in a feedback loop to a field effect transistor (FET) that controls the oscillator's current. In this manner the FET controls the current to be a predetermined minimum value.

Conventionally VCOs having fixed bias voltage circuitry have been employed, and the bias voltage within the VCO has typically been heavily filtered. However, the amount of filtering must be controlled so as not to make the VCO too slow to stabilize when switching channels.

Also, in conventional usage the VCO has been powered on all the time in the conversation mode, while in the receive/idle mode the VCO has the fixed bias level, and is switched off only when it is determined that it will not be required again for some predetermined period of time (that is typically longer than the time for one or several bursts in a TDMA-type system, or some hundreds of microseconds).

SUMMARY OF THE PREFERRED EMBODIMENTS

The foregoing and other problems are overcome, and other advantages are realized, in accordance with the presently preferred embodiments of these teachings.

Disclosed is an oscillator circuit for use in a local oscillator of an RF communications device that communicates over an RF channel. The oscillator circuit includes an oscillator transistor coupled to a power supply voltage (Vcc) through a buffer transistor, and a bias voltage network having bias voltage outputs coupled to a control input of the oscillator transistor and to a control input of the buffer transistor. In one embodiment the bias voltage network is coupled to Vcc, while in another embodiment the bias voltage network is coupled to a separate voltage (Vbias). Circuitry is provided for setting a magnitude of Vcc and/or Vbias as a function of at least one of RF channel conditions, such as channels conditions determined from a calculation of the (SNR), or an operational mode of the RF communications device. The magnitude of Vcc (and Vbias) may be set between about zero volts (i.e., turned off) and some maximum value. The operational mode can be, for example, one of a TDMA, burst-type narrow bandwidth mode, or a CDMA, substantially continuous, wider bandwidth mode. The value of Vcc and/or Vbias may be set so as to minimize power consumption as a function of an amount of allowable local oscillator phase noise.

A broad bandwidth/narrow bandwidth dual mode RF transceiver in accordance with these teachings includes at least one phase locked loop (PLL) that includes a voltage controlled oscillator (VCO) providing a local oscillator signal for at least one of an I/Q modulator or an I/Q demodulator; a processor responsive to an output of said I/Q demodulator for determining at least one aspect of RF channel quality; and circuitry coupled between the processor and the VCO for minimizing at least VCO power consumption as a function of an amount of allowable VCO phase noise for a current RF channel quality.

In order to reduce overall power consumption it may be possible to turn off the VCO and possibly also the associated PLL loop, such as when no signal is being received or transmitted. This approach implies that sufficient time be allocated when turning the VCO and PLL back on to settle these circuits to a stable operational state.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other aspects of these teachings are made more evident in the following Detailed Description of the Preferred Embodiments, when read in conjunction with the attached Drawing Figures, wherein:

FIG. **1** is a simplified circuit diagram of a conventional VCO having a fixed VCC/bias supply;

FIG. **2** is a simplified circuit diagram showing the tuning of the supply voltage of the VCO to adjust its performance and power consumption;

FIG. **3** is a simplified circuit diagram showing the tuning of either one or both of the supply voltage and bias voltage of the VCO to adjust its performance and power consumption;

FIG. **4** is a simplified circuit diagram showing the tuning of either one or both of the supply voltage and bias voltage of the VCO, including the use of a separate bias voltage (Vbias**2**) for the oscillator transistor to adjust the VCO performance and power consumption;

FIG. **5** is a block diagram of a mobile station this constructed and operated in accordance with these teachings;

FIG. **6** is a block diagram that shows a portion of mobile station of FIG. **5** in greater detail, in particular the use of transmit (TX) and receive (RX) VCOs that are operated and controlled in accordance with these teachings;

FIG. **7** is an exemplary waveform and timing diagram showing the turning off and on of the VCO in a TDMA reception/transmission mode of operation;

FIG. **8**A illustrates a more detailed schematic diagram of the VCO of FIG. **3**; and

FIG. **8**B illustrates a more detailed schematic diagram of the VCO of FIG. **4**.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. **1** is a simplified circuit diagram of a portion of a conventional VCO **1** having a fixed VCC/bias supply. The VCO **1** includes a buffer stage transistor Q**1**, an oscillator stage transistor Q**2**, and a plurality of resistances or impedances shown generally as R**1**, R**2**, R**3** and R**4**, connected as shown. In general, R**1**, R**2** and R**3** are series connected between Vcc and circuit ground, and a bias voltage for Q**1** is developed between R**1** and R**2**, and a bias voltage for Q**2** is developed between R**2** and R**3**. An optional noise reduction filter capacitor C**1** may be connected from the biasing point of Q**2** to ground, however its presence can adversely affect the response and turn-on times of the VCO. In this conventional embodiment the value of VCC is not specifically tuned based on the operating condition or mode of the VCO, but instead may be fixed by the output of a voltage regulator that experiences normal fluctuations based on load, temperature and the like.

FIG. **2** is a simplified circuit diagram showing the tuning of the supply voltage of a VCO **10** to adjust its performance and power consumption, in accordance with an aspect of these teachings. In this embodiment the value of Vcc is made adjustable (shown for convenience as an adjustable resistor (Radj)), and it may also be turned off and on (shown for convenience as a switch (SW)). In this latter case it is preferred that the oscillator bias voltage filter capacitor C**1** of FIG. **1** not be used, or if it is that its value be made small, so as not to detrimentally affect the turn-on and turn-off times of Q**2**.

FIG. **3** is a simplified circuit diagram showing the tuning of the supply voltage of the VCO **10** to adjust its performance and power consumption, as in FIG. **2**, and further shown in this embodiment is that the bias voltage Vbias can be decoupled from Vcc, and can also be made adjustable and/or switchable on/off using Vbias_Radj and Vbias_SW. While Vbias may be sourced from a separate supply, it may also be supplied by Vcc. In this manner the value of Vbias can be separately controlled and optimized, and switched on and off as well, in order to change the performance and power consumption of the VCO **10**. The optional bias filter capacitor C**1** is also shown in this diagram.

FIG. **4** is a simplified circuit diagram showing the tuning of the supply voltage of the VCO **10** to adjust its performance and power consumption, as in FIG. **2**, and in a further embodiment that the bias voltage Vbias for the oscillator Q**2** is made separately variable and/or switchable on/off using Vbias_Radj and Vbias_SW. In this manner the value of Vbias for the oscillator transistor Q**2**, referred to as Vbias**2**, can be separately controlled and optimized, and switched on and off as well, in order to change the performance and power consumption of the VCO **10**. The optional bias filter capacitor C**1** is also shown in this circuit diagram. Note that the main current path through Q**1** and Q**2** (collector current) is isolated from C**1**, and thus is enabled to be switched on and off in a rapid manner.

Reference is made now to FIG. **5** for showing a VCO **10** and a PLL **20** in the context of a wireless communication terminal transceiver, such as a cellular telephone, also referred to herein for simplicity as a mobile station **100**. More specifically, FIG. **5** is a block diagram of a transmitter-receiver (transceiver) of the mobile station **100**, wherein the receiver is embodied as direct conversion receiver. An RF signal received by an antenna **138** is conducted via a duplex filter **102** to a low noise amplifier (LNA) **104**. The purpose of the duplex filter **102** is to permit the use of the same antenna both in transmitting and in receiving. Instead of the duplex filter **102**, a synchronous antenna changeover switch could be used in a time-division system. An RF signal output from the LNA **104** is low-pass filtered **106** and demodulated in an I/Q demodulator **108** into an in-phase (I) signal **108***a* and into a quadrature (Q) signal **108***b*. A local oscillator signal **114***b*, used for I/Q demodulation, is received from a synthesizer **114**. The synthesizer **114** contains the PLL **20** and the VCO **10**, described in further detail below in regard to FIG. **6**. In block **110**, the removal of a DC voltage component is carried out, as is automatic gain control (AGC). Block **110** is controlled by a processing block **116** that may contain, for example, a microprocessor. Automatic gain control is regulated by a signal **110***a* and removal of the offset voltage is regulated by a signal **110***b*. The analog signals output from block **110** are converted into digital signals in block **112**, and from which the digital signals are transferred to digital signal processing circuits in the processing block **116**.

The transmitter portion of the mobile station **100** includes an I/Q modulator **128** that forms a carrier frequency signal from an in-phase (I) signal **128***a* and from a quadrature (Q) signal **128***b*. The I/Q modulator **128** receives a local oscillator signal **114***c* from the synthesizer **114**. The generated carrier frequency signal is low-pass filtered and/or high-pass filtered by a filter **130** and is amplified by an RF amplifier **132** containing a variable gain amplifier (VGA) and a power amplifier (PA). The amplified RF signal is transferred via the duplex filter **102** to the antenna **138**. A transmitter power control unit **134** controls the amplification of the RF amplifier **132** on the basis of the measured output power **136** and in accordance with a control signal **134***a* received from the processor **116**.

The processor **116** also controls the synthesizer **114** using a programming line or bus **114***a*, whereby the output frequency of the synthesizer **114** is controllably changed, as when tuning to different transmission and reception channels and/or to different frequency bands. The processor **116** can include a digital signal processor DSP) **116**A, shown in FIG. **6** and described in further detail below.

For completeness FIG. **5** also shows, connected to the processor **116**, a memory unit **126** and a user interface having a display **118**, a keyboard **120**, a microphone **122** and an earpiece **124**.

FIG. **6** shows in greater detail the construction of the I/Q demodulator **108** and the I/Q modulator **128**, as well as the synthesizer **114** and the DSP **116**A for a dual mode (Mode 1, Mode 2) embodiment. As an example, Mode 1 is a TDMA GSM mode, while Mode 2 is WCDMA mode. Shown in the receive (RX) path in this exemplary embodiment are separate LNAs **104**, a plurality of I/Q mixers **30**A, **30**B and associated filters **32**A–**32**D, and variable gain amplifiers **34**A–**34**D outputting, at any given time, either the received Mode 1 I/Q signals (RXI**1**, RXQ**1**) or the Mode 2 I/Q signals (RXI**2**, RXQ**2**) to the DSP **116**A. The receive PLL **20**A and associated RX_VCO **10**A function as a local oscillator (LO) and provide the mixing frequency to the I/Q mixers **30**A, **30**B. The DSP **116**A outputs over a control bus **116**B control information to receive control logic **25**A, which in turn outputs the Vcc and Vbias**2** voltages to the RX_VCO **10**A (this example thus assumes the embodiment of FIG. **4**, but is not limited for use only within this embodiment, as the embodiments of FIGS. **2** and **3** could be utilized as well.) The control logic **25**A also implements the switching on and off of these voltages. As such, the control logic **25**A may be implemented using a plurality of D/A converters for converting digital data from the DSP **116**A into corresponding voltages Vcc and Vbias**2** for the RX_VCO **10**A, and thereby implements the functions shown generally as the variable resistances Radj and Vbias_Radj, and the switches SW and Vbias_SW, in FIG. **4**.

The transmit (TX) side is constructed so as to basically mirror the RX side, and includes a plurality of input filters **36**A–**36**D for the incoming TXI**1**, TXQ**1** and TXI**2**, TXQ**2** signals to be transmitted. Mode 1 and 2 I/Q modulators **38**A and **38**, respectively, receive their respective mixing frequencies from the PLL **20**B/TX_VCO **10**B, and provide their outputs to variable gain amplifiers (VGAs) **132**A and power amplifiers **132**B, shown collectively in FIG. **5** in circuit block **132**. As in the receive side, the DSP **116**A controls the magnitudes of the TX_VCO **10**B Vcc and Vbias**2** voltages using TX control logic block **25**B.

For completeness each of the RX and TX PLLs **20**A and **20**B is shown to contain a loop filter **21**A, **22**1B, respectively, and receives a (common) reference clock.

The specific mobile station **100** construction shown in FIGS. **5** and **6** is exemplary, and is not to be construed in a limiting sense upon the practice of these teachings. For example, a superheterodyne type of RF architecture could be employed in other embodiments, as opposed to the direct conversion architecture depicted in FIGS. **5** and **6**.

Based on the foregoing it can be appreciated that these teachings provide a VCO **10** that has different bias modes, for example one for the GSM mode and one the WCDMA mode. There may be different bias currents, and hence different amounts of power consumption, used when the spectral environment of the MS **100** changes. For example, burst-type GSM-based systems typically require better signal quality at the receiver when high interference levels are present, while WCDMA-based systems require low VCO power consumption as the VCO **10** must be turned on almost continuously during the conversation mode or state. The required VCO **10** output level also determines the power consumption. For example, the output level required is dependent on the Signal-to-Noise (SNR) requirements and the circuitry to be driven. In general, it is desired to operate so that the VCO level is at or near the minimum required level so that the power consumption can be minimized.

Referring to FIG. **7**, with systems using time division duplex (TDD) it is possible to shut off the VCO **10**A, **10**B and the PLL **20**A, **20**B for certain periods between received and/or transmitted bursts. In this case it is preferred to shut off the primary VCO current (collector current of Q**2**) and to leave the bias voltages (base currents) on. This also provides the opportunity to perform optimum low noise, low frequency filtering for these critical bias voltages, to avoid the amplification of noise at the base of the oscillator transistor Q**2**. When RC filtering is employed, the decoupling of the base and collector currents, as in FIG. **4**, does not negatively impact the turn on and turn off times of Q**2**, as the collector current path not connected to the filter capacitor C**1**. The settling time of the VCO **10** is thus made faster, making this type of operation feasible using low cost and readily fabricated circuitry.

In order to control the levels of Vcc and Vbias**2**, the Signal to Noise Ratio (SNR) of the received signal can be calculated by the DSP **116**A in a conventional manner, and then used to determine the bias/current level of the VCO **10**. The SNR may be calculated as often as is desired, and the magnitudes of Vcc and/or Vbias**2** also controlled as often as desired, preferably in real-time or in near-real time in order to accommodate the changing propagation conditions of the radio channel. When the SNR is found to exceed some threshold, and the VCO **10** cannot be shut off, then Vcc can be reduced, along with Vbias**2**, to run the VCO **10** in a lower power consumption mode. If the SNR is found to be degrading over time, for example in a TDMA or a WCDMA embodiment, then the DSP **116**A is enabled to increase the Vcc and Vbias**2** levels of the VCOs **10**A and **10**B until the SNR is at an acceptable level, or until a maximum Vcc/Vbias**2** level is reached. Using these teachings the MS **100** is enabled to adjust or tune the phase noise of the VCO according to the mode of operation of the transceiver, and to thus control the amount of current consumption as a function of the required VCO signal quality. Furthermore, and as was shown in FIG. **7**, the VCO **10** and PLL **20** can be switched off when not needed, such as between bursts in a narrow band (TDMA) made.

In general, the SNR calculated by the DSP **116**A provides good information regarding the quality of the received signal, as it includes the entire signal path with all gain stages, filtering, saturation, VCO/PLL-based noise and so on. Furthermore, the signal used for the SNR calculation is in the digital domain after A/D conversion, and thus includes any disturbances that may be introduced by digital filtering and the like.

It has been known to calculate the SNR using DSP **116**A software for enabling the sleep stage or mode of the MS receiver. However, the SNR information is available as well in the idle mode and in the conversation mode. By using this information it is possible to detect the reduction in performance (lowering of the SNR, and related increases in the Bit Error Rate (BER) and/or Block Error Rate (BLER)), and to compensate by increasing the performance of the VCO **10**. When propagation conditions improve, the performance of the VCO **10** can be reduced accordingly, thereby reducing power consumption and prolonging battery life.

Other parameters and metrics can be determined and used as well, such as a received signal strength indicator (RSSI), signal to interference ratio (SIR) and/or the received signal code power (RSCP). Combinations of these and other metrics may be made in order to determine the optimum settings for the VCO **10** Vcc and/or Vbias **2** voltages. The employed

metrics may also change as the operational mode is changed (e.g., from a TDMA mode to a CDMA mode and vice versa).

Other parameters, such as the mixer and I/Q demodulator **108** currents and other signal dependant RF stages can also be optimized for low current consumption, such that when the signal quality degrades additional power/current/voltage in provided to the affected stage(s) to increase their performance.

As was mentioned, in the WCDMA mode of operation the continuous current consumption of the receiver is important because, for example in the talk mode or conversation state, the receiver is on almost continuously. Thus, a large benefit is realized by using low amounts of battery current in those typical conditions where the transmitter level is low and/or in a signal environment at the receiver input that is "clean" (i.e., free of high disturbing levels and interference). Furthermore, in the WCDMA system the transmitter of the MS **100** can cause receiver saturation when transmitting at high levels and when the receiver is operating with low currents/voltages.

However, the WCDMA may be only one mode out of two or more in the MS **100**, so that the problems introduced by its operation may disappear when operating in another mode, such as the TDMA GSM mode, or in a multi-media mode. The teachings of this invention enable one to better optimize the performance of MS **100** for different modes and conditions, and to optimize the power consumption to the current mode of operation.

The SNR calculated by the DSP **116**A can be used as well for other purposes, such as tuning the timing of certain RF functions, changing the states of the receiver, for example changing the states of certain gain stages, as well as to generally optimize the receiver performance, such as sensitivity, blocking and adjacent time slot performance.

Typical Vcc voltages that may be employed are in the range of about 2.7 to 1.8 volts, and the value of Vbias depends on the value of Vcc. For the case where narrowband and wideband modes are used examples include, but are not limited to, a GSM/WCDMA embodiment wherein the GSM channel spacing is 200 kHz and the WCDMA channel spacing is 5 Mhz.

It can be appreciated that the schematic diagrams of FIGS. **2**, **3** and **4** were greatly simplified in order to more clearly illustrate the teachings of this invention. For a more practical (and exemplary) embodiment reference can be made to FIGS. **8**A and **8**B, where FIG. **8**A is a more detailed schematic diagram of the VCO **10** of FIG. **3** and FIG. **8**B is a more detailed schematic diagram of the VCO **10** of FIG. **4**. Note that these schematic diagrams are based on FIG. 1 of U.S. Pat. No.: 5,926,071 (incorporated by reference herein). However, as compared to FIG. 1 of U.S. Pat. No. 5,926,071 the designations of Q1 and Q2 are reversed, and R1, R2 and R3 are renumbered, so as to agree with the numbering scheme of FIGS. **3** and **4**. These schematic diagrams are provided merely as examples to show the voltage control (Vctrl) input to Q1, the RF output node (RFOUT) of the VCO **10**, as well as a more practical circuit implementation of VCOs that incorporate the teachings of this invention. In FIGS. **8**A and **8**B the magnitude of Vcc is assumed to be adjustable, as is the magnitude of Vbias and Vbias**2**, as was discussed in detail above.

The specific circuitry shown in FIGS. **8**A and **8**B is not intended to be viewed as a limitation upon the practice of this invention, as those skilled in the art will recognize that other circuit embodiments having more or fewer components could be employed to construct a working VCO. Further in this regard, it should also be realized that in some embodiments the buffer stage transistor Q1 could be eliminated, and RFOUT taken through C1 from the upper end of R5 in FIGS. **8**A and **8**B. In this case Vcc is fed directly to Q1, and not through Q2. It is also within the scope of these teachings that each of Q1 and Q2 have their own Vcc supply.

Thus, it should be appreciated that while these teachings have been presented in the context of certain presently preferred embodiments, that changes in form and detail may be made by those skilled in the art, when guided by these teachings, and that these changes will still fall within the scope of the teachings of this invention.

What is claimed is:

1. An oscillator circuit for use in a local oscillator of an RF communications device that communicates over an RF channel, said oscillator circuit comprising an oscillator transistor coupled to a power supply voltage (Vcc) through a buffer transistor and a biasing network having bias voltage outputs coupled to a control input of said oscillator transistor and to a control input of said buffer transistor, said bias voltage network being coupled to Vcc, and further comprising circuitry for setting a magnitude of Vcc as a function of at least one of RF channel conditions or an operational mode of the RF communications device, wherein the value of Vcc is set so as to minimize power consumption as a function of an amount of allowable local oscillator phase noise, and where Vcc is coupled to said oscillator transistor directly or via a buffer transistor.

2. An oscillator circuit as in claim **1**, wherein said RF channel conditions are determined by calculating a signal-to-noise ratio (SNR).

3. An oscillator circuit as in claim **1**, wherein the magnitude of Vcc is set between about zero volts and some maximum value.

4. An oscillator circuit as in claim **1**, wherein said operational mode is one of a TDMA mode or a CDMA mode.

5. An oscillator circuit as in claim **1**, wherein said operational mode is one of a burst transmission and reception mode or a substantially continuous transmission and reception mode.

6. An oscillator circuit as in claim **1**, wherein said operational mode is one of a narrow bandwidth mode or a wider bandwidth mode.

7. An oscillator circuit for use in a local oscillator of an RF communications device that communicates over an RF channel, said oscillator circuit comprising an oscillator transistor coupled to a power supply voltage (Vcc) through a buffer transistor and a bias voltage network having bias voltage outputs coupled to a control input of said oscillator transistor and to a control input of said buffer transistor, said bias voltage network being coupled to another power supply voltage Vbias, and further comprising circuitry for setting a magnitude of both Vcc and Vbias as a function of at least one of RF channel conditions or an operational mode of the RF communications device, wherein the values of Vcc and Vbias are set so as to minimize power consumption as a function of an amount of allowable local oscillator phase noise.

8. An oscillator circuit as in claim **7**, wherein said RF channel conditions are determined by calculating a signal-to-noise ratio (SNR).

9. An oscillator circuit as in claim **7**, wherein the magnitude of Vcc and Vbias is set between about zero volts and some maximum value.

10. An oscillator circuit as in claim **7**, wherein said operational mode is one of a TDMA mode or a CDMA mode.

11. An oscillator circuit as in claim 7, wherein said operational mode is one of a burst transmission and reception mode or a substantially continuous transmission and reception mode.

12. An oscillator circuit as in claim 7, wherein said operational mode is one of a narrow bandwidth mode or a wider bandwidth mode.

13. A broad bandwidth/narrow bandwidth dual mode RF transceiver, comprising:

at least one phase locked loop (PLL) that includes a voltage controlled oscillator (VCO) providing a local oscillator signal for at least one of an I/Q modulator or an I/Q demodulator;

a processor responsive to an output of said I/Q demodulator for determining at least one aspect of RF channel quality; and

circuitry coupled between said processor and said VCO for minimizing at least VCO power consumption as a function of an amount of allowable VCO phase noise for a current RF channel quality.

14. A dual mode RF transceiver as in claim 13, wherein at least said VCO can be turned off between bursts when operating in said narrow bandwidth mode.

15. A dual mode RF transceiver as in claim 13, wherein a magnitude of one or both of a VCO supply voltage Vcc and a VCO biasing supply voltage Vbias are variable by said circuitry for varying the power consumption of said VCO.

16. A dual mode RF transceiver as in claim 15, wherein the magnitude of Vcc and Vbias is variable between about zero volts and some maximum value.

17. A dual mode RF transceiver as in claim 13, wherein said RF channel quality is determined by calculating a signal-to-noise ratio (SNR).

18. A method for operating a broad bandwidth/narrow bandwidth dual mode RF transceiver, comprising:

operating at least one phase locked loop (PLL) that includes a voltage controlled oscillator (VCO) to provide a local oscillator signal for at least one of an I/Q modulator or an I/Q demodulator;

responsive to an output of said I/Q demodulator, determining at least one aspect of RF channel quality; and

minimizing at least the power consumption of said VCO as a function of an amount of allowable VCO phase noise for a current RF channel quality.

19. A method as in claim 18, and further comprising turning off at least said VCO between bursts when operating in said narrow bandwidth mode.

* * * * *

EXHIBIT C

US006115593A

United States Patent [19]

Alinikula et al.

[11] Patent Number: 6,115,593

[45] Date of Patent: Sep. 5, 2000

[54] **ELIMINATION OF D.C. OFFSET AND SPURIOUS AM SUPPRESSION IN A DIRECT CONVERSION RECEIVER**

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[73] Assignee: **Nokia Mobile Phones, Ltd.**, Espoo, Finland

[21] Appl. No.: **08/851,530**

[22] Filed: **May 5, 1997**

[30] **Foreign Application Priority Data**

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[52] **U.S. Cl.** **455/324**; 455/283; 375/319; 375/316

[58] **Field of Search** 455/283, 293, 455/324, 295, 296, 309, 308, 312, 337; 375/319, 316, 285, 346

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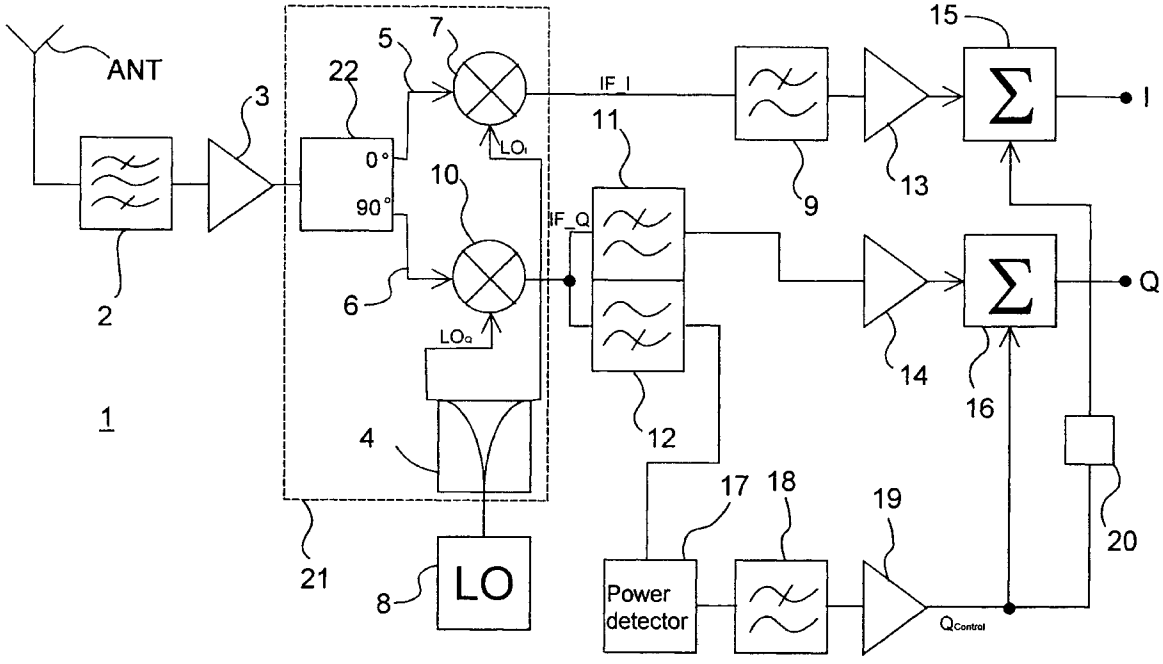
Primary Examiner—Wellington Chin
Assistant Examiner—Sheila Smith
Attorney, Agent, or Firm—Perman & Green, LLP

[57] **ABSTRACT**

In a method for compensating D.C. offset in a direct conversion receiver by a signal (IF_I, IF_Q) received and demodulated in one of the channels of the reception frequency band of a radio communication system, a correction signal ($Q_{control}$) is produced from the signals in the channels of the reception frequency band. The correction signal ($Q_{control}$) is combined with the demodulated signal. The apparatus for implementing the method comprises means (**12**, **17**, **18**, **19**) for producing the correction signal, and means (**15**, **16**) for combining the correction signal with the received and demodulated signal.

15 Claims, 6 Drawing Sheets



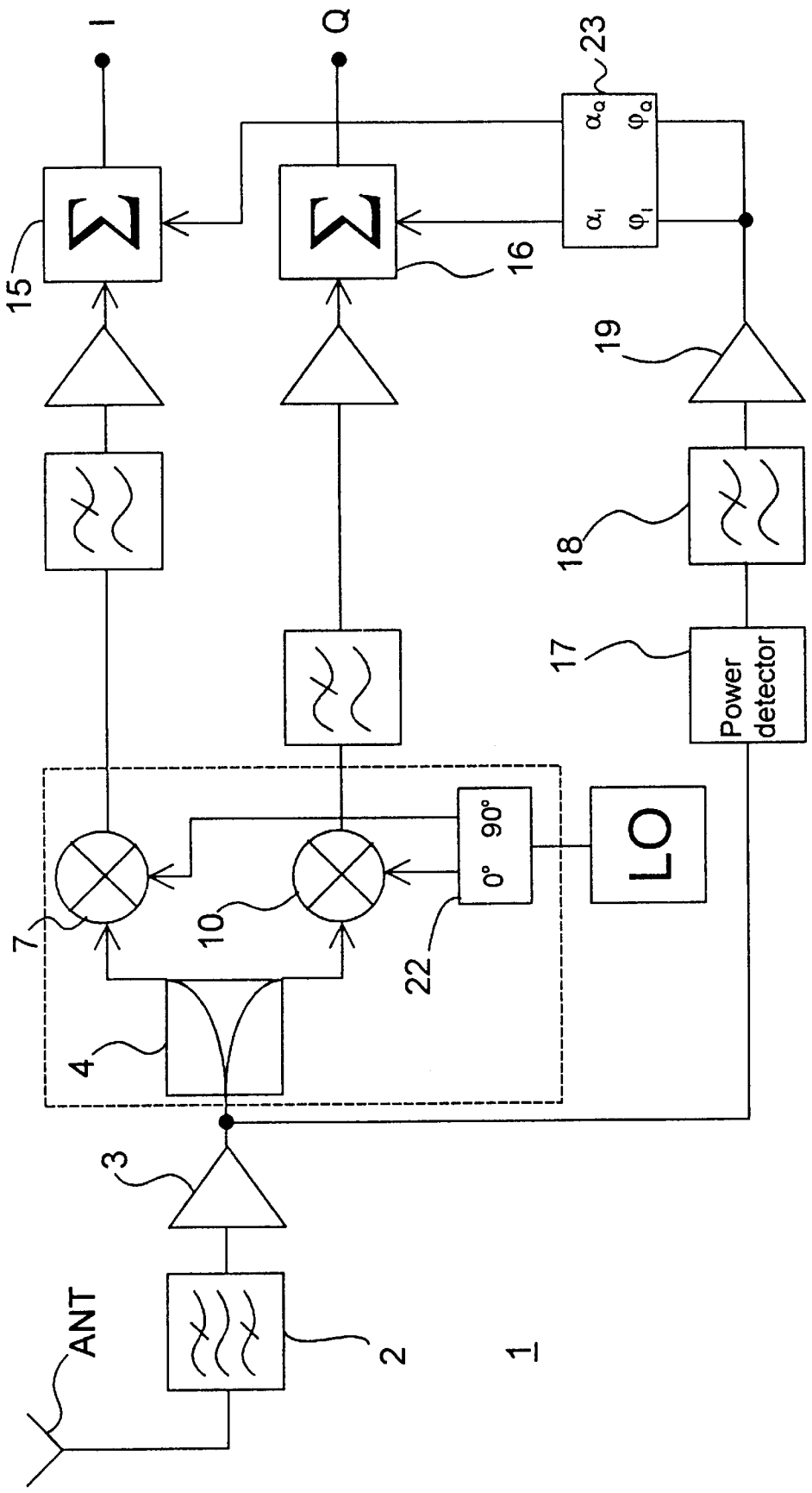


Fig. 1

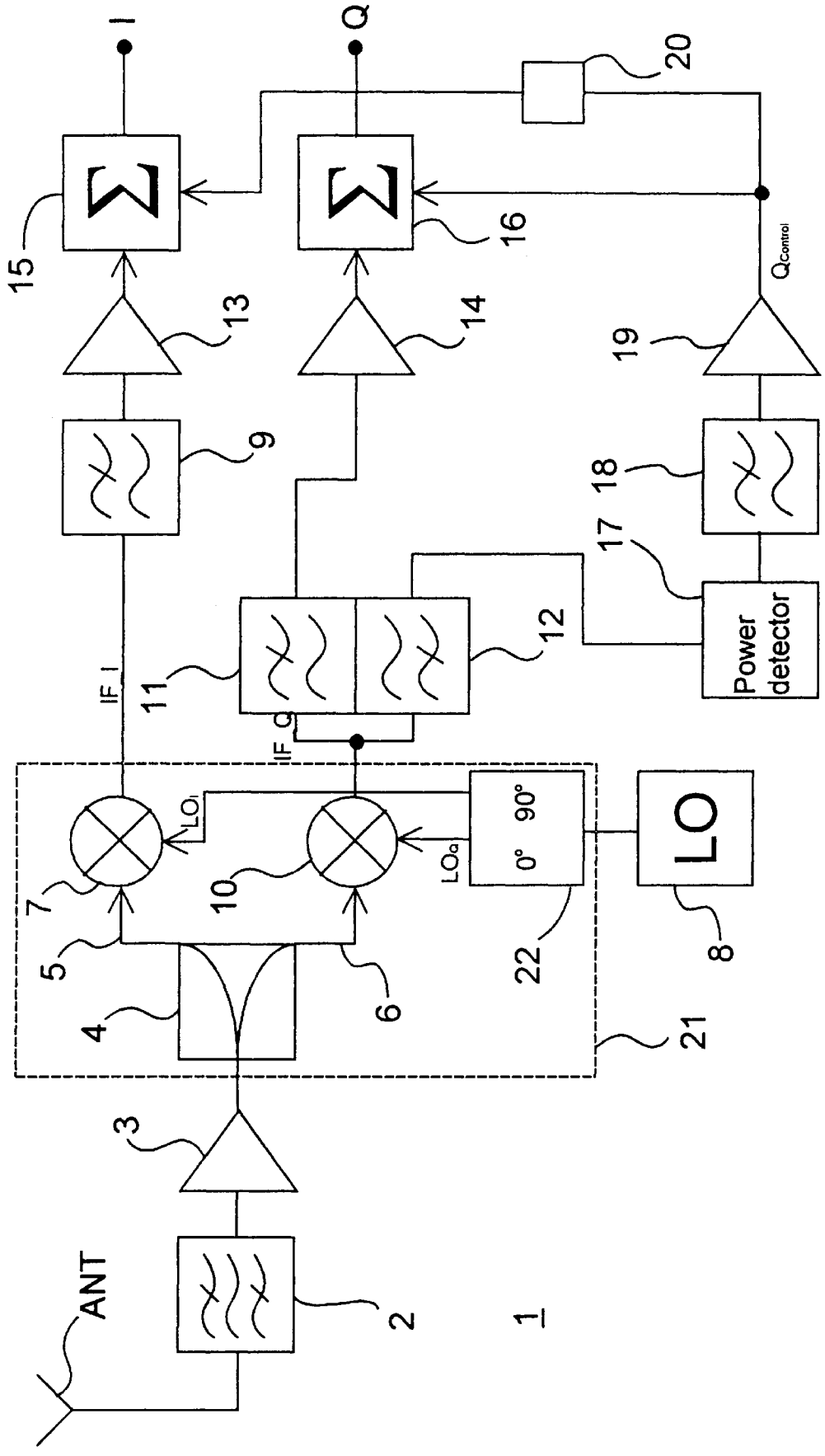


Fig. 2a

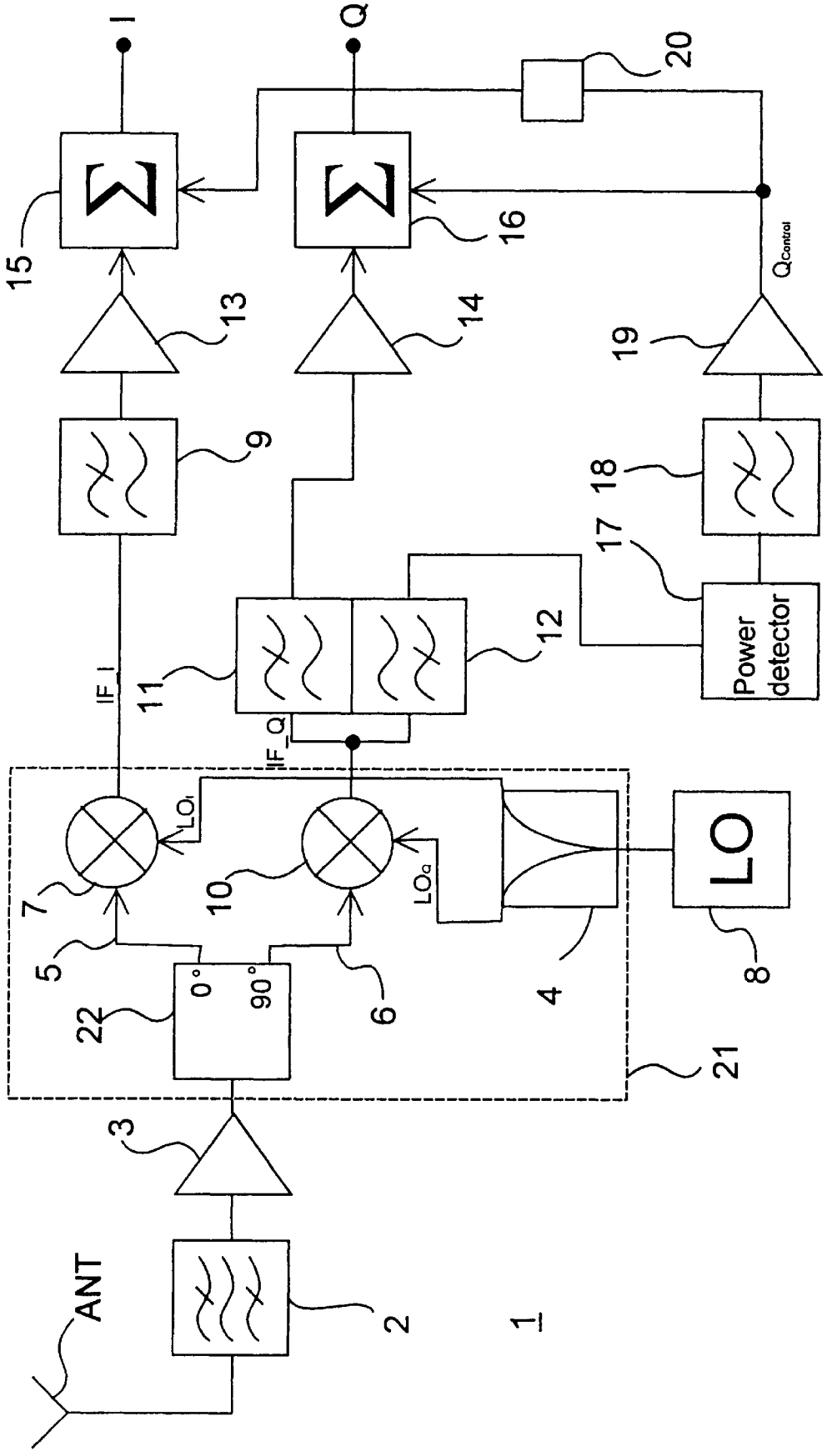


Fig. 2b

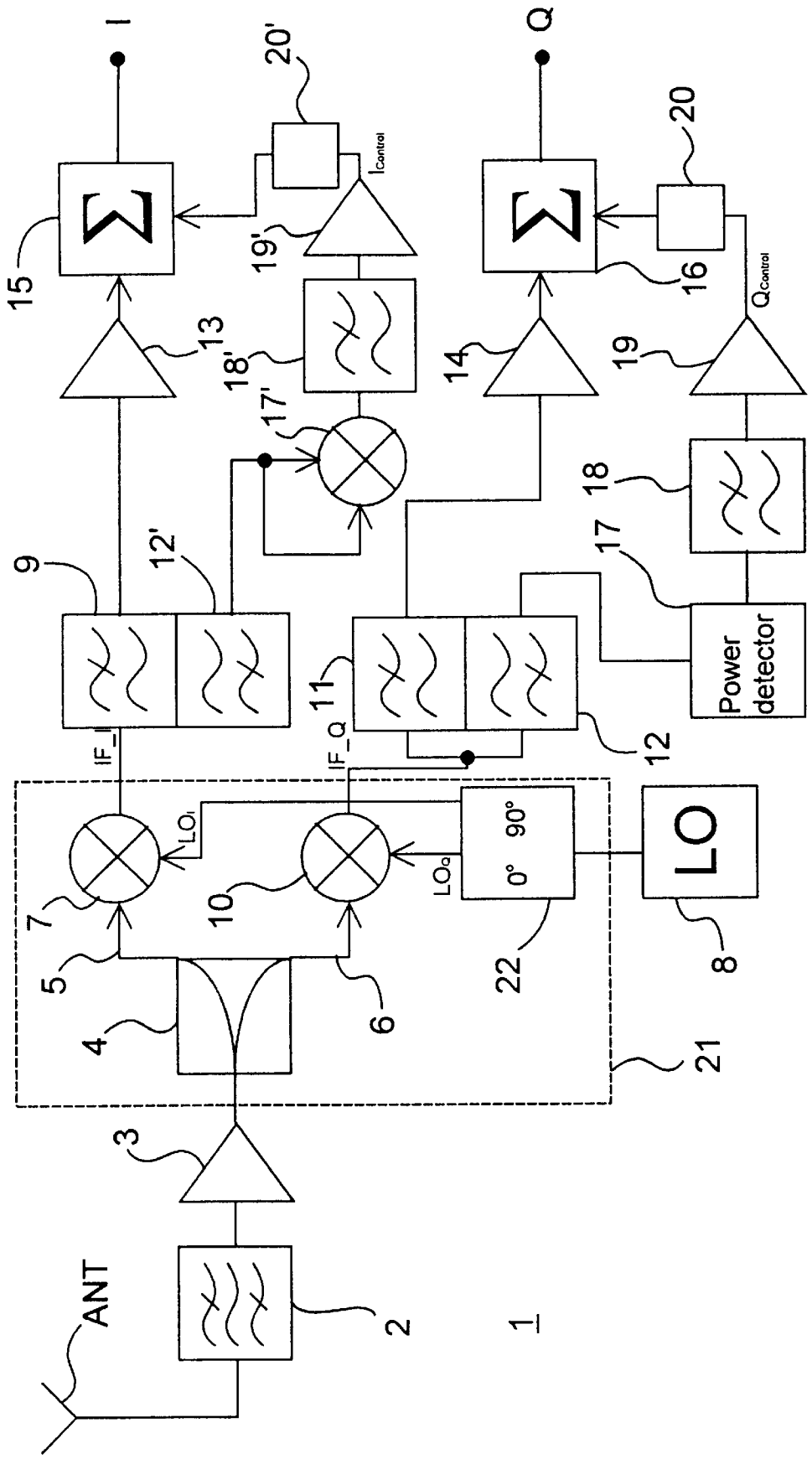


Fig. 3

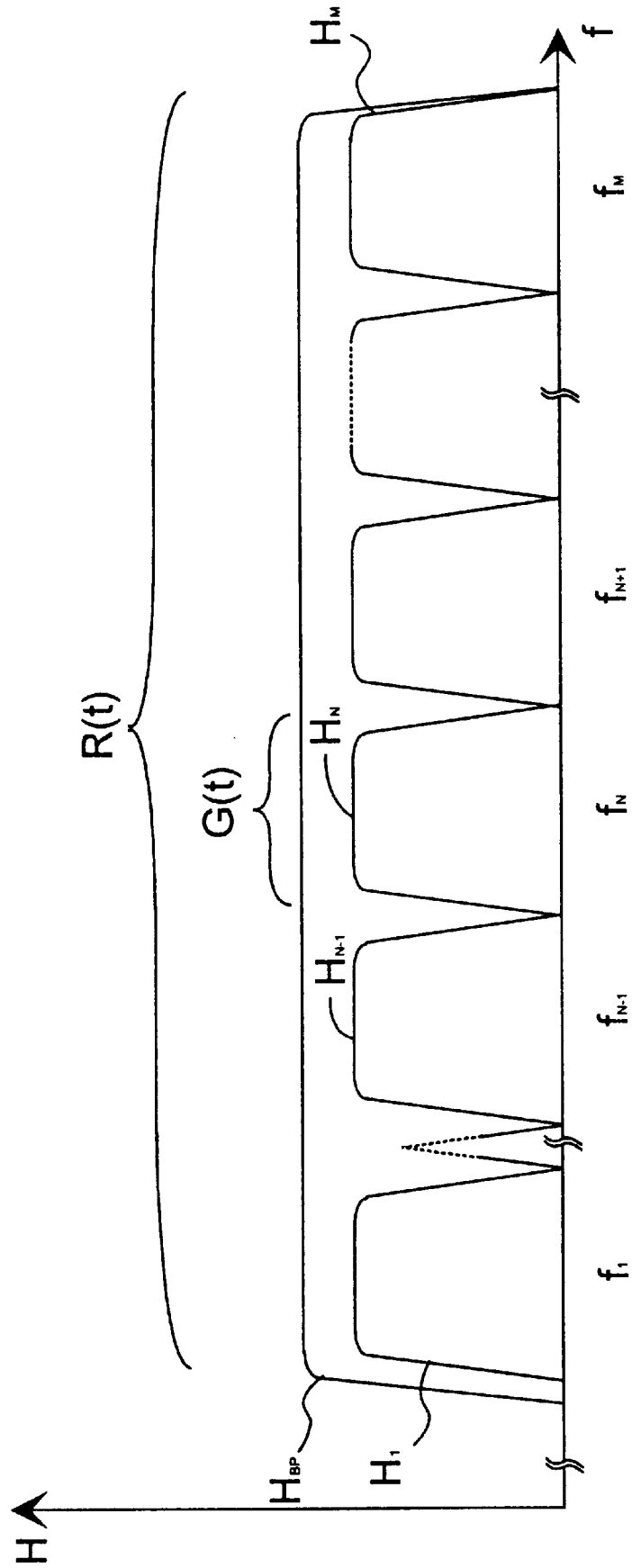


Fig. 4a

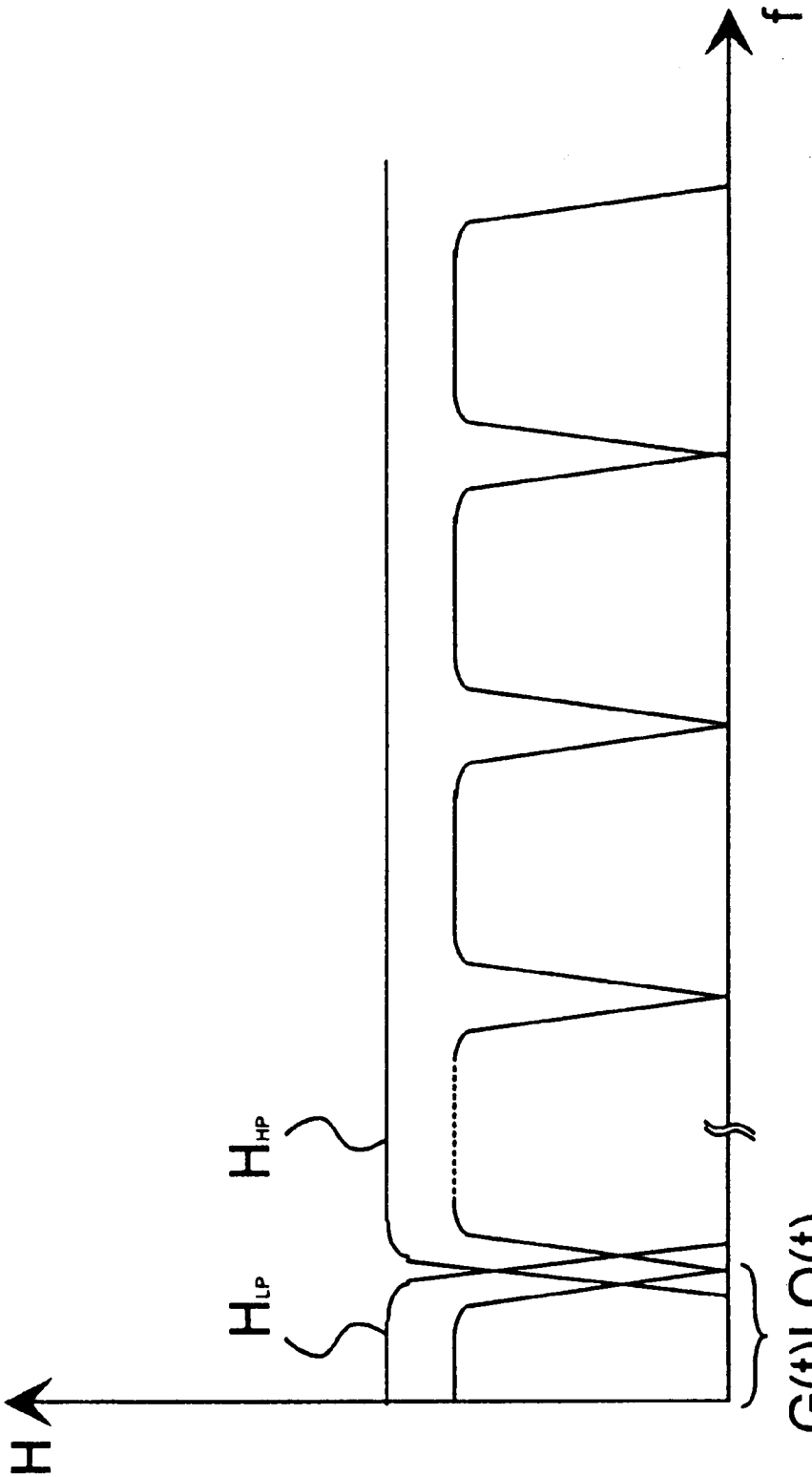


Fig. 4b

ELIMINATION OF D.C. OFFSET AND SPURIOUS AM SUPPRESSION IN A DIRECT CONVERSION RECEIVER

BACKGROUND OF THE INVENTION

The present invention relates to a method presented in the preamble of claim **1** and to an apparatus presented in the preamble of claim **10** for eliminating D.C. offset and achieving AM suppression in a direct conversion receiver.

In a direct conversion receiver, radio frequency signals are converted directly into baseband signals, whereby separate intermediate frequency stages are not required. In that case, the number of high frequency components needed in direct conversion receivers is smaller than in conventional receivers which include intermediate frequency stages. Due to less complexity, the integration degree of direct conversion receivers can be increased compared to receivers which include intermediate frequency stages.

However, receivers implemented with the direct conversion technique have the problem that their dynamic range is smaller than in receivers which include intermediate frequency stages. The dynamic range is adversely affected by the fact that in addition to the high frequency signal of the reception channel, the mixer of the receiver also receives high frequency signals of the adjacent channels, whereby due to the non-ideality of the mixer, a disturbing D.C. offset is produced on the output of the mixer. Thus the stronger signals of the adjacent channels can produce a substantially higher D.C. offset in the signal than the desired signal expressed on the reception channel.

In a digital receiver, the decision on whether the transmitted symbol is 0 or 1 is made on the basis of the voltage level of the demodulated signal. Thus the D.C. offset can cause a wrong decision to be made in the receiver concerning the transmitted symbol. In an I/Q-modulated signal, two consecutive symbols are combined into I and Q signals.

Thus I and Q signals are produced from the received signal in the I/Q demodulator, on the basis of which a decision is made in the receiver as to which symbol pair (00, 01, 10, 11) has been transmitted. The D.C. offset can occur in both I and Q signals, whereby a wrong decision can be made in the receiver as to the signal pair transmitted. In the worst case, even the error correction logic of the receiver cannot correct the information that has got a faulty expression.

There are some prior art solutions, in which an attempt is made to express the signal of the reception channel in spite of a high interfering D.C. offset. However, a drawback of these solutions is the fact that they only operate in situations in which the disturbing D.C. offset is constant or changes very slowly. In situations in which the powers of the signals in the adjacent channels vary quickly, the disturbing D.C. offset also changes quickly, whereby the prior art solutions are not capable of fully eliminating the disturbance caused by the D.C. offset. This is a typical situation in TDMA systems, for example.

The published solutions to eliminate the problem caused by the D.C. offset are mainly based on various DC filter applications. When a narrowband filter is used, the settling time becomes long, whereby the filter cannot react to quick changes of power. On the other hand, with a wideband filter it is possible to achieve a short settling time, but a filter of this kind also filters a substantial part of the useful signal, whereby the performance of the receiver is reduced.

The U.S. Pat. No. 5,212,826 presents a method for eliminating the D.C. offset in a manner such that, during the delay period of the receiver, the HF signal is prevented from entering the receiver, and the D.C. offset thus appearing in the receiver is measured. On the basis of the measurement, a constant correction voltage is produced and fed into the correction circuit of the receiver during the reception stage. A new measurement is performed during the next delay period, and a correction voltage corresponding to the new measured value is fed to the correction circuit during reception. A drawback of this method is, for example, the fact that the correction voltage is constant during the whole reception phase, and a HF signal is not fed to the receiver during the measurement, whereby the D.C. offset caused by the HF signal cannot be eliminated.

The British patent application GB 2 274 759 presents a method in which the D.C. offset is assessed by filtering from the demodulated baseband signal. This method can be applied primarily in cases in which the change of the offset voltage is substantially slower than the bit rate of the received signal.

In the prior art solutions, the correction of D.C. offset is based on a corrupted signal and possibly some advance information of the useful signal, but the source of the interference is not taken into account in the correction.

SUMMARY OF THE INVENTION

It is an object of the present invention to eliminate the above drawbacks and to achieve a method and a device for eliminating D.C. offset and gaining AM suppression particularly in direct conversion receivers. The invention is based on the idea that a correction signal is derived from the signal powers of the reception channels used, and the correction signal is added to the signals demodulated from the signals of the received channel. Thus the signals received from the output of the summers correspond to the original, desired signals as well as possible. The method according to the invention is characterized in that a correction signal ($Q_{control}$) is produced from the signals (R(t)) of the channels of the reception frequency band, and in that the correction signal is combined with the demodulated signal. The apparatus according to the invention is characterized in that the apparatus comprises means for producing a correction signal, and means for combining the correction signal with the received and demodulated signal.

In a method according to the first preferred embodiment of the invention, the correction signal is produced directly from the received HF signal.

In the second preferred embodiment of the invention, the correction signal is produced from a downconverted and prefiltered signal.

The invention provides considerable advantages compared to the methods and devices known at present. In a direct conversion receiver implemented with the method according to the invention, the compensation of the D.C. offset and the AM suppression is performed in real time, whereby even momentary and quick changes in the D.C. offset can be eliminated as well as possible. In this invention, knowledge of the adjacent signals and the interference caused by them is used for producing the correction voltage. In the second preferred embodiment the D.C. signal of the reception channel does not have an effect on the correction signal.

BRIEF DESCRIPTION OF THE DRAWING

In the following, the invention will be described in more detail with reference to the appended drawings, in which

FIG. **1** shows a simplified block diagram of a receiver according to the first preferred embodiment of the invention, in which the correction voltage is produced from the signal powers of the entire radio frequency band of the invention,

FIG. **2***a* shows a simplified block diagram of a receiver according to the second preferred embodiment of the invention, in which the correction voltage is produced from signal powers of the radio frequency spectrum of the system outside the received channel,

FIG. **2***b* shows an alternative construction of the I/Q demodulator as a simplified block diagram,

FIG. **3** shows a simplified block diagram of a receiver according to one preferred embodiment of the invention, in which a separate correction signal is produced for each demodulation branch, and

FIG. **4***a* shows a simplified diagram of the frequency spectrum of the reception frequency band of the radio communication system, and

FIG. **4***b* shows a simplified diagram of the frequency spectrum of the output port of the I/C demodulator.

DETAILED DESCRIPTION OF THE INVENTION

FIG. **1** shows a method according to the first embodiment of the invention for compensating the D.C. offset and for achieving AM-attenuation in the receiver. A power detector **17** has been added to the receiver, and a signal from the output of the HF amplifier **3** is led to the signal port and local oscillator port of the detector. The output of the HF amplifier **3** thus includes the signals in the reception channel of the whole system, that is, both the signal in the actual reception branch and the signals in other channels of the system. The mixing results in the output port of the third mixer are low-pass filtered and amplified, whereby there is a correction signal in the output of the third low-frequency amplifier **19**, and the correction signal is directed via an adapting device **23** to the summers **15**, **16**. The adapting device **23** adapts the amplitude and phase of the correction signal so that the compensation of the D.C. offset can be performed in the adders **15**, **16** as well as possible. However, in addition to the power of the signals of the adjacent channels, the correction signal also includes the power of the actual useful reception signal, therefore it overcompensates the interfering D.C. offset by the correction signal.

In a receiver according to preferred embodiments of the invention shown in FIGS. **1–3**, the received RF signal is directed via an antenna ANT to a passband filter **2**, the passband of which comprises a reception frequency band of the radio communication system in which the receiver is intended to be used. In a GSM system, for example, the reception frequency band is 925 to 960 MHz, which is divided into channels of 200 kHz. In the PCN system, the reception frequency band is 1805 to 1880 MHz, divided into channels of 200 kHz.

From the passband filter, the filtered signal is directed to the HF amplifier **3**. From the HF amplifier **3**, the signal is further directed to the I/Q demodulator **21**. The I/Q demodulator **21** comprises a power divider **4**, a first and a second mixer **7**, **10** and a phase shifter **22**. The phase shifter **22** produces two local oscillator frequencies LO_I/LO_Q from the local oscillator frequency produced by the local oscillator **8**, whereby the local oscillator frequencies produced have a phase difference of 90°. The power divider **4** divides the coming RF signal into two essentially identical signals having the same phase.

From the first output line **5** of the power divider, the RF signal is directed to the first mixer **7**, in which the local oscillator frequency LO_I of the reception channel frequency, coming from the first output line of the phase shifter **22** is mixed with the signal. The signal IF_I produced by the first mixer **7** is directed to the first low-pass filter **9**, in which all other signals except the baseband I signal (in-phase) received is filtered away from the signal.

A signal coming from the second output line **6** of the power divider **4** is taken to the second mixer **10**, in which a local oscillator frequency LO_Q, coming from the second output line of the phase shifter **22** at the reception channel frequency, which has a 90° phase offset compared to the local oscillator frequency LO_I to be directed to the first mixer **7**, is mixed with the signal. The mixing result IF_Q is directed to the second low-pass filter **11** and the high-pass filter **12**. The second low-pass filter **11** eliminates all other signals from the mixing result except the received, baseband frequency Q-signal (Quadrature phase).

The I/Q demodulator **21** can also be implemented by changing the places of the power divider **4** and the phase shifter **22** as shown in FIG. **2***b*, whereby the phase shifter **22** produces two identical signals with 90° phase difference from the radio frequency signal coming from the high-frequency amplifier **3**. Correspondingly, the power divider **4** uses the local oscillator frequency to produce two local oscillator frequencies LO_I, LO_Q, which are both at the same phase. Otherwise the operation is like in FIG. **2***a*. The alternative I/Q demodulator **21** shown in FIG. **2***b* can also be applied in the receivers shown in FIGS. **1** and **3**.

The baseband I and Q signals, which at this stage also include the D.C. offset caused by the signals in the adjacent channels, are amplified in the low-frequency amplifiers **13**, **14** and directed to the adders **15**, **16**. Here they are converted with the help of output signal of amplifier **19** derived from the power detector **17**.

The high-pass filter **12** removes the received, baseband signal from the signal produced by the second mixer **10**. The high-pass filtered signal is directed to a power detector **17**, which provides, the total power of the signals in the adjacent channels. The signal produced by the power detector **17** is low-pass filtered in the third low-pass filter **18** and amplified in the third low-frequency amplifier **19**. The third low-pass filter **18** eliminates all other signals except the baseband part from the signal produced by the power detector **17**.

The power detector **17** can consist of a mixer, for example, or it can be a simple diode power detector.

The output signal of the third low-frequency amplifier **19** is used as the correction signal in the adders **15**, **16**. An AM-attenuated I-signal is thus obtained from the output of the first adder **15**, in which signal the D.C. offset has been compensated. Correspondingly, an AM-attenuated Q-signal is obtained from the output of the second adder **16**, from which signal the D.C. offset has been compensated. The amplification of the small-signal amplifier **19** has been set so as to achieve maximum compensation of the D.C. offset.

The mixers **7**, **10** shown in the coupling of FIG. **2***a* are assumed to be identical, whereby the same correction signal can be used in both adders **15**, **16**. The correction signal has been formed from the signal produced by the second mixer **10**, but the correction signal can also be formed from the signal produced by the first mixer **7**. If the mixers **7**, **10** are not identical, the correction signal can be formed for the first adder **15** from the signal produced by the first mixer **7** by a correction circuit **12'**, **17'**, **18'**, **19'**, which is identical with the correction circuit **12**, **17**, **18**, **19** shown in FIG. **2***a*, as shown in FIG. **3**.

In practical applications some of the blocks shown in the couplings of FIGS. **1–3** can also be implemented as digital,

whereby the analog signal is converted into digital by an A/D converter. For the sake of clarity, the A/D converters are not shown in the figures, because their location depends on the implementation used in each case.

In the following, the operation of a method according to the invention is shown by way of calculation with reference to the coupling shown in FIG. **2***a* and to FIGS. **4***a* and **4***b*. The signal coming to the high-frequency amplifier **3** of the receiver **1** can be divided into two components:

$$R(t)=G(t)+I(t), \quad (1)$$

in which G(t) is the desired signal in the reception channel N, and I(t) includes the sum of the signals of all the channels **1**–(N–1), (N+1)–M in the passband area of the passband filter **2**. In FIG. **4***a* the passband area of the passband filter **2** is represented by the curve H_{BP}, and the curves $H_1, \ldots, H_M$ represent the channels **1**, **2**, . . . , M of the reception frequency band.

FIG. **4***b* shows a simplified frequency spectrum at the output port of the mixer **7**, **10**. Then the signal of the reception channel is at the baseband frequency, and the signals of the adjacent channels are at a higher frequency band. A curve H_{LP}, which depicts the frequency response of low-pass filtering and a curve H_{HP}, which depicts the frequency response of high-pass filtering are shown in FIG. **4***b*.

Because the isolation ϵ between the signal and local oscillator port of the mixer is not infinite, the signal R(t) coming to the signal port of the mixer is seen as attenuated also in the local oscillator port of the mixer, where it is superposed to the local oscillator signal LO(t). The local oscillator port of the mixer then, in fact, has the signal

$$L(t)=LO(t)+\epsilon[G(t)+I(t)]. \quad (2)$$

Then the output port of the mixer has the mixing results

$$IF(t)=[G(t)+I(t)]*[LO(t)+\epsilon[G(t)+I(t)]]=G(t)LO(t)+I(t)LO(t)+\epsilon[G^2(t)+I^2(t)+2G(t)I(t)], \quad (3)$$

where

G(t)LO(t)=the desired baseband signal,

I(t)LO(t)=all other channels of the system at a low intermediate frequency,

$\epsilon[G^2(t)+I^2(t)]$=dynamic D.C. offset, and

$\epsilon[2G(t)I(t)]$=intermodulation products.

The second term I(t)LO(t) of the formula (3), which represents the signals of the adjacent channels, is removed by low-pass filtering. The third term $\epsilon[G^2(t)+I^2(t)]$ represents the interfering D.C. offset, which varies with the power variations of the adjacent signals. The last term $\epsilon[2G(t)I(t)]$ represents the intermodulation products between the desired signal and the signals of the adjacent channels.

In practice, the intermodulation products $\epsilon[2G(t)I(t)]$ can be ignored. In connection with the formula (1) it was defined that G(t) is the desired signal which has a frequency between $0<f_G<f_{BB}$, and I(t) is limited between $f_{BB}<f_I<f_{RF}$, where f_{RF} is the width of the reception frequency band of the system. It is assumed that the mixer is sufficiently linear, whereby no considerable second and third order terms $I^2(t)$, $I^3(t)$ are produced, whereby only the intermodulation results of signals in the frequency band $f_{BB}<f_I<2f_{BB}$ have an effect in the desired baseband frequency area. In an ideal filter, the edge of the passband is vertical, whereby signals outside the passband do not get through the filter. In practical applications, however, it is not possible to make the edge of the passband completely vertical, whereby part of the signals outside the passband get through the filter. In this case, the power of the channels adjacent to the received channel must be limited in order to eliminate the intermodulation results. When applied in a GSM system, it has been found that with the mixer port isolation value $\epsilon<-24$ dB the last term of the formula (3) has no effect.

The frequency spectrum of the dynamic D.C. offset of the correction channel also includes the power contained in the desired signal, but multiplied by the port isolation ϵ, which is very small, and thus it causes only a very small error in the desired signal regardless of the intensities of the signals I(t) and G(t). If disturbing coupling only occurs within the mixer, it can be assumed that the attenuation coefficient ϵ is real. In practical applications, however, coupling also occurs between microstrips and external components, whereby the attenuation coefficient ϵ is complex and causes some phase offset between the dynamic, interfering D.C. offset and the correction signal amplified in the correction channel. In this case, the phase offset must be tuned before the correction signal is summed to the demodulated signals. This is shown in FIG. **3**, in which phase offset devices **20**, **20'** have been added to the demodulation branches.

As has been stated earlier in connection with the description, one correction channel is sufficient to produce a correction signal for both the I and Q signals, if the mixers **7**, **10** are identical. This can be proved as follows. The frequency spectrum of the correction signal is low-pass filtered, whereby only the signals $|\omega_{Aj}-\omega_{Ai}|<\omega_{BB}$ have an effect on the production of the correction signal, but these difference terms do not include the phase offset of the local oscillator frequencies. Ai and Aj represent channels that are in the reception frequency band. This can be easily proved mathematically by two sine waves A_1, ω_{A1} and A_2, ω_{A2}, which depict the amplitudes and frequencies of the adjacent channels, multiplied by the third sine wave ω_C, which represents the local oscillator frequency LO. The formula is:

Channel I

$$\begin{aligned} IF\_I &= \cos\omega_c t(A_1\cos\omega_{A1}t + A_2\cos\omega_{A2}t) \quad (4)\\ &= 1/2\,A_1[\cos(\omega_c-\omega_{A1})t + \cos(\omega_c+\omega_{A1})t] + \\ &\quad 1/2\,A_2[\cos(\omega_c-\omega_{A2})t + \cos(\omega_c+\omega_{A2})t] \end{aligned}$$

The summed terms $\omega_C+\omega_{A1}$ and $\omega_C+\omega_{A2}$ have such a high frequency that they are eliminated. The remaining terms are squared, whereby:

$$\begin{aligned} (IF\_I)^2 &= 1/4\,A_1^2\cos^2(\omega_c-\omega_{A1})t + 1/4\,A_2^2\cos^2(\omega_C-\omega_{A2})t + \quad (5)\\ &\quad 1/2\,A_1A_2[\cos[\omega_c-\omega_{A1})t * \cos(\omega_c-\omega_{A2})t]\\ &= 1/8\,A_1^2[1+\cos2(\omega_C-\omega_{A1})t] +\\ &\quad 1/8\,A_2^2[1+\cos2(\omega_C-\omega_{A2})t] +\\ &\quad 1/4\,A_1A_2[\cos(\omega_{A2}-\omega_{A1})t + \cos(2\omega_C-\omega_{A1}-\omega_{A2})t] \end{aligned}$$

The signals ω_{A1} and ω_{A2} represent the channels adjacent to the received channel, whereby

$|\omega_C-\omega_{A1}|>\omega_{BB}$, $|\omega_C-\omega_{A2}|>\omega_{BB}$ and $|2\omega_C-\omega_{A1}-\omega_{A2}|>\omega_{BB}$, where ω_{BB} is the bandwidth of the baseband frequency band. After the low-pass filtering, the correction signal obtained from the I-branch is:

$$I_{control}=\tfrac{1}{8}A_1^2+\tfrac{1}{8}A_2^2+\tfrac{1}{4}A_1A_2\cos(\omega_{A2}-\omega_{A1})t \quad (6)$$

Channel Q

$$IF\_Q = \sin\omega_C t(A_1\cos\omega_{A1}t + A_2\cos\omega_{A2}t) \quad (7)$$

$$= 1/2\,A_1[\sin(\omega_C-\omega_{A1})t + \sin(\omega_C+\omega_{A1})t +$$

$$1/2\,A_2[\sin(\omega_C-\omega_{A2})t +$$

$$\sin(\omega_C+\omega_{A2})t]$$

Similarly, like above in the formulas (4) and (5), the formula (7) is squared as follows:

$$(IF\_Q)^2 = 1/4\,A_1^2\sin^2(\omega_C-\omega_{A1})t + 1/4\,A_2^2\cos^2(\omega_C-\omega_{A2})t + \quad (8)$$

$$1/2\,A_1A_2(\sin(\omega_C-\omega_{A1})t * \sin(\omega_C-\omega_{A2})t]$$

$$= 1/8\,A_1^2[1-\cos2(\omega_C-\omega_{A1})t] +$$

$$1/8\,A_2^2[1-\cos2(\omega_C-\omega_{A2})t] +$$

$$1/4\,A_1A_2[\cos(\omega_{A2}-\omega_{A1})t -$$

$$\cos(2\omega_C-\omega_{A1}-\omega_{A2})t]$$

Further, considered that ω_{A1} and ω_{A2} represent the channels adjacent to the received channel, after the low-pass filtering the correction signal obtained from the Q-branch is:

$$Q_{control}=\tfrac{1}{8}A_1^2+\tfrac{1}{8}A_2^2+\tfrac{1}{4}A_1A_2\cos(\omega_{A2}-\omega_{A1})t \quad (9)$$

The phase offset of local oscillator frequencies LO_i, LO_Q occurs only in terms which include ω_C, but these terms are always outside the baseband frequency band ω_{BB} and are removed in low-pass filtering.

It can be seen from the above that the correction signals $I_{control}$ and $Q_{control}$ are the same, and so in this case the same signal can be used as the correction signal for both demodulation branches.

The correction channel includes information of the signal power in other channels. Particularly in a cellular mobile phone system, if the channels adjacent to the received channel contain a much stronger signal, it can be assumed that a stronger base station is available. Then the correction signal can also be used to assist in determining the need to change to another channel.

Although the invention has above been described as applied to a direct conversion receiver in which an I/Q demodulator is used, the method according to the invention can also be applied in other types of direct conversion receivers.

What is claimed is:

1. A method for compensating the D.C. offset and for obtaining spurious AM suppression from a signal (IF_I, IF_Q) received and demodulated in a channel of a reception frequency band in a radio communication system in a direct conversion receiver, comprising steps of:

detecting power of a signal received in a channel at the reception frequency band;

producing a correction signal ($Q_{control}$) from the signals (R(t)) of the channels of the reception frequency band by use of said power; and

combining the correction signal with the demodulated signal.

2. A method according to claim **1**, characterized in that the signals of all channels (R(t)) of the reception frequency band are used to produce the correction signal.

3. A method for compensating the D.C. offset and for obtaining spurious AM suppression from a signal (IF I, IF Q) received and demodulated in a channel of a reception frequency band in a radio communication system in a direct conversion receiver; wherein

a correction signal ($Q_{control}$) is produced from the signals (R(t)) of the channels of the reception frequency band, and the correction signal is combined with the demodulated signal; and

the correction signal is produced from the signals of the channels (I(t)) of the reception frequency band outside the received channel.

4. A method according to claim **1, 2**, characterized in that the power of the signals of the reception frequency band is used to produce the correction signal.

5. A method according to claim **1**, characterized in that the correction signal is summed to the received and demodulated signal.

6. A method according to claim **1**, characterized in that the received and demodulated signal is a signal of a digital radio communication system.

7. A method according to claim **1**, characterized in that the received and demodulated signal is an I/Q-modulated signal.

8. A method according to claim **1**, characterized in that the direct conversion receiver is a GSM receiver, and the reception frequency band is a reception frequency band of the GSM system.

9. A method for compensating the D.C. offset and for obtaining spurious AM suppression from a signal (IF I, IF Q) received and demodulated in a channel of a reception frequency band in a radio communication system in a direct conversion receiver; wherein

a correction signal ($Q_{control}$) is produced from the signals (R(t)) of the channels of the reception frequency band, and the correction signal is combined with the demodulated signal; and

the direct conversion receiver is a PCN receiver and the reception frequency band is a reception frequency band of the PCN system.

10. An apparatus for compensating the D.C. offset from the received and demodulated signal in a direct conversion receiver (**1**), which includes means for receiving and demodulating signals in the reception frequency band, characterized in that the apparatus also comprises:

means (**12, 17, 18, 19**) for producing a correction signal, and

means (**15, 16**) for combining the correction signal with the received and demodulated signal.

11. An apparatus according to claim **10**, characterized in that the means (**12, 17, 18, 19**) for producing a correction signal comprise a high-pass filter, a power detector (**17**), a third low-pass filter (**18**), and a third low-frequency amplifier (**19**), and that the means (**15, 16**) for combining the correction signal with the demodulated signal comprise at least one adder (**15, 16**).

12. An apparatus according to claim **10**, characterized in that the apparatus also comprises at least one AID converter, whereby the correction signal is produced at least partly digitally.

13. An apparatus according to claim **10**, characterized in that the direct conversion receiver (**1**) is a GSM receiver.

14. An apparatus according to claim **10**, characterized in that the direct conversion receiver (**1**) is a PCN receiver.

15. A method for compensating the D.C. offset and for obtaining spurious AM suppression from a signal (IF_I, IF_Q) received and demodulated in a channel of a reception frequency band in a radio communication system in a direct conversion receiver, characterized in that a correction signal ($Q_{control}$) is produced from the signals (R(t)) of the channels of the reception frequency band, and the correction signal is combined with the demodulated signal.

* * * * *

EXHIBIT D

US006292474B1

(12) **United States Patent**
Ali et al.

(10) **Patent No.: US 6,292,474 B1**
(45) **Date of Patent: Sep. 18, 2001**

(54) **MULTI-FREQUENCY BAND NYKTU-MODE RADIO RECEIVER AND ASSOCIATED METHOD HAVING SHARED CIRCUIT ELEMENTS**

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(73) Assignee: **Nokia Mobile Phones Limited**, Espoo (FI)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(22) Filed: **May 24, 1999**

(51) **Int. Cl.**[7] **H04J 13/00**; H04Q 11/00

(52) **U.S. Cl.** **370/328**; 370/335; 455/74; 455/143

(58) **Field of Search** 370/328, 465, 370/329, 335, 342; 455/74, 142, 143

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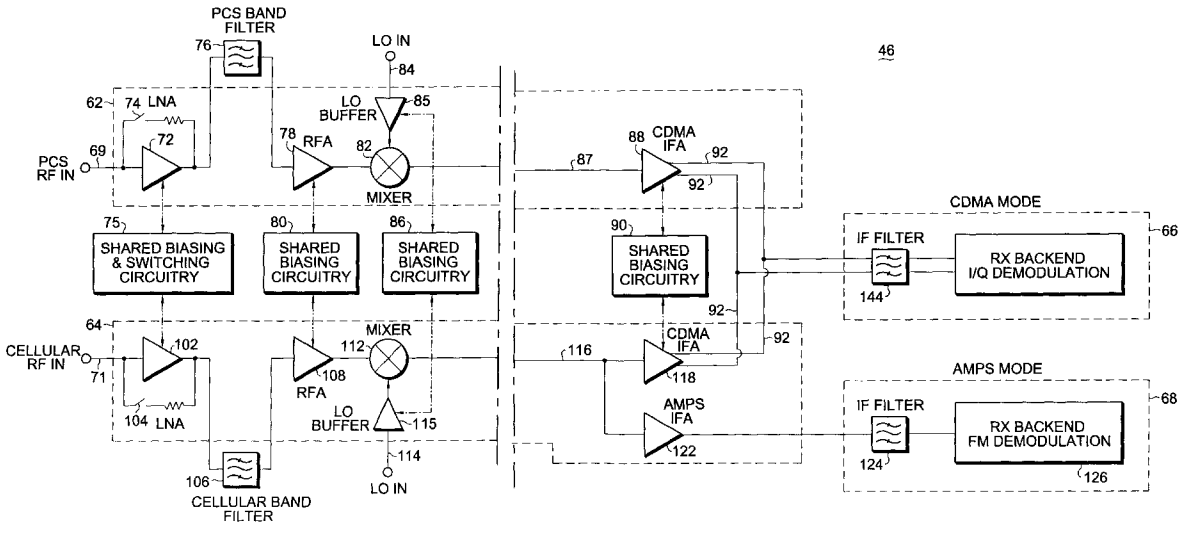
Primary Examiner—Melvin Marcelo
(74) *Attorney, Agent, or Firm*—Milan I. Patel

(57) **ABSTRACT**

Apparatus, and an associated method, for radio receiver circuitry operable in multi-modes to receive signals generated during operation of a multiple number of radio communication systems. The receiver circuitry is divided into receive chain portions which are selectably utilized depending upon which of the multiple number of the radio communication systems in which communications are to be effectuated. Selected combinations of the receive chain portions are formed, depending upon which of the modes in which the receiver circuitry is to be operable. Different combinations of the receive chain portions permit sharing of receive chain portions thereby to reduce the required number of circuit elements to form the multi-mode receiver circuitry. In one implementation, the radio receiver circuitry forms the receive portion of a dual-band, tri-mode mobile station operable in a selected one of three different cellular communication systems.

16 Claims, 4 Drawing Sheets



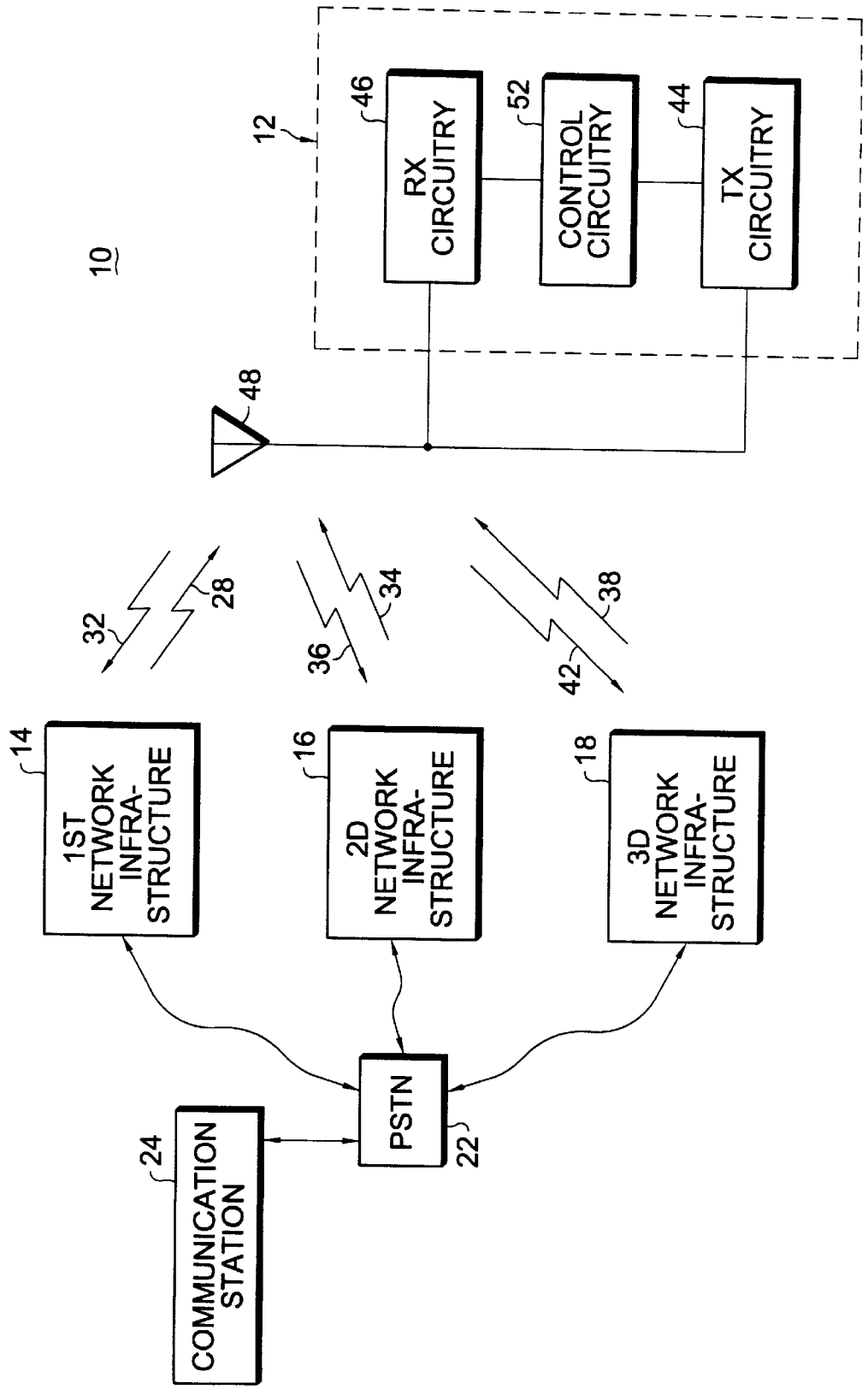

10
12
46
RX CIRCUITRY
52
CONTROL CIRCUITRY
44
TX CIRCUITRY
48
32
28
36
34
42
38
14
1ST NETWORK INFRA-STRUCTURE
16
2D NETWORK INFRA-STRUCTURE
18
3D NETWORK INFRA-STRUCTURE
PSTN
22
24
COMMUNICATION STATION

FIG. 1

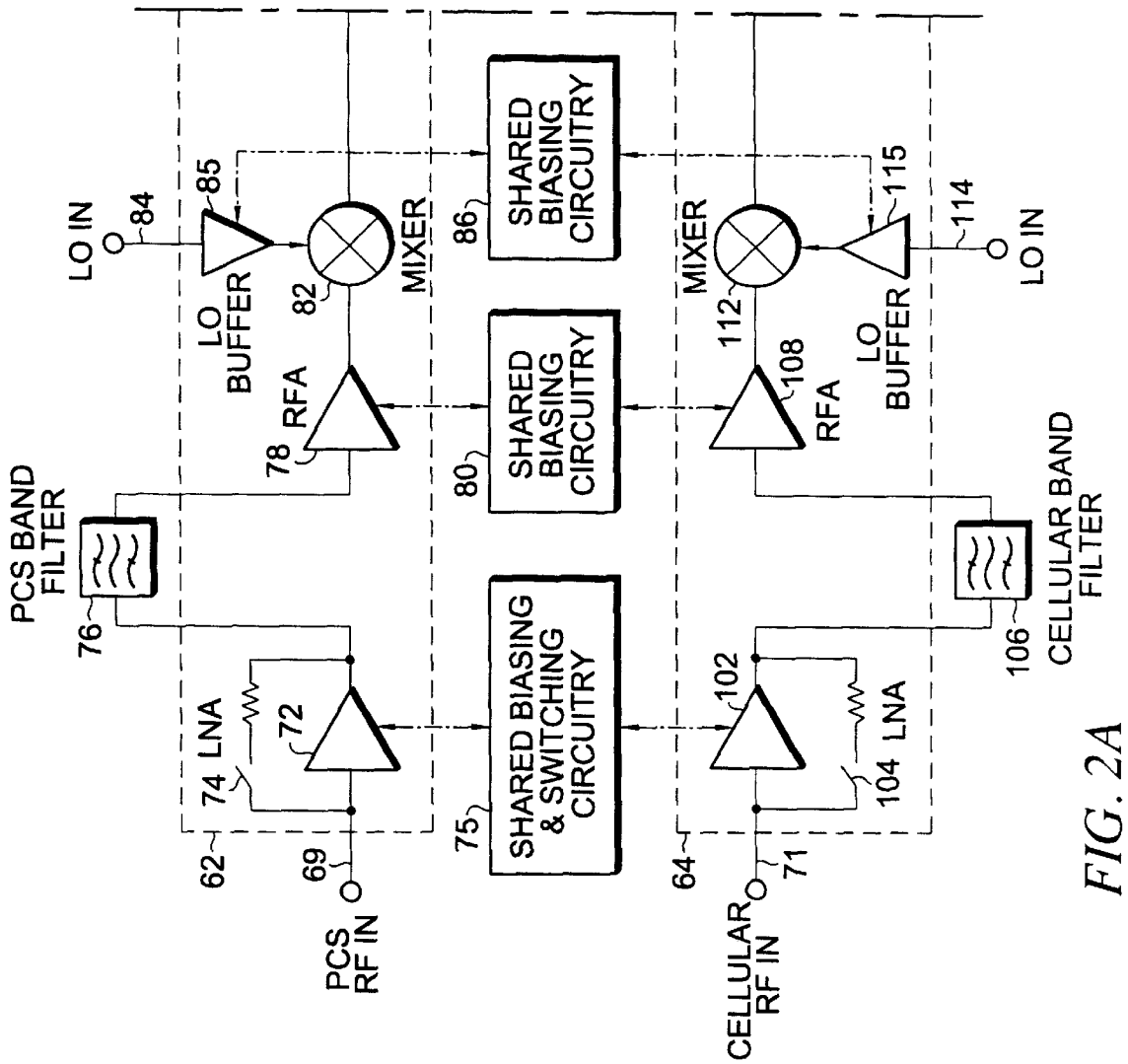

LO IN
84
85
LO BUFFER
82
MIXER
86
SHARED BIASING CIRCUITRY
MIXER
112
115
114
LO IN
LO BUFFER
RFA
78
80
SHARED BIASING CIRCUITRY
108
RFA
PCS BAND FILTER
76
CELLULAR BAND FILTER
106
74 LNA
72
SHARED BIASING & SWITCHING CIRCUITRY
102
104 LNA
62
69
75
64
71
PCS RF IN
CELLULAR RF IN

FIG. 2A

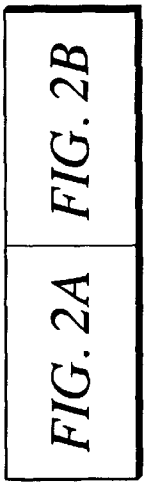


FIG. 2A
FIG. 2B

FIG. 2

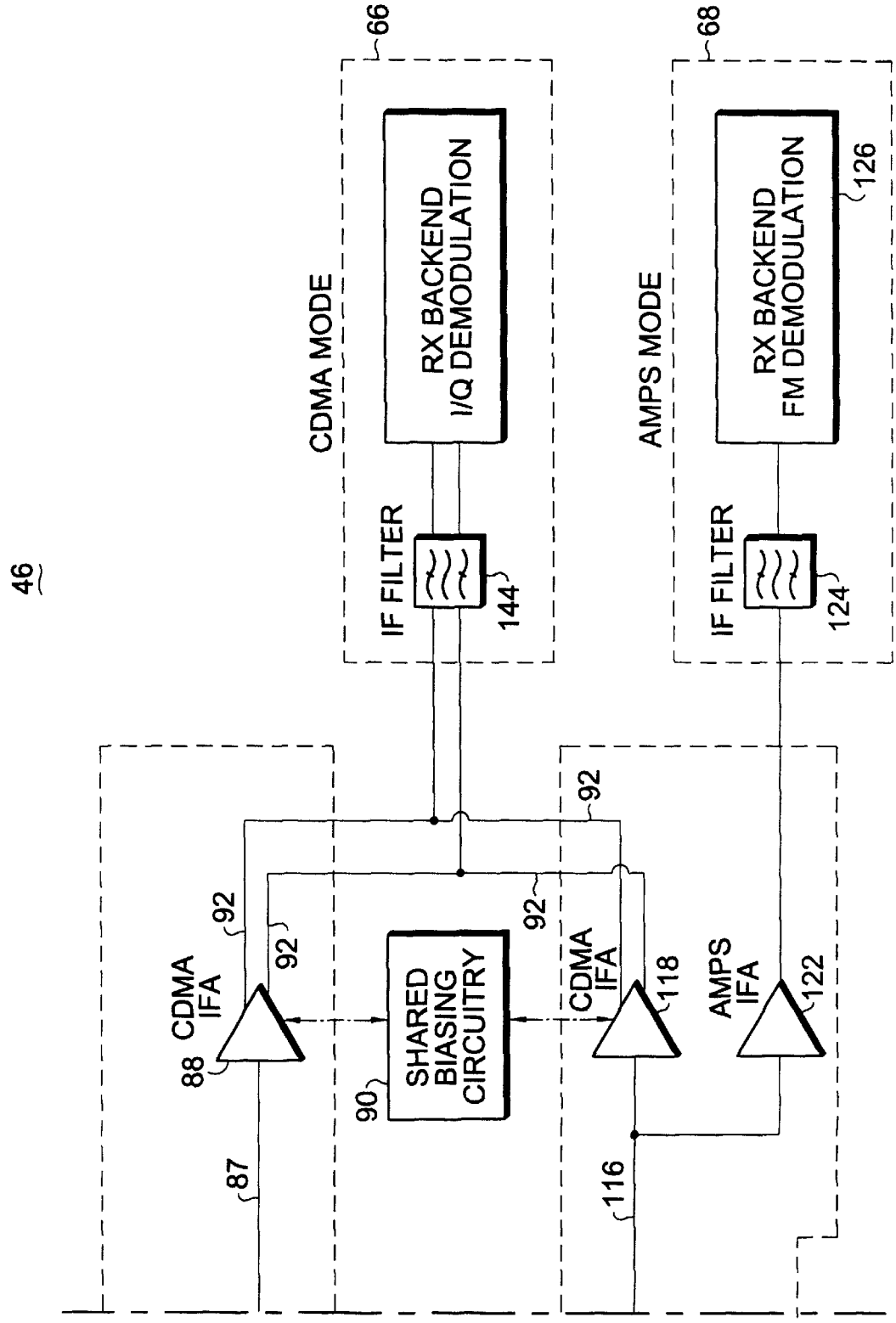

46
66
CDMA MODE
RX BACKEND I/Q DEMODULATION
IF FILTER
144
68
AMPS MODE
RX BACKEND FM DEMODULATION
126
IF FILTER
124
92
92
92
92
CDMA IFA
88
SHARED BIASING CIRCUITRY
90
CDMA IFA
118
AMPS IFA
122
87
116

FIG. 2B

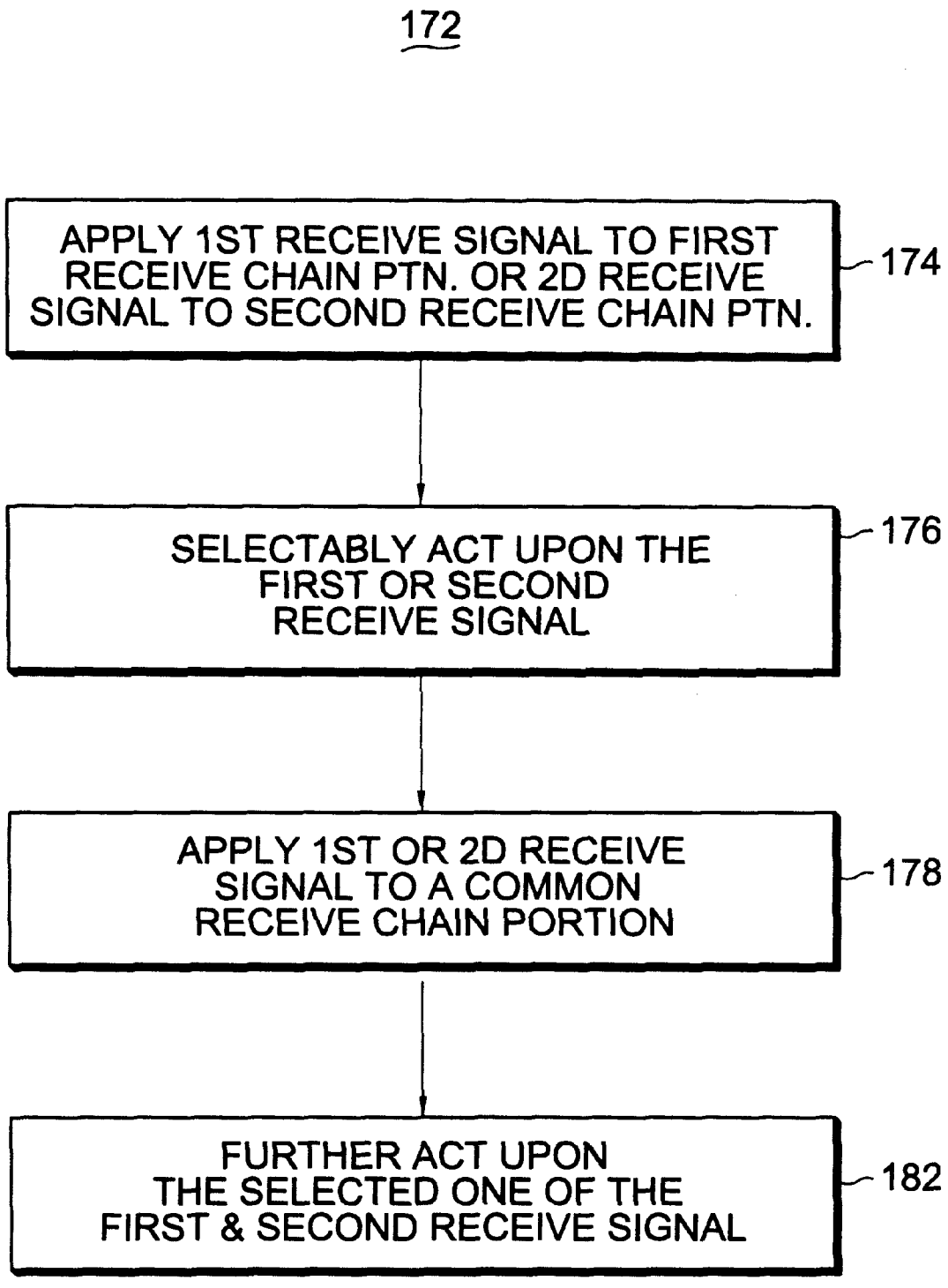

172
APPLY 1ST RECEIVE SIGNAL TO FIRST RECEIVE CHAIN PTN. OR 2D RECEIVE SIGNAL TO SECOND RECEIVE CHAIN PTN.
174
SELECTABLY ACT UPON THE FIRST OR SECOND RECEIVE SIGNAL
176
APPLY 1ST OR 2D RECEIVE SIGNAL TO A COMMON RECEIVE CHAIN PORTION
178
FURTHER ACT UPON THE SELECTED ONE OF THE FIRST & SECOND RECEIVE SIGNAL
182

FIG. 3

MULTI-FREQUENCY BAND NYKTU-MODE RADIO RECEIVER AND ASSOCIATED METHOD HAVING SHARED CIRCUIT ELEMENTS

The present invention relates generally to a radio device, such as a multi-mode mobile station selectively operable in more than one mobile communication system. More particularly, the present invention relates to a multi-mode radio receiver and an associated method, in which circuitry portions required for operation of the radio receiver in its different modes of operation are shared. By sharing the circuitry portions, cost-savings and size-savings are achieved.

BACKGROUND OF THE INVENTION

Information is communicated in a communication system between two or more communications stations. Information which is to be communicated between the communication stations is transmitted upon a communication channel formed to extend between the communication stations. In a two-way communication system, a communication station includes both a transmitter and a receiver operable to transmit and to receive, respectively, communication signals. Thereby in a two-way communication system, information is both transmitted and received at a single communication station.

A radio communication system is a communication system in which the communication channel formed between the communication channels is a radio channel defined upon a portion of the electromagnetic spectrum.

A radio communication system inherently increases communication mobility as communication channels defined in such a system are formed of radio channels and do not require wireline connections to form the communication channels. A radio communication system, however, typically is bandwidth-limited. That is to say, regulatory bodies which allocate usage of the electromagnetic spectrum allocate only a limited amount of the electromagnetic spectrum for communications in a particular radio communication system. Because the spectrum allocation for use by a particular system is limited, communication capacity increase of a radio communication system is limited by such allocation. Efforts are made, therefore, to construct a radio communication system in manners which efficiently utilize the allocated spectrum.

A PCS, or other mobile communication system is exemplary of a radio communication system. Mobile communication systems make relatively efficient use of the spectrum allocated thereto. Signals generated during operation of the mobile communication system are of relatively low power levels. Because of the use of low-power signals, the same channels can be reused throughout a mobile communication system according to a cell reuse plan. Concurrent use of the same channels is permitted according to the cell reuse plan, thereby to effectuate concurrent communications on the same channels by different communication station pairs at different locations throughout the area encompassed by the mobile communication system.

However, even with the relatively efficient utilization of the allocated spectrum, many mobile communication systems have been operated at their maximum capacities, particularly at certain-times-of-day and within certain cells of the mobile communication system. With technological advancements and the need to address the capacity problems of conventional mobile communication systems, various

mobile communication systems have been developed which permit increased capacities of communication therein.

In many instances, the mobile communication systems of such increased capacities require the installation of separate network infrastructures and the construction of separate mobile stations to be operable to communicate therewith. The separate network infrastructure are commonly overlaid upon existing mobile communication systems. And, mobile systems constructed according to different communication standards have been installed also in non-overlapping geographical areas. That is to say, different types of mobile communication systems are installed in different geographical areas. A mobile station operable pursuant in only one of the systems is operable only in the geographical area encompassed by such system.

Dual-mode mobile stations, for instance, are available to permit a user to communicate alternately by way of two different mobile communication systems. More generally, multi-mode mobile stations have been developed to permit their operation in multiple different mobile communication systems. Such dual- and multi-mode mobile stations typically must include circuitry specifically constructed for each of the different mobile communication systems in which the mobile station is operable. The various communication systems, for instance, are operable at different frequency bands, with different modulation schemes, with different coding schemes, etc. Therefore, conventional dual- and multi-mode mobile stations are sometimes to include separate, but functionally redundant, circuit paths for each of the communication systems in which the mobile station is to be operable.

Such duplication increases the complexity of the mobile station as well as the costs of the mobile station. And, because the redundant circuit paths each require separate circuit elements, the physical size of the resultant mobile station increases.

However, different ones of the mobile communication system standards sometimes exhibit some commonalities. For instance, the same modulation schemes are utilized but at different frequency ranges. Or, different modulation schemes might be utilized in the different communication systems but at the same range of frequencies.

For instance, an analog system such as AMPS (Advanced Mobile Phone System) is operable at a frequency range located about 800 MHz and utilizes an FDMA (Frequency Division Multiple Access) method. This system utilizes frequency modulation techniques to modulate information which is to be communicated during its operation. A digital systems such as PCS (Personal Communication System) which is operable at a frequency range of about 1.9 GHz utilizes various access methods, including a CDMA (code division, multiple-access). CDMA systems generally utilize QPSK (Quadrature Phase Shift Keying) modulation technique. Therefore, this same modulation technique is also utilized for CDMA systems operable at the cellular band of frequencies, i.e., the range located at about 800 MHz.

If advantage could be taken of the commonality of the different systems in which a multi-mode mobile station is to be operable, sharing of circuitry portions of the different circuit branches could be made. Such sharing would reduce the cost of the mobile station, along with permitting a reduction in the physical dimensions of the resultant mobile station.

It is in light of this background information related to radio devices, such as mobile stations operable in mobile communication systems, that the significant improvements of the present invention have evolved.

SUMMARY OF THE INVENTION

The present invention, accordingly, advantageously provides a manner by which to share circuitry portions required for operation of a multi-mode radio receiver. Circuitry portions, which conventionally form separate circuit chain portions, are shared in an embodiment of the present invention. By sharing the circuitry portions, the radio receiver is of less costly construction. And, because sharing of the circuitry portions results in a reduction of parts required of the radio receiver, a reduction in the physical dimensions required of the radio receiver is also provided.

In one aspect of the present invention, radio-frequency receive chain portions are used to act upon first receive signals and second receive signals generated during operation of a first mobile communication system and a second mobile communication system, respectively. The first and second mobile communication systems are operable over a common frequency band, thereby to permit the RF receive chain portion to be shared, operable to receive either the first receive signal or the second receive signal.

In another aspect of the present invention, a lower-frequency receive chain portion, for example, an IF (intermediate frequency) level or baseband level receive chain portion, is operable alternately to act upon indications of a first receive signal generated during operation of a first mobile communication system and a second receive signal generated during operation of a second mobile communication system. The first and second mobile communication systems are operable pursuant to a common modulation scheme, thereby to permit the lower-frequency receive chain portion to be used to act upon the indications of either the first or the second radio signals.

In yet another aspect of the present invention, a radio receiver of a trimode radio device is provided. The radio receiver is operable to receive and to act upon, a first radio signal generated by a first radio communication system, a second radio signal generated by a second radio communication system, and a third radio signal generated by a third mobile communication system. An RF receive chain portion is operable to act upon the radio signals generated by at least two of the radio communication systems. Thereby, a reduction in the required number of RF receive chain portions required of the tri-mode device is reduced. In analogous manner, a lower-frequency receive chain portion is selectively operable to act further upon indications of a receive signal generated by more than one of the radio communication systems. Thereby, the required number of lower-frequency, receive chain portions required of the tri-mode device is also reduced.

In an exemplary implementation, a dual-frequency band, tri-mode mobile station is provided. The mobile station is selectably operable in a PCS-CDMA communication system, an AMPS system, and a cellular-CDMA system. A first, RF receive chain portion is operable to act upon receive signals generated during operation of the PCS-CDMA system. The first, RF receive chain portion is operable also to down-convert such signal to an IF frequency. A second receive chain portion is operable to receive and to act upon receive signals generated during operation of the cellular-CDMA system and the AMPS system. The second RF receive chain portion is operable also to down-convert in frequency receive signals acted upon thereat to an IF frequency. Because the second RF receive chain portion acts upon signals generated during operation of two separate systems, a reduction in circuitry relative to conventional constructions of such a mobile station is achieved. The mobile station further includes a common receive chain portion coupled to both the first and second RF receive chain portions. The common receive chain portion acts upon indications of a selected one of the receive signals applied to, and acted upon, the first and second RF receive chain portions. The common receive chain portion includes a CDMA demodulator to demodulate the signals generated, alternatively, by the PCS-CDMA system and the cellular-CDMA system. Because the common receive chain portion acts upon signals generated by two separate communication systems, a reduction in circuitry is again achieved. The mobile station further includes a third receive chain portion coupled to the second RF receive chain portion, and selectably operable to act upon indications of the receive signal generated during operation of the AMPS system.

In yet another aspect of the present invention, biasing and switching circuitry is shared between the first and second RF receive chain portions. Because only one or the other of the RF receive chain portions is selected to be operable at a particular time period, such biasing and switching circuitry need only be coupled to the operable one of the RF receive chain portions. Additional reduction in circuitry required of the mobile station is thereby further achieved.

In these and other aspects, a multi-mode radio receiver, and an associated method is provided. The multi-mode radio receiver is operable to receive first receive signals generated during operation of a first radio communication system and to receive at least second receive signals generated during operation of at least a second radio communication system. A first receive chain portion has a front end side and a back end side. The front end side of the first receive chain portion is coupled to receive indications of the first receive signal. The first receive chain portion is selectably operable to act upon the indications of the first receive signal. A second receive chain portion has a front end side and a back end side. The front end side of the second receive chain portion is coupled to receive indications of the second receive signal. The second receive chain portion is selectably operable to act upon the indications of the second receive signal. Either one, but not both, of the first receive chain portion and the second receive chain portion are selected to be operable during a selected period. A common receive chain portion is coupled both to the back end side of the first receive chain and to the back end side of the second receive chain. The common receive chain acts further upon a selected one of the indications of the first receive signal and the indications of the second receive signal. The selected one corresponds to which of the first receive chain portion and the second receive chain portion is selected to be operable during the selected period.

A more complete appreciation of the present invention and the scope thereof can be obtained from the accompanying drawings which are briefly summarized below, the following detailed description of the presently-preferred embodiments of the present invention, and the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates a functional block diagram of a mobile station of an embodiment of the present invention positioned to transceive communication signals in three separate radio communication systems.

FIG. **2** illustrates a functional block diagram of a portion of the mobile station shown in FIG. **1** of an embodiment of the present invention.

FIG. **3** illustrates a method flow diagram listing the method of operation of an embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring first to FIG. **1**, a communication arrangement, shown generally at **10**, includes a multi-mode mobile station **12** capable of transceiving communication signals with a plurality, here three, radio communication systems. In the exemplary implementation, the mobile station **12** forms a dual-band, tri-mode, cellular mobile station selectably operable in three separate mobile communication systems. While the following description shall describe the mobile station **12** with respect to such an implementation, it should be understood that other embodiments of the present invention can analogously be implemented to be operable in other types of communication systems.

Three separate network infrastructures, a first network infrastructure **14**, second network infrastructure **16**, and a third network infrastructure **18** are installed and are permitting of radio communications with the mobile station **12** when the mobile station is positioned in a geographical area encompassed by the network infrastructure of the respective communication systems. The separate network infrastructures may be overlaid, or partially overlaid, upon one another. Or, the network infrastructure may be installed at separate geographical areas, and the mobile station communicates with the respective one of the separate radio communication systems when the mobile station is positioned in the geographical area encompassed by such respective communication system.

The network infrastructure **14** is here representative of a PCS-band, CDMA (code division, multiple-access) mobile communication system operable at approximately 1.9 GHz. The network infrastructure **16** is representative of a cellular-band, CDMA mobile communication system operable at about 800 MHz. And, the network infrastructure **18** is representative of the network infrastructure of a cellular-band, AMPS (advanced mobile phone service) mobile communication system operable also at about 800 MHz. It should be noted that the terminology of cellular and mobile shall be, at times, used interchangeably herein.

The network infrastructure **14–18** of the respective communication systems are coupled to a PSTN (public-switched, telephonic network) **22**, in conventional manner. A communication station **24** is also shown to be coupled to the PSTN. The communication station **24** is exemplary of a communication station with which communications can be effectuated with the mobile station.

During operation of the first cellular communication system, communication signals are transceived between the network infrastructure **14** and the mobile station. Here, first downlink communication signals **28** and first uplink signals **32** are representative of the signals communicated between the network infrastructure and the mobile station. Analogously, during operation of the second cellular communication system, communication signals are transceived between the network infrastructure **16** and the mobile station **12**. Here, second downlink communication signals **34** and second uplink communication signals **36** are representative of communication of the signals between the network infrastructure and the mobile station. And, during operation of the third cellular communication system, communication signals are transceived between the network infrastructure **18** and the mobile station **12**. Here, third downlink communication signals **38** and third uplink communication signals **42** are representative of signals communicated during operation of the third cellular communication system.

The mobile station **12** is here shown to include transmitter circuitry **44** and receiver circuitry **46**. Information sourced at the mobile station is acted upon by the transmitter circuitry and transduced by an antenna transducer **48** to form, selectably, the uplink communication signals, **32**, **36**, and **42**, as appropriate. And, when any of the first, second and third downlink communication signals **28**, **34**, and **38** are detected at the transducer **48** and converted in electrical form to be applied to the receiver circuitry **46**, the receiver circuitry is selectably operable to act upon the signals applied thereto.

The mobile station **12** is further shown to include control circuitry **52** operable to control operation of the transmitter and receiver circuitry **44** and **46**, respectively. The control circuitry controls operation of the respective circuitry to cause operation of the mobile station in a selected one of the different cellular communication systems with which the mobile station **12** is operable. By appropriate control over which of the communication systems with which the mobile station is operable, an available one, or a desired one, of the cellular communication systems, is caused to be utilized by the mobile station.

FIG. **2** illustrates the receiver circuitry **46** of an embodiment of the present invention. In the exemplary implementation, the receiver circuitry **46** forms a portion of the mobile station **12** of a dual-band, tri-mode mobile station. While the circuitry **46** of the exemplary implementation shown in the Figure is representative of the circuitry of such a device, in other implementations, the receiver circuitry is alternately configured to be operable in selected communication systems, as appropriate.

The receiver circuitry **46** here includes a first receive chain portion **62**, a second receive chain portion **64**, a common receive chain portion **66**, and a third receive chain portion **68**.

The first receive chain portion **62** includes a front end side coupled to the antenna transducer **48** (shown in FIG. **1**), thereby to receive indications of the first downlink communication signal **28** (shown in FIG. **1**), when detected at the mobile station of which the receiver circuitry forms a portion. The indications are applied to the portion **62** on the line **69**, here indicated as "PCS RF In." Analogously, the second receive chain portion **64** also includes a front end side, also coupled to the antenna transducer (shown in FIG. **1**), thereby to receive indications of the second downlink communication signal **34** (shown in FIG. **1**). The indications are applied to the portion **64** on the line **71**, here indicated as "CELLULAR RF In." The first and second receive chain portions **62** and **64** further define back end sides to which the common receive chain portion **66** is coupled. The first and second receive chain portions are coupled to the common receive chain portion in a wired-OR configuration in which indications of either the first receive signal, once acted upon by the first receive chain portion, or indications of the second receive chain portion once acted upon by the second receive chain portion are provided to the common receive chain portion to be acted further upon thereat.

The third receive chain portion **68** is also coupled to the back end side of the second receive chain portion **64** and is selectably operable, alternate to operation of the common receive chain portion.

The first receive chain portion **62** forms an RF (radio frequency)-stage of a PCS-band receive operable at about 1.9 GHz. Indications of the first receive signal, detected at the antenna transducer **48** and converted into electrical form thereat, are provided to a low-noise amplifier (LNA) **72**. The LNA **72** is a switched amplifier which permits bypassing of the amplifier if determinations are made that amplification at the LNA is unnecessary. Such switching is performed by a

switch element **74**. Selection of the switch position of the switch element **74** is made by biasing and switching circuitry **75** to position the switch element **74** in a desired switch position. The LNA **72** is coupled to a PCS-band filter **76** which has a passband to pass signal frequency within the PCS passband. Signal frequencies passed by the filter **76** are applied to an RF amplifier **78** to be amplified thereat. The amplifier **78** is biased by shared biasing circuitry **80**. Once amplified, the signal is provided to a first input of a mixer **82**. A down mixing signal, the "LO In" signal, generated on the line **84** is applied to a second input of the mixer **82** by way of an isolating buffer **85**. The buffer **85** is biased by shared biasing circuitry **86**. The mixer operates as a down-mixer to down-convert in frequency the amplified signal applied to the first input of the mixer to form an IF (intermediate frequency)-frequency signal on the line **87** extending from an output of the mixer. The IF signal is applied to an IF-stage amplifier **88**, here a differential amplifier. The amplifier is biased by shared biasing circuitry **90**. Differential, amplified signals are generated on the lines **92**, and the lines **92** are connected to the common receive chain portion **66**.

The second receive chain portion **64** forms an RF-stage of a cellular-band receiver operable at cellular frequencies of about 800 MHz. Indications of the second downlink signals detected at the antenna transducer **48** and converted into electrical form thereat are applied to an input of a low-noise amplifier (LNA) **102**. The LNA **102** is a switched amplifier which permits bypassing of the amplifier if determinations are made that amplification at the LNA is unnecessary. Such switching is performed by a switch element **104**. Selection of the switch position of the switch element **104** is made by the shared biasing and switching circuitry **75**. The LNA **102** is coupled to a cellular band filter **106** having a passband to pass signal frequencies within a cellular band of approximately 800 MHz. Signal frequencies passed by the filter **106** are amplified by an RF amplifier **108**. The amplifier **108** is biased by biasing circuitry **80**. Amplified signals are applied to a first input of a mixer **112**. A down-mixing signal, the "LO In" signal, generated on the line **114** is applied to a second input of the mixer **112** by way of an isolating buffer **115**. The buffer **115** is biased by shared biasing circuitry **86**. The mixer **112** is operable to down-convert the indications of the second receive signal applied to the first input of the mixer in frequency to an IF frequency. An IF signal is formed on the line **116** at an output of the mixer **112**. The line **116** is coupled to an input of a differential amplifier **118** operable to generate amplified signals on the line **92**. The amplifier is biased by the shared biasing circuitry **90**. The lines **92** are connected to the common receive chain portion **66**.

The line **116** is also coupled to an input of an amplifier **122**. The amplifier **122**, an output line of which is coupled to the third receive chain portion **68**. The amplifier is selectably operable to amplify the IF signal formed on the line **116** and to apply such signal, once amplified, to an IF filter **124**. Signal frequencies within the passband of the filter **124** are applied to a receiver backend FM Demodulation element **126**. The element **126** performs functions such as baseband down conversion and demodulation operations. The FM demodulation can be performed by digital or analog methods.

The lines **92**, connected to the differential outputs of the IF amplifiers **88** and **118** of the first and second receive chain portions **62** and **64**, respectively, are coupled to an IF filter **144** which forms a portion of the common receive chain portion **66**. The filter **144** exhibits a passband corresponding to the passband to pass signal frequencies of CDMA signals generated during operation of a cellular, CDMA system, either of those operable at a PCS-band frequency or operable at a cellular-band frequency. Signal frequencies passed by the filter **144** are applied to a receiver backend I/Q Demodulation element **146**. The element **146** performs functions such as baseband down conversion and demodulation operations.

The receiver circuitry **46** shown in the Figure is of reduced circuit element count relative to conventional such constructions because circuit paths are shared amongst the circuit paths required for operation of the different mode of which the mobile station is operable. Advantage is taken of the fact that the mobile station is operable in a single mode at a time. That is to say, when the mobile station is operable to communicate pursuant to the first communication network, here a PCS-band, CDMA system, only the circuit path relating to that communication system is operable. In one implementation, the IF-stage amplifiers **88**, **118**, and **122**, are selectably powered. Such selective powering of the amplifiers is determinative of operation of the receiver circuitry.

When the mobile station of which the receiver circuitry forms a portion is to be operable in a PCS-band, CDMA mode, the IF-stage amplifier **88** is powered while the amplifiers **118** and **122** are not powered. Thereby, a receive chain, formed of the receive chain portion **62** and the common receive chain portion **66** acts upon signals received at the mobile station. When, conversely, the mobile station is to be operable in the cellular-band, CDMA mode, the amplifier **118** is caused to be powered while the amplifiers **88** and **122** are caused not to be powered. Thereby, the second receive chain portion **64** and the common receive chain portion **66** form a receive chain which acts upon the signals received at the mobile station. And when the mobile station is to be operated in a cellular-band, AMPS mode, the amplifier **122** is caused to be powered, and the amplifiers **88** and **118** are caused not to be powered. Thereby, the second receive chain portion **64** and the third receive chain portion **68** form a receive chain for acting upon signals received at the mobile station. In other implementations, other manners are used by which to selectably connect the different portions **62**, **64**, **66**, and **68** to form a receive chain, operable as desired. In similar manner, the shared circuitry **75**, **80**, **86**, and **90** is operable with a selected one of the first receive chain portion with a second receive chain portion. Circuit element-count is thereby reduced, relative to conventional constructions of the receiver circuitry **48**.

FIG. **3** illustrates a method, shown generally at **172**, of an embodiment of the present invention. The method selectably acts upon a first receive signal and at least a second receive signal when received at a multimode radio receiver operable to receive first receive signals generated during operation of a first radio communication system and to receive at least second receive signals generated during operation of at least a second radio communication system.

First, and as indicated by the block **174**, indications of the first receive signal, if received at the multi-mode receiver, are applied to a first receive chain portion. And, indications of the second receive signal, if received at the multi-mode receiver, are applied to a second receive chain portion.

Then, and as indicated by the block **176**, the indications of the first receive signal are selectably acted upon at the first receive chain portion, and the indications of the second receive signal are selectably acted upon at the second receive chain portion. Either one, but not both, of the first receive chain portion and the second receive chain portion are operable during the selected period.

Then, and as indicated by the block **178**, indications of a selected one of the indications of the receive signal and the indication of the second receive signal are applied to a common receive chain portion. And, as indicated by the block **182**, the indications of the selected one of the indications of the first and second receive signal, applied to the common receive chain portion are further acted upon.

The previous descriptions are of preferred examples for implementing the invention, and the scope of the invention should not necessarily be limited by this description. The scope of the present invention is defined by the following claims.

We claim:

1. A multi-mode radio receiver operable to receive first receive signals generate during operation of a first radio communication system and to receive at least second receive signals generated during operation of at least a second radio communication system, said multi-mode radio receiver comprising:

a first receive chain portion having a front end side and a back end side, the front end side of said first receive chain portion coupled to receive indications of the first receive signal, said first receive chain portion having at least a first amplifier, the first amplifier selectably biased to cause said first receive chain portion to act upon the indications of the first receive signal;

a second receive chain portion having a front end side and a back end side, the front end side of said second receive chain portion coupled to receive indications of the second receive signal, said second receive chain portion having at least a second amplifier, the second amplifier selectably biased to cause said second receive chain portion to act upon the indications of the second receive signal, either one, but not both, of said first receive chain portion and said second receive chain portion selected to be operable during a selected period;

shared circuitry coupled to both said first receive chain portion and to said second receive chain portion, said shared circuitry alternately operable with said first receive chain portion to from a portion thereof and with said second receive chain portion to form a portion thereof, said shared circuitry including amplifier biasing and switching circuitry for biasing a selected one of the first amplifier and the at least the second amplifier; and

a common receive chain portion coupled both to the back end side of said first receive chain portion and to the back end side of said second receive chain portion, said common receive chain portion for acting further upon a selected one of the indications of the first receive signal and the indications of the second receive signal, the selected one corresponding to which of said first receive chain portion and said second receive chain portion is selected to be operable during the selected period.

2. The multi-mode radio receiver of claim **1** wherein said first receive chain portion and said second receive chain portion each comprises an RF (radio frequency)-stage for acting upon the indications of the first receive signal and upon the indications of the second receive signal, respectively, when at radio frequencies, and wherein said common receive chain portion comprises an IF (intermediate frequency)-stage for acting upon the selected one of the indications of the first receive signal and of the second receive signal, respectively, when at intermediate frequencies.

3. The multi-mode radio receiver of claim **2** wherein said common receive chain portion further comprises an intermediate-stage for acting upon the selected one of the indications of the first receive signal and of the second receive signal, when at baseband frequencies.

4. The multi-mode radio receiver of claim **2** wherein the first receive signal is of a bandwidth within a first range of frequencies, wherein the second receive signal is of a bandwidth within a second range of frequencies, said first receive chain portion operable at the first range of frequencies, and said second receive chain portion operable at the second range of frequencies.

5. The multi-mode receiver of claim **4** wherein the first radio communication system comprises a first cellular communication system operable at the first range of frequencies according to a first modulation scheme, wherein the second radio communication system comprises a second cellular communication system operable at the second range of frequencies according also to the first modulation scheme, said first receive chain portion having a first down-converter for down-converting the indications of the first receive signal to an IF (intermediate frequency) range, and said second receive chain portion having a second down-converter for down-converting the indications of the second receive signal to the IF range.

6. The multi-mode receiver of claim **5** wherein said first amplifier further comprises a first IF amplifier for selectively amplifying the indications of the first receive signal once down-converted by the first down-converter to the IF range, wherein said second amplifier further comprises a second IF amplifier for selectively amplifying the indications of the second receive signal once down-converted by the second down-converter to the IF range, the first amplifier and the second IF amplifier alternately operable, and wherein the selected one of the indications of the first receive signal and the indications of the second receive signal upon which said common receive chain further acts upon is determined by which of the first IF amplifier and the second IF amplifier is operable.

7. The multi-mode receiver of claim **1** wherein the at least second receive signals generated during operation of the at least second radio communication system comprises the second receive signals generated during operation of the second radio communication system and at least third receive signals generated during operation of at least a third radio communication system, said second receive chain portion further selectably operable to act upon indications of the third receive signals, said multi-mode receiver further comprising a third receive chain portion coupled to the back end side of said second receive chain portion, said third receive chain portion selectably operable further to act upon the indications of the third receive signal, said third receive chain portion operable alternate to operation of said common receive chain portion.

8. The multi-mode receiver of claim **7** herein said second receive chain portion comprises an RF (radio frequency)-stage for selectably acting upon the second receive signal and the third receive signal, respectively, at radio frequencies, and wherein said third receive chain portion comprises an IF (intermediate frequency)-stage for selectably further operating upon the indications of the third receive signals at intermediate frequencies.

9. The multi-mode radio receiver of claim **8** wherein the first receive signal is of a bandwidth within a first range of frequencies, wherein the second receive signal is of a bandwidth within a second range of frequencies, and wherein the third receive signal is of a bandwidth also within

the second range of frequencies, said first receive chain portion operable at the first range of frequencies, and said second receive portion operable at the second range of frequencies.

10. The multi-mode receiver of claim **9** wherein the first radio communication system comprises a first cellular communication system operable at the first range of frequencies according to a first modulation scheme, wherein the second radio communication system comprises a second cellular communication system operable at the second range of frequencies according also to the first modulation scheme, and wherein the third radio communication system comprises a third cellular communication system operable pursuant to a second modulation scheme, said first receive chain portion having a first down-converter for down-converting the indications of the first receive signal to an IF (intermediate frequency)-range and said second receive chain portion having a second down-converter for down-converting the indications of the second receive signal to the IF range.

11. The multi-mode receiver of claim **10** wherein the first cellular communication system comprises a CDMA (code division, multiple-access) system operable at a PCS (personal communication system) frequency range, wherein the second cellular communication system comprises a CDMA (code division, multiple-access) system operable at a cellular-band frequency range, and wherein the third cellular communication system comprises an AMPS (Advanced Mobile Phone Service) system operable at the cellular-band frequency range, said common receive chain portion having CMDA demodulation elements and said third receive chain portion having AMPS demodulation elements.

12. The multi-mode receiver of claim **10** wherein the first amplifier of said first receive chain portion further comprises a first IF amplifier for selectively amplifying the indications of the first receive signal once down-converted by the first down-converter, wherein the at least second amplifier of said second receive chain portion further comprises a second IF amplifier for selectively amplifying the indications of the second receive signal once down-converted by the second down-converter, and a third IF amplifier for amplifying the indications of third receive signal once down-converted by the second down-converter, a selected one of the first amplifier, the second amplifier, and the third amplifier operable during the selected period.

13. The multi-mode receiver of claim **12** wherein the second IF amplifier of said second receive chain portion includes a front end side coupled to the second down-converter and wherein the third IF amplifier of said third receive chain portion includes a front end side coupled to the second down-converter of said second receive chain portion.

14. The multi-mode receiver of claim **7** having a first integrated circuit element and a second integrated circuit element, said first receive chain portion disposed at said first integrated circuit element, and said first receive chain portion, said common receive chain portion, and said third receive chain portion disposed at said second integrated circuit element.

15. In a method for operating a multi-mode radio receiver operable to receive first receive signals generated during operation of a first radio communication system and to receive at least second receive signals generated during operation of at least a second radio communication system, an improvement of a method for selectively acting upon the first receive signal and the at least second receive signal when received at the multi-mode radio receiver, said method comprising:

applying indications of the first receive signal, if received at the multimode receiver, to a first receive chain portion and indications of the second receive signal, if received at the multi-mode receiver, to a second receive chain portion, the first receive chain portion having at least a first amplifier and the second receive chain portion having at least a second amplifier;

selectably biasing a selected one of the first amplifier and the second amplifier, thereby selectably to cause the indications of the first receive signal to be acted upon by the first receive chain portion and the indications of the second receive signal to be acted upon by the second receive chain portion, either one, but not both, of the first receive chain portion and the second receive chain portion operable during a selected period;

applying indications of selected one of the indications of the first receive signal and the indications of the second receive signal to a common receive chain portion, subsequent to actions performed thereon during said operation of selectably acting; and

further acting upon the indications of the selected one of the indications of the first receive signal and the second receive signal, respectively, applied to the common receive chain portion.

16. The method of claim **15** wherein the multi-mode radio receiver is further operable to receive third receive signals generated during operation of a third radio communication system, wherein said operation of applying the indications of the first receive signal the first receive chain portion and the indications of the second receive signal portion to the second receive chain portion further comprises applying indications of the third receive signals, if received at the multi-mode receiver, to the second receive chain portion, wherein the second receive chain portion further has a third amplifier and wherein said operation of selectably biasing further comprises selectably biasing the third amplifier, thereby further selectably to cause the indications of the third receive signal at the second receive chain portion.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,292,474 B1
DATED : September 18, 2001
INVENTOR(S) : Fazal Ali, et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title page,
Item [54], Delete "**NYKTU-MODE** " and insert -- **MULTI-MODE** --.

Signed and Sealed this

Twenty-eighth Day of May, 2002

Attest:

Attesting Officer

JAMES E. ROGAN
Director of the United States Patent and Trademark Office

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,292,474 B1
APPLICATION NO. : 09/317660
DATED : September 18, 2001
INVENTOR(S) : Ali et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

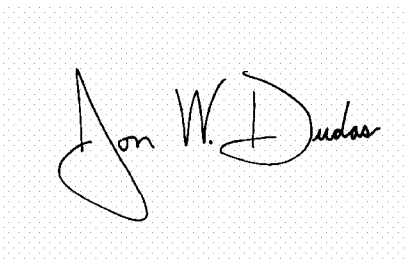
Column 9,
Line 15, "generate" should read -- generated --;
Line 41, "from" should read -- form --.

Column 11,
Line 42, "indications of third receive signal" should read -- indications of the third receive signal --.

Column 12,
Line 43, "first receive signal the first receive chain portion" should read -- first receive signal to the first receive chain portion --.

Signed and Sealed this

Twentieth Day of June, 2006



JON W. DUDAS
Director of the United States Patent and Trademark Office

EXHIBIT E

US006714091B2

(12) **United States Patent**
Norskov et al.

(10) **Patent No.: US 6,714,091 B2**
(45) **Date of Patent: Mar. 30, 2004**

(54) **VCO WITH PROGRAMMABLE OUTPUT POWER**

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(73) Assignee: **Nokia Mobile Phones Limited**, Espoo (FI)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/739,230**

(22) Filed: **Dec. 19, 2000**

(65) **Prior Publication Data**

US 2001/0011928 A1 Aug. 9, 2001

(30) **Foreign Application Priority Data**

Dec. 21, 1999 (GB) 9930241

(51) **Int. Cl.**[7] **H03B 5/24**

(52) **U.S. Cl.** **331/185**; 331/182; 331/186; 331/74

(58) **Field of Search** ..... 331/1 R, 74, 185, 331/186, 175, 182; 323/282

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(74) *Attorney, Agent, or Firm*—Antonelli, Terry, Stout & Kraus, LLP

(57) **ABSTRACT**

Voltage controlled oscillator assembly which includes at least one voltage controlled oscillator, and a regulator for regulating the output power from the at least one voltage controlled oscillator.

13 Claims, 2 Drawing Sheets

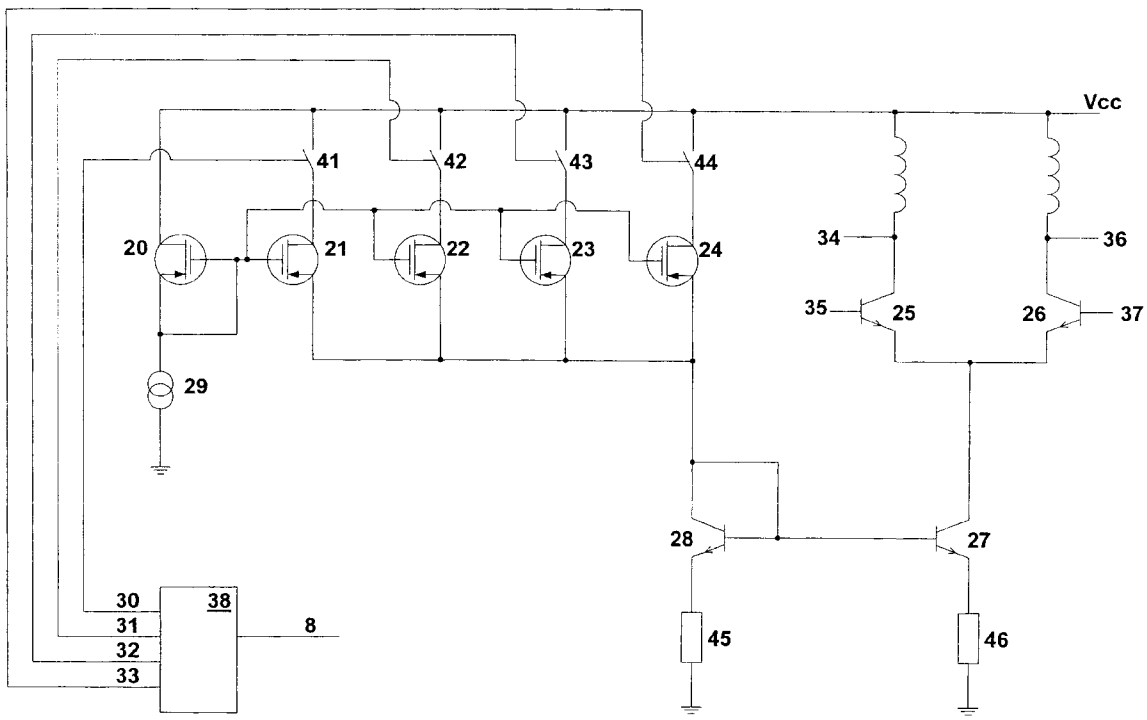

FIG. 1

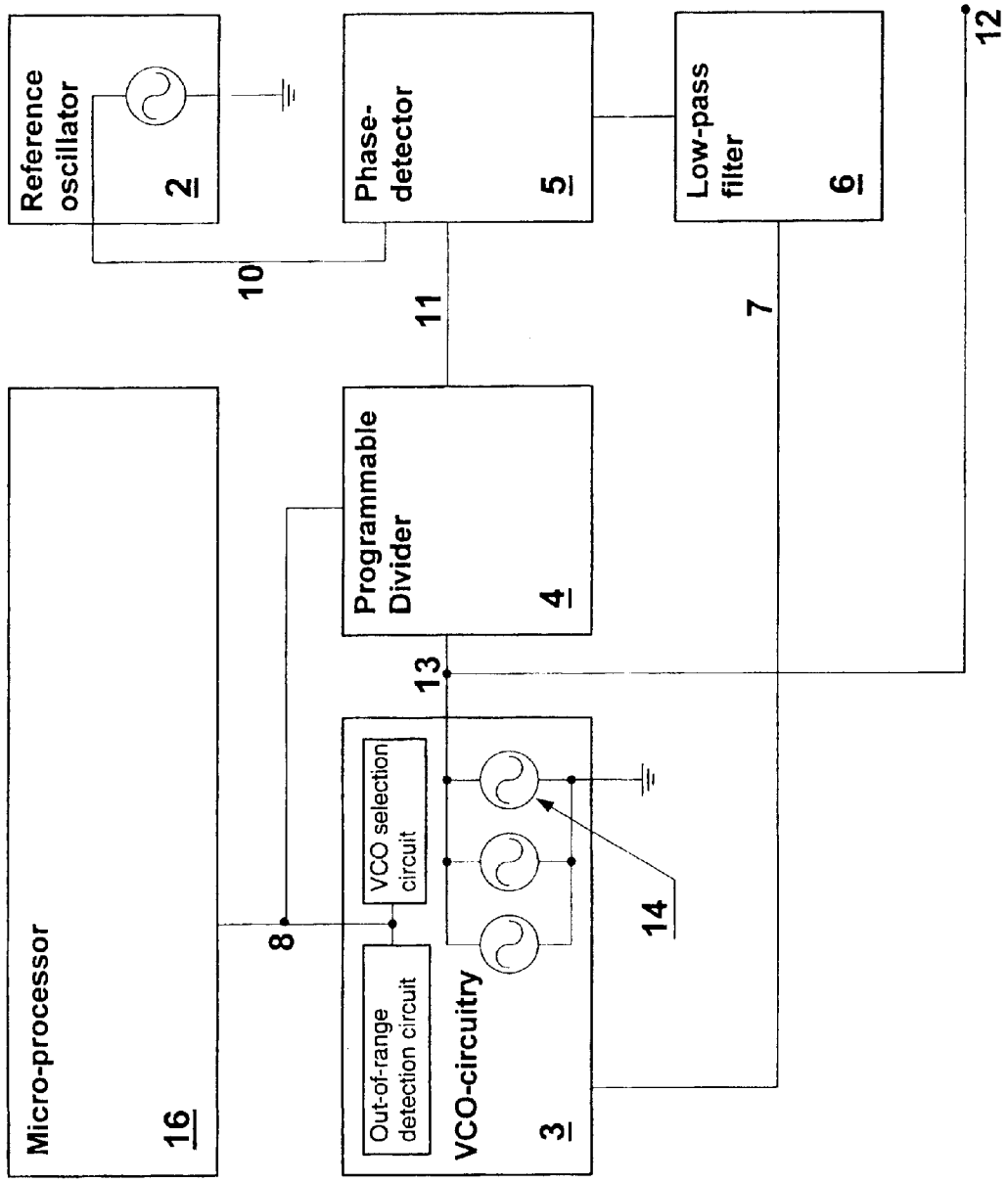
Reference oscillator
2
Phase-detector
5
Low-pass filter
6
12
10
11
7
Micro-processor
16
Programmable Divider
4
13
8
VCO selection circuit
Out-of-range detection circuit
VCO-circuitry
3
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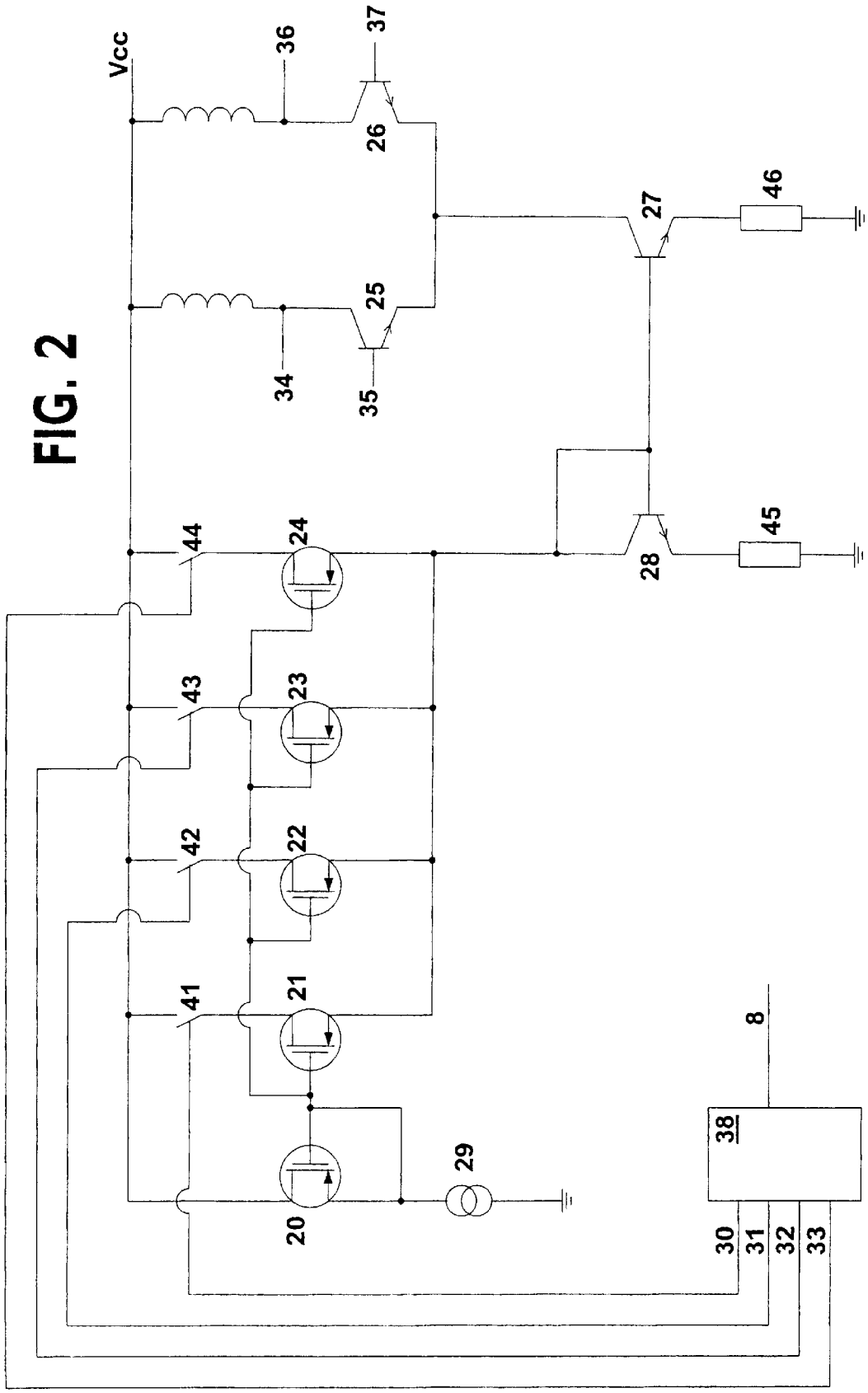
FIG. 2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VCO WITH PROGRAMMABLE OUTPUT POWER

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to voltage controlled oscillators, and more specifically it relates to regulation of the output signal level from voltage controlled oscillators, when used in different applications, further the invention relates to a method for reducing losses in phase locked loops using voltage controlled oscillators.

2. Description of the Prior Art

Voltage controlled oscillators are widely used in generating various frequencies within a specified frequency band.

Typically for such uses the voltage controlled oscillator is incorporated in a phase locked loop.

Such a phase locked loop may incorporate a reference oscillator, a phase detector, a low pass filter, a programmable divider and a voltage, controlled oscillator, all co-operating in the following manner.

The reference oscillator, typically a crystal oscillator, generates a fixed frequency which is supplied to the phase detector on a first line. The phase detector compares the phase of the signal on the first line with the phase of a frequency signal on a second line originating from the voltage controlled oscillator. This frequency signal from the voltage controlled oscillator may be divided down by a programmable divider before the phase comparison in the phase detector takes place. Based on the comparison, the phase detector generates an error signal on a third line, via which it is input to the voltage controlled oscillator. The error signal is in the form of a control voltage signal for the voltage controlled oscillator. Based on the control voltage signal the voltage controlled oscillator generates an output signal on an output line. This signal is at a different frequency from the fixed frequency, depending on the division ratio of the programmable divider.

When using a voltage controlled oscillator in a phase locked loop in modern mobile communications, the operating frequency will typically be in the vicinity of 4 GHz. This signal may then conveniently be divided down with integer factors of 2, 4 and 8, thereby achieving frequencies in the most commonly used frequency bands around 1800 MHz, 1900 MHz, 900 MHz and 450 MHz.

However, operating a phase locked loop at 4 GHz in a mobile phone involves some problems.

At these frequencies the transmission of signals between individual parts of circuit in which the voltage controlled oscillator is incorporated depend very much on the actual design of the circuit in which the voltage controlled oscillator is incorporated. In fact it may in some cases even be a problem transmitting the signal from the voltage controlled oscillator to the programmable divider.

Increasing the output power of the voltage controlled oscillator may in some cases be a way around this problem.

However, it is generally undesired to increase power consumption anywhere in a mobile phone because they are generally battery powered. In fact quite a lot of effort has been put into decreasing the overall power consumption of mobile phones, in order to allow long standby times and long talk times without having to recharge the battery.

Further, programmable dividers for the use at 4 GHz are generally sensitive to too powerful signals.

One reason for this is that their design is inherently unstable, in order to be able to achieve the necessary operating speed for such high frequencies. Thus they are more prone to counting errors resulting in overtones in the output signal when the input signal is too powerful.

Since the voltage controlled oscillator is to be used in different mobile telephone constructions where it has to be ensured both that there is sufficient signal and that the signal is not too powerful, the output power has to be adjusted to the actual application.

Traditionally this has been done by having a voltage controlled oscillator with comparably high output power, and then having an attenuator in the circuit in which the voltage controlled oscillator is incorporated, in order to be able to attenuate the signal if it proves necessary in the particular application. In a phase locked loop the attenuator is found between the output of the voltage controlled oscillator and the input of the programmable divider.

As mentioned earlier, this is in mobile phones in contradiction to the overall object of reducing power consumption.

The present invention provides a voltage controlled oscillator, which may be used in a variety of applications, yet does not suffer from the above drawbacks.

SUMMARY OF THE INVENTION

According to the invention a voltage controlled oscillator comprises a voltage controlled oscillator assembly including means for regulating the output power from the at least one voltage controlled oscillator.

The invention reduces losses when using a voltage controlled oscillator in a phase locked loop.

According to the invention a method for reducing losses in a phase locked loop includes a micro-controller, arranged on the same chip as the voltage controlled oscillator, is used for regulating the level of the output signal from the voltage controlled oscillator chip.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates a phase locked loop incorporating a voltage controlled oscillator assembly **3** according to the invention; and

FIG. **2** illustrates a circuit diagram of the output stage of a voltage controlled oscillator assembly according to the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS OF THE INVENTION

The invention will now be explained in greater detail, based on the following description of an exemplary, non-limiting, preferred embodiment and using the enclosed drawing.

As can be seen in FIG. **1**, the phase locked loop incorporates a reference oscillator **2**, a phase detector **5**, a low pass filter **6**, a programmable divider **4** and a voltage controlled oscillator assembly **3** comprising at least one voltage controlled oscillator **14**.

These elements co-operate in the following manner.

The reference oscillator **2**, typically a crystal oscillator, generates a fixed frequency which is supplied to the phase detector **5** on a first line **10**. The phase detector **5** compares the phase of the signal on the first line **10** with the phase of a frequency signal on a second line **11** originating from the voltage controlled oscillator. This frequency signal from the

voltage controlled oscillator may be divided down by the programmable divider **4** before the phase comparison in the phase detector **5** takes place. Based on the comparison, the phase detector **5** generates an error signal on a third line **7**, via which it is input to the voltage controlled oscillator **14**. The error signal is in the form of a control voltage signal for the voltage controlled oscillator **14**. Based on the control voltage signal, the voltage controlled oscillator **14** generates an output signal on an output line **13**. This signal is at a different frequency from the fixed frequency, depending on the division ratio of the programmable divider **4**.

From the output line **13** the actual signal of interest is tapped via a line **12**. In the line **12** there may optionally be incorporated a second divider (not shown) used to divide the signal of interest down to a frequency desired for a specific use.

According to the invention, the line **13** connects the output of the voltage controlled oscillator assembly **3** directly to the programmable divider **4**, without any intermediate stages such as attenuators.

In FIG. **2** is shown a simplified circuit diagram of an embodiment of the output stage of a VCO according to the invention. Two output transistors **35** and **37** are biased by a current mirror comprising two transistors **27** and **28**. The differential oscillator signal (not shown) is fed to the two input terminals **35** and **37**, the differential output signal is available at two output terminals **34** and **36**. A current multiplier sets the current in the current mirror. The current multiplier operates as follows: A current source **29** sets the current in MOSFET (Metal Oxide Semiconductor Field Effect Transistor) **20**. Another MOSFET **21** is identical to MOSFET **20**, thus the currents in the two MOSFETS **21**, **22** are the same. MOSFET **22** is chosen, so that for a given gate-source voltage, the current is two times the current through the MOSFET **20** with the same gate-source voltage. Likewise, a MOSFET **23** is chosen so that the current for a given gate-source voltage is 4 times that of the MOSFET **20**, and a MOSFET **24** is chosen so that the current for a given gate-source voltage is 8 times that of the MOSFET **20**. MOSFETs **21–24** can be switched in and out of the circuit by four switches **41–44**. The switches **41–44** are controlled by digital circuit **38** comprising a memory and a bus interface circuit capable of receiving calibration information from e.g. a micro-controller. The logical levels on four digital signal lines **30–33** are determined by the calibration information being sent to a digital circuit **38** through the bus **8**. For example, if the current source **29** sets the current through the MOSFET **20** to 10 mA and the switches **41** and **44** are closed, corresponding to a logic level "1" on the signal lines **30** and **33** (the switches **42** and **43** are open corresponding to logic level "0" on the signal lines **31** and **32**), the current through the transistor **27** and, thus the transistor **28**, is 20 mA+80 mA=100 mA. This current is divided equally between the transistors **25** and **26**, setting the bias current in each to 50 mA. As the output-power of transistors **25**, **26** is proportional to the bias current, the output power of the VCO is seen to be digitally controlled (programmed).

The regulated output on the line **13** need not be derived directly from the voltage controlled oscillator itself, but via an amplifier or buffer associated with the voltage controlled oscillator within the voltage controlled oscillator assembly **3**. i.e. on the same chip. In this case the regulation may be effected by regulating the amplification of the amplifier.

In order to regulate the output from the voltage controlled oscillator assembly **3**, the assembly incorporates a micro-controller **16** which as an external connection which may be connected to an external bus **8**. Via this external bus **8** the micro-controller **16** receives information about the output level required for the specific circuit configuration in which the voltage controlled oscillator assembly is placed. The voltage controlled oscillator assembly **3** is thus digitally programmable to deliver a specific output level.

This is particularly advantageous in applications such as mobile communication, which to a large extent depend on digital computing power anyway. Thus controlling the output power of the voltage controlled oscillator assembly via an already present bus **8**, does not require any substantial additional circuitry. The bus **8** used could for instance be the same bus **8** as used for transmitting the division ratio to the programmable divider.

Thus the invention facilitates the use of the same integrated circuit containing the voltage controlled oscillator assembly **3**, in a wide range of different circuits, because it is of less importance to adapt the layout and properties of these circuits to match the voltage controlled oscillator assembly.

Even though the above description has been given with reference to a voltage controlled oscillator it must be understood that the principle may also be applied in other circuits with different functions where a regulated power output is needed.

What is claimed is:

1. A voltage controlled oscillator assembly, comprising:

at least one voltage controlled oscillator including an output stage and a micro-controller for digitally regulating output power from the at least one voltage controlled oscillator; and wherein

the output power is controlled by applying a variable current bias to only the output stage and the output stage is within the at least one voltage controlled oscillator.

2. A voltage controlled oscillator assembly according to claim **1**, wherein the micro-controller is on a chip on which the at least one voltage controlled oscillator is located.

3. A voltage controlled oscillator assembly according to claim **1**, comprising an input which receives information which controls the output power.

4. A voltage controlled oscillator assembly according to claim **2**, comprising an input which receives information which controls the output power.

5. A phase locked loop comprising a voltage controlled oscillator assembly according to claim **1**.

6. A phase locked loop comprising a voltage controlled oscillator assembly according to claim **2**.

7. A phase locked loop comprising a voltage controlled oscillator assembly according to claim **3**.

8. A phase locked loop according to claim **5**, comprising:

a microprocessor which provides power control information to the microcontroller to control the output power from the at least one voltage controlled oscillator.

9. A phase locked loop according to claim **6**, comprising:

a microprocessor which provides power control information to the microcontroller to control the output power from the at least one voltage controlled oscillator.

10. A phase locked loop according to claim **7**, comprising:

a microprocessor which provides power control information to the microcontroller to control the output power from the at least one voltage controlled oscillator.

11. A method of regulating output power from at least one voltage controlled oscillator with a micro-controller comprising:

providing information to the micro-controller specifying an output level of power to be provided by the at least one voltage controlled oscillator including an output stage; and

generating a control signal from the information which is applied as a variable current bias only to the output stage of the voltage controlled oscillator to control the output power of the at least one voltage controlled oscillator to be in accordance with the information specifying the output power; and wherein the output stage is within the at least one voltage controlled oscillator.

12. A method in accordance with claim 11, wherein:

the at least one voltage controller oscillator and the micro-controller is part of one integrated circuit; and

the control signal controls current in the output stage.

13. A method in accordance with claim 12, wherein:

the output stage is a differential oscillator having differentially connected transistors; and

the control signal controls a bias current of the differentially connected transistors.

* * * * *

EXHIBIT F

US005898740A

United States Patent [19]

Laakso et al.

[11] **Patent Number: 5,898,740**

[45] **Date of Patent: Apr. 27, 1999**

[54] **POWER CONTROL METHOD IN A CELLULAR COMMUNICATION SYSTEM, AND A RECEIVER**

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[73] Assignee: **Nokia Telecommunications OY**, Espoo, Finland

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[22] PCT Filed: **Aug. 23, 1995**

[86] PCT No.: **PCT/FI95/00450**

§ 371 Date: **Feb. 21, 1997**

§ 102(e) Date: **Feb. 21, 1997**

[87] PCT Pub. No.: **WO96/07246**

PCT Pub. Date: **Mar. 7, 1996**

[30] **Foreign Application Priority Data**

Aug. 24, 1994 [FI] Finland 943889

[51] **Int. Cl.**[6] **H04B 1/10**

[52] **U.S. Cl.** **375/346**; 375/349; 455/522; 455/69; 455/574; 370/318

[58] **Field of Search** 375/200, 206, 375/219, 221, 285, 343, 346, 349; 455/67.1, 69, 422, 127, 13.4, 38.3, 522, 574, 92, 226.1, 226.2; 370/320, 342, 318, 319

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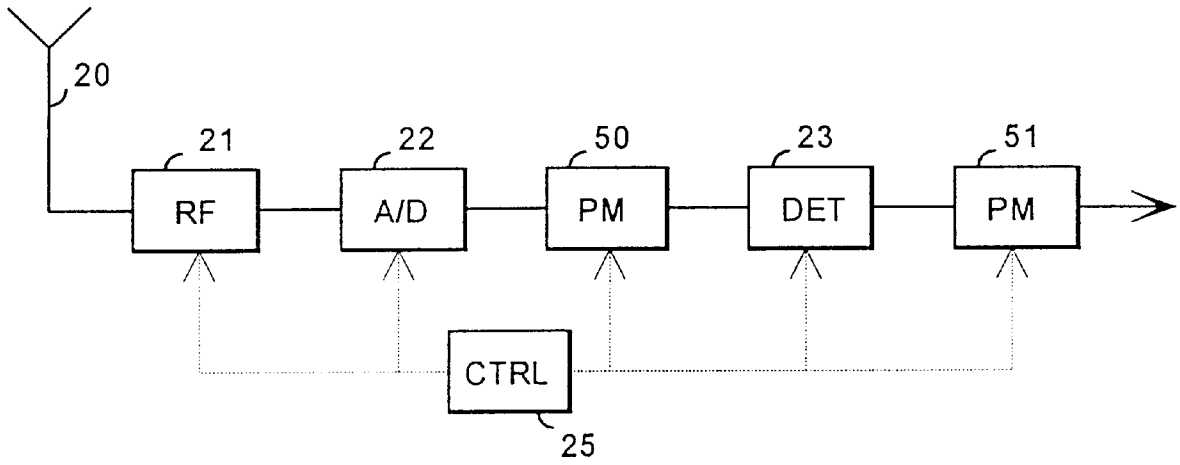
Primary Examiner—Stephen Chin
Assistant Examiner—Amanda Le
Attorney, Agent, or Firm—Pillsbury Madison & Sutro LLP

[57] **ABSTRACT**

In a method for controlling transmission power in a cellular communication system which utilizes a technique for canceling multiple access interference, and in which a receiver controls the transmission power of a transmitter on the basis of a received signal, power control is carried out on the received signal after the received signal has been subjected to interference cancellation.

11 Claims, 3 Drawing Sheets



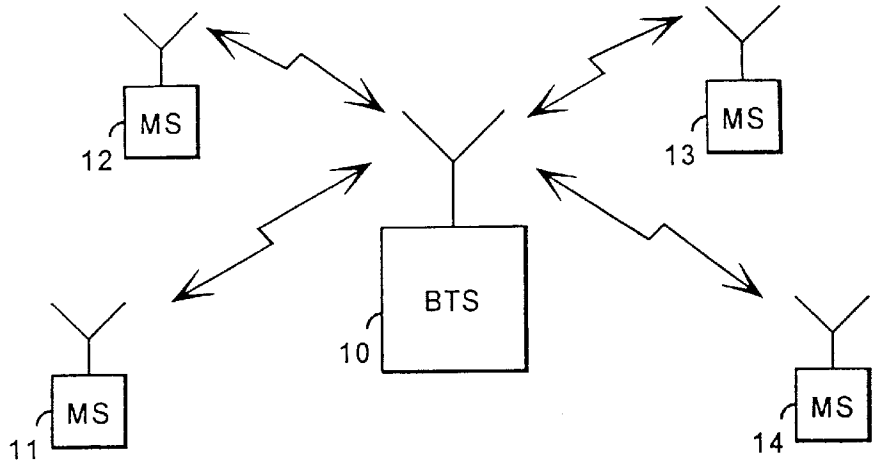

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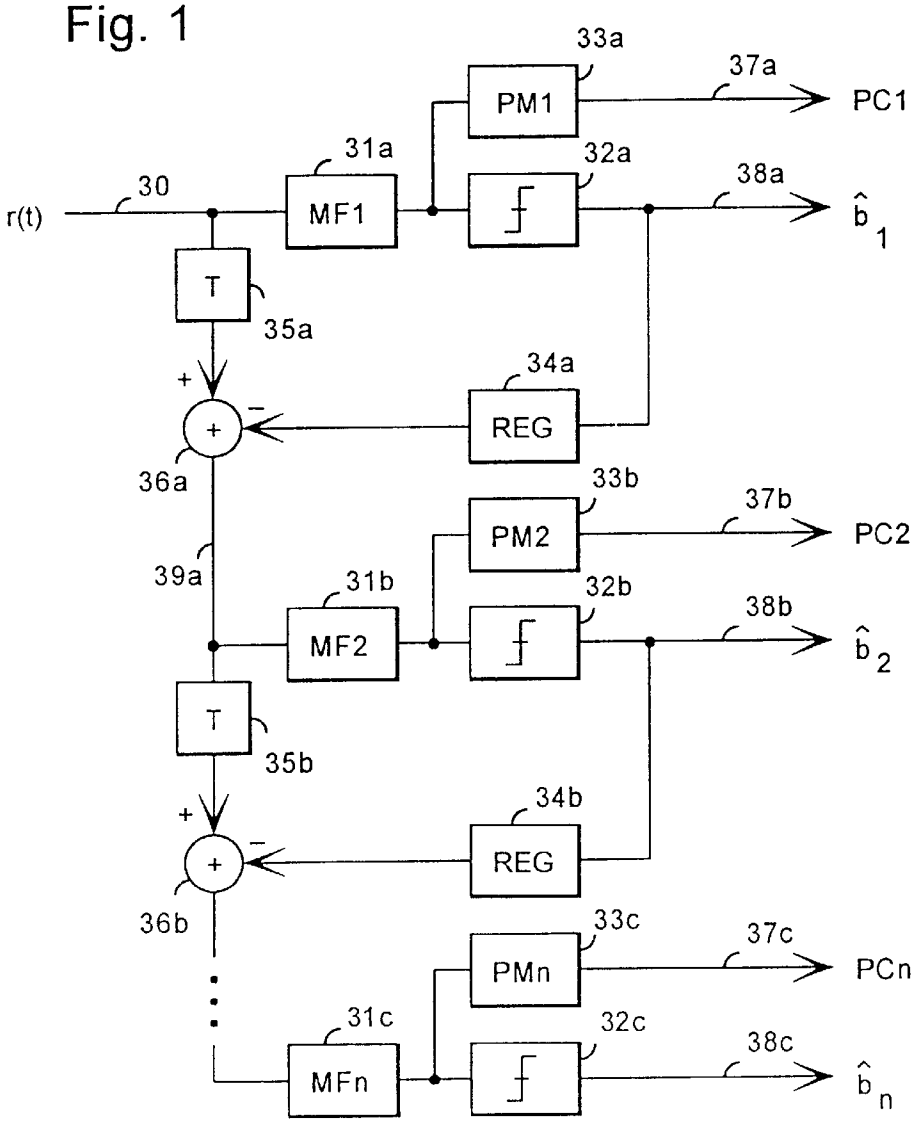
Fig. 1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34a
+
−
REG
36a
33b
37b
PM2
PC2
39a
31b
32b
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MF2
$\hat{b}_2$
T
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Fig. 3

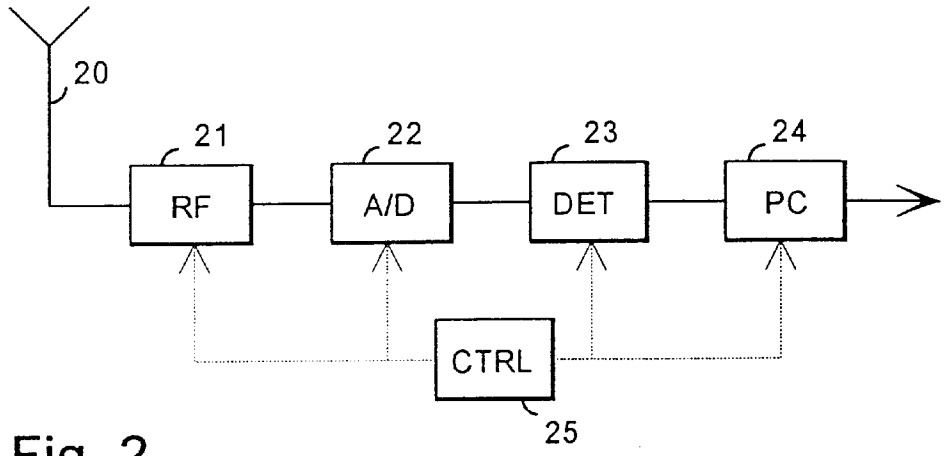
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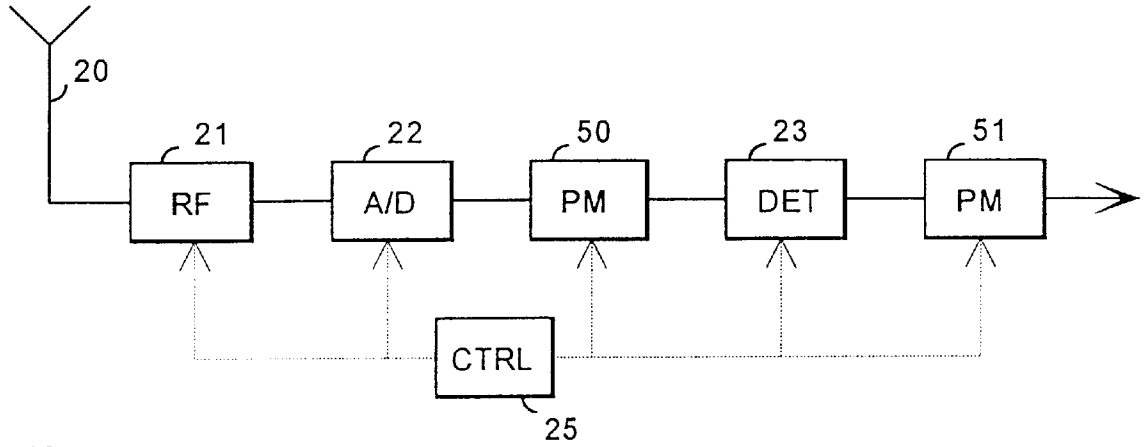
Fig. 2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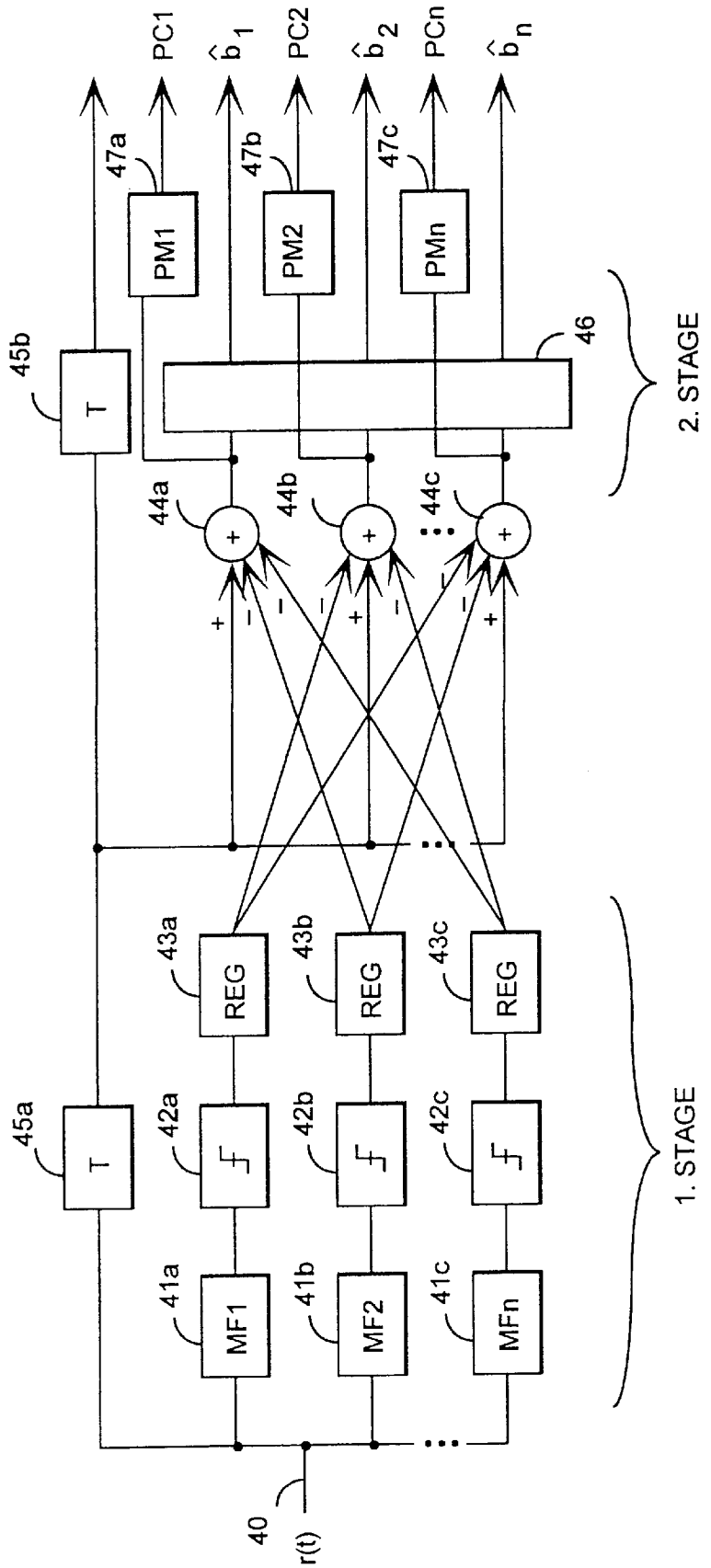
PM
CTRL
25

Fig. 5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PC2
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PCn
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45b
T
46
2. STAGE
44a
44b
44c
+
−
43a
43b
43c
REG
45a
42a
42b
42c
41a
41b
41c
MF1
MF2
MFn
1. STAGE
40
r(t)

Fig. 4

POWER CONTROL METHOD IN A CELLULAR COMMUNICATION SYSTEM, AND A RECEIVER

This s application is the national phase of international application PCT/ F195 /00450 filed Aug. 23, 1995.

BACKGROUND OF THE INVENTION

The invention relates to a method for controlling transmission power in a cellular communication system in which some method for cancelling multiple access interference is utilized and in which a receiver controls the transmission power of a transmitter on the basis of a received signal.

When data transmission systems are designed and implemented, it is endeavored to maximize the number of simultaneous users on an available frequency band without compromising the quality of the transmission. An essential problem is simultaneous transmission and reception of the signals of several simultaneous users, so that the signals cause as little interference to each other as possible. Owing to this fact and the available transmission capacity, several different transmission protocols and multiple access methods have been developed, the most common of which in particular in mobile communication are the FDMA and the TDMA methods, and lately also the CDMA method. The present invention is suited for use in particular in CDMA cellular communication systems.

CDMA is a multiple access method, which is based on the spread spectrum technique, and which has been applied recently in cellular communication systems, in addition to the prior FDMA and TDMA methods. CDMA has several advantages over the prior methods, such as the simplicity of frequency planning and spectral efficiency, which results in a large capacity, i.e. the number of simultaneous users on a given frequency band.

In CDMA, the narrow-band data signal of the user is multiplied to a relatively wide band by means of a spreading code having a remarkably broader band than the data signal. Bandwidths used in known test systems are e.g. 1.25 MHz, 10 MHz and. 25 MHz. In connection with the multiplication, the data signal spreads onto the whole of the band used. All users transmit simultaneously by using the same frequency band. An individual spreading code is used on each connection between the base station and the mobile station, and the signals of the users may be distinguished from each other in the receivers on the basis of the spreading code of each user. An attempt is made for choosing the spreading codes so that they are mutually orthogonal, i.e. they do not correlate with each other.

Correlators or adapted filters in CDMA receivers implemented in a conventional way are synchronized with the desired signal, which is identified on the basis of the spreading code. The data signal is returned in the receiver onto the original band by multiplying it by the same spreading code as in the transmission phase. The signals which have been multiplied by some other spreading code neither correlate nor return to the narrow band in an ideal case. They thus appear as noise from the point of view of the desired signal. The aim is thus to detect the signal of the desired user among several interfering signals. In practice, the spreading codes are not completely non-correlated, and the signals of other users complicate the detection of the desired signal by distorting the received signal. This interference caused by the users for each other is termed as multiple access interference.

The mutual interference caused by simultaneous users for each other described above is the decisive factor for the

capacity of the CDMA cellular communication system. The interference may be reduced e.g. by attempting to keep the transmission power levels of the mobile stations as low as possible by means of accurate power control. The power control may be based on some parameter measured or calculated from a received transmission, such as the received power, the signal-to-noise ratio or other quality parameter.

It is advantageous from the point of view of the capacity of the CDMA system if the base station receives the signal from all mobile stations with the same power. However, accurate and fast power control has been difficult to implement, and active reception methods based on interference cancellation thus have also been developed for reducing the interference. Such methods include, for example, interference cancellation methods (IC) and the multiuser detection (MUD). From the point of view of the present invention, the above mentioned reception methods are equal, and in the following they will be generally termed as interference cancellation methods.

In the solutions disclosed above, power control and interference cancellation are discussed as separate solutions. Conventional power control does not take into account the interference cancellation methods which are possibly used in the system, and which also improve the quality of the signal in the receiver, and conventional power control has thus resulted in an under-optimal result, in which case the available capacity has not been successfully utilized in the best possible way.

SUMMARY OF THE INVENTION

The object of the present invention is thus to implement a power control method which takes into account the effect of the interference cancellation on the received signal, and thus leads to a better result than heretofore provided from the point of view of the capacity of the system.

This is achieved with a method of the type set forth in the foregoing BACKGROUND section, which is characterized in that power control is carried out on the basis of the received signal processed with the interference cancellation method.

The invention further relates to a receiver in a cellular communication system, comprising means for reducing multiple access interference, and means for controlling the transmission power of the transmitter on the basis of the received signal. The receiver of the invention is characterized in that means for measuring the parameters required for power control from the received signal are connected after the interference cancellation means.

In the method of the invention, the measurement of the parameters that have an effect on power control is carried out from the signal from which interferences have been reduced with an appropriate interference cancellation method. Thus, a better result can be achieved in interference cancellation, which results in a larger capacity of the system.

The power control of the invention does not set any limits to the interference cancellation method used or the selection of the interference signals to be eliminated.

In a second embodiment of the invention, the measurement of the parameters is carried out both before and after the interference cancellation. Then the preceding measurement provides a rapid response, which does not depend on the delay of the interference cancellation. The latter measurement provides a final, accurate measurement result, which results in the desired quality of the user's signal.

BRIEF DESCRIPTION OF THE INVENTION

In the following, the invention will be described in greater detail with reference to the examples in the attached drawings, in which

FIG. **1** shows a cellular communication system in which the method of the invention may be applied,

FIG. **2** is a block diagram illustration of the structure of the receiver in accordance with a preferred embodiment of the invention,

FIG. **3** shows a more detailed illustration of a possible structure of the receiver of the invention,

FIG. **4** illustrates an example of a second possible structure of the receiver of the invention, and

FIG. **5** is a block diagram showing the principle of the structure of the second embodiment of the invention.

DETAILED DESCRIPTION

FIG. **1** illustrates a part of the cellular communication system in which the method of the invention may be applied. Each cell of a cellular radio network comprises at least one base station **10** communicating with the subscriber terminal equipments **11–14** within its area. All terminal equipments transmit on the same frequency to the base station **10**, which distinguishes the transmissions of different terminal equipments from each other on the basis of the spreading code used by each respective terminal equipment. As it has been described above, the signals of the terminal equipments interfere with each other. In the receiver, the power level perceived at the reception of each signal is measured. The results of this power measurement may be utilized for power control. On the basis of the power measurement, it is also possible to calculate other parameters to be utilized for power control and for other purposes, as well.

It is also possible that the base station of FIG. **1** has other frequency bands available to be used for communication with other terminal equipments located within its area. However, these terminal equipments on different frequencies do not interfere with each other, and within both frequencies, the operation of the cell may be assumed to be independent from the point of view of the invention.

Let us assume that in the cellular communication system of FIG. **1** some interference cancellation system is used for reducing multiple access interference. The method of the invention is suited to be used in connection with any known interference cancellation method or power control algorithm. The basic idea of the invention is to take into account the improvement caused by the interference cancellation method used in the system in the received signal prior to calculating and measuring the parameters that have an effect on power control. A power control command is calculated on the basis of the measured parameters, and the command is transmitted to the transmitter by means of known methods. As the measurement of the parameters is carried out after the interference cancellation, the power levels of different signals settle so that a desired quality of the signal is obtained for each user. The aim is generally to balance the final signal-to-interference ratio before the bit decision is made. The balancing leads to the same average bit-error rate for all users.

Filtering, such as averaging of successive parameters may also be connected with the measurement of the parameters, and the purpose of such filtering is to equalize the statistical variation of the estimates, and the prediction with the aid of which it is endeavored to follow and forecast the changes in the received signal.

The method of the invention may be applied, e.g., in connection with the successive interference cancellation. In the successive interference cancellation, the receiver processes the received transmission so that the signals are demodulated in a certain order, typically in order of magnitude, regenerated and reduced from the received transmission, whereafter the following signal is processed in the same way until all the signals have been processed. In the method of the invention, instead of estimating the power of each user from the total signal in which all interferences are included, the power control and the measurement of parameters connected therewith are carried out on the basis of the purged signal, from which the signals stronger than those of the current user have been reduced.

The invention is also suited to be used in connection with so-called multi-stage interference cancellation in which all the users to be received are processed in parallel, and the bit estimates are adjusted iteratively by repeating the reception procedure after the interference estimates have been reduced. Similarly, the estimates of the necessary power control parameters may be adjusted iteratively for obtaining as reliable power control as possible.

FIG. **2** illustrates a block diagram of the structure of the preferred embodiment of the invention. The receiver of the invention comprises an antenna **20**, by means of which the received signal is applied to radio frequency elements **21**. From the radio frequency elements, the signal is applied via an A/D converter **22** to means **23**, where the interference cancellation and detection of the received signal are carried out. The receiver further comprises means **24**, which carry out the measurement of power control parameters from the received signal, and which are connected after the interference cancellation and detection means **23**. The signal received from means **24** is further applied to other elements of the receiver. The receiver further comprises control means **25**, which control the operation of the elements mentioned above and calculate the actual power control commands on the basis of the parameters obtained from the measurement means.

FIG. **3** illustrates the structure of the receiver of the invention in closer detail as to the essential parts of the invention, in a case in which the successive interference cancellation is employed in the system. The blocks shown in FIG. **3** correspond to blocks **23** and **24** in FIG. **2**. As it has been described above, in the successive interference cancellation, the received transmission is processed in the receiver, so that the signals are demodulated in a certain order, typically in order of magnitude, regenerated and reduced from the received transmission, whereafter the following signal is processed in the same way, until all signals have been processed.

The receiver in accordance with FIG. **3** comprises a plurality of adapted filters or RAKE receivers **31***a*–**31***c*, which are each adapted to receive and demodulate the signal of one user, which signals may be distinguished from each other on the basis of the spreading code. The signals are typically demodulated in order of magnitude, whereby the interfering effect of the strongest signals may be eliminated prior to processing the weaker signals.

The received transmission **30** is applied to a first adapted filter **31***a*, where the desired signal is demodulated, and further to a first detector **32***a*, where the bit decision is made. Signal **38***a* obtained from detector **32***a*, thus comprising the estimate of the transmission of the first user, is further applied to other elements of the receiver. In accordance with the successive interference cancellation method, the signal obtained from the first detector **32***a* is also applied to a first regeneration means **34***a*, where the detected signal is regenerated again, i.e. re-multiplied by the spreading code. The obtained regenerated signal is further applied to a first

summing means **36***a,* where it is reduced from the received transmission **30**, which has been applied to summing means **36***a* via a first delay means **35***a*. The signal located at the output of the first adapted filter **31***a* is applied, in addition to the first detector **32***a,* to a first measurement means **33***a,* which carries out from the signal the measurement of the parameters required for power control. A typical measurement parameter is, e.g., the received power contained by the signal. The obtained measurement results **37***a* are applied to further processing.

A signal **39***a* obtained from the first summing means **36***a* thus comprises the received transmission, from which the effect of the signal demodulated by the first adapted filter **31***a,* i.e. typically the effect of the strongest signal has been eliminated. The signal **39***a* is applied to a second adapted filter **31***b* and a second detector **32***b,* the output of which provides the bit decision **38***b* of the signal of the second user. The signal **38***b* of the second user is correspondingly applied to a second regeneration means **34***b,* wregener is regenerated and applied to a second summing means **36***b,* where it is reduced from the transmission **39***a,* which has been applied to the summing means via a second delay means **35***b*. The signal at the output of the second adapted filter **31***b* is applied, in addition to the second detector **32***b,* to a second measurement means **33***b,* which carries out from the signal the measurement of the parameters required for power control. In the receiver of the invention, the measurement results correspond better to a real situation, since the interfering effect of the stronger signals has been eliminated from the signal from which the measurement is carried out. The obtained measurement results **37***b* are applied to further processing.

The corresponding operations are performed to all received signals until the last user, whose signal is demodulated by means of an adapted filter **31***c* and a detector means **32***c*. From the output signal of the adapted filter **31***c,* the measurement of the power control parameter of the last user is carried out in measurement means **33***c*. The signal **38***c* of the last user does not need to be regenerated as it does not have to be reduced from the received signal, since all users have already been detected.

FIG. **4** illustrates the structure of the receiver of the invention in closer detail as to the essential parts for the invention, when a parallel multi-stage interference cancellation is employed in the system. The blocks in FIG. **4** correspond to blocks **23** and **24** in FIG. **2**. As has been described above, in the multi-stage interference cancellation, all users received are processed in parallel, and bit estimates are adjusted iteratively by repeating the reception procedure after eliminating the interference estimates. The procedure may be repeated twice or several times, i.e. the receiver may comprise several successive stages. The estimates of the necessary power control parameters may also be adjusted iteratively, as well as the detected signal for accomplishing as reliable power control as possible.

FIG. **4** illustrates the first two stages of a multi-stage receiver, but there may be more stages. A received signal **40** is simultaneously applied to adapted filters **41***a*–**41***c,* which each demodulate the signal of one user. The number of the adapted filters is thus the same as the number of current users. The output signals of the adapted filters are applied to detector means **42***a*–**42***c,* where a bit decision is made for each signal. When desired, the bit decision may be made in other elements of the receiver, but it is not marked in the figure for the sake of simplicity. The detected signals are further applied to regeneration means **43***a*–**43***c,* where the original transmission of each user is regenerated from the detected signal estimates. The adapted filters **41***a*–**41***c,* the detector means **42***a*–**42***c* and the regeneration means **43***a*–**43***c* form the first stage of the receiver.

The regenerated signals are further applied as negative inputs to summing means **44***a*–**44***c,* the number of which is the same as the number of the users of the system. The original received transmission **40** is applied as a positive input to each summing means **44***a*–**44***c* via a first delay means **45***a*. In a first summing means **44***a,* the regenerated signals, i.e. the output signals of regeneration means **43***b*–**43***c* of the other users except that of the first user are reduced from the original signal. The output signal of the first summing means **44***a* thus comprises a transmission which comprises the signal of the first user, and from which the interference estimate of the other users has been reduced. Accordingly, the output signals of summing means **44***b* and **44***c* only comprise the transmission of the desired user, from which transmission the interference estimates of other users have been reduced. The obtained signals are further applied to a second stage **46** of the receiver, where signals are further processed and re-detected. There may be several successive stages.

The output signals of summing means **44***a*–**44***c* are also each applied to a separate measurement means **47***a*–**47***c,* where the parameters required for power control are measured from each signal, and those parameters are further applied to the unit which is responsible for power control. Since the interfering effect of other signals has been eliminated from the signal from which the measurement is carried out, the obtained result is more accurate than what has been possible to achieve with prior art methods. A corresponding measurement may also be carried out from the output signals of latter stages, which provides an even more accurate result.

The power control of the invention thus takes into account the effect of the interference cancellation on the signal-to-interference ratio, on the basis of which the quality of each signal is determined, and thus leads to a desired optimal power control result when interference cancellation algorithms are employed.

When the successive interference cancellation method is employed, the power control of the invention leads to a power distribution in which the signals to be removed first are the strongest, whereas in the multi-stage interference cancellation the power distribution is even. Special features may be added to the power control of the invention if desired, such as generation of different grades of service. For example, part of the users may be set a better signal-to-interference target level the power control aims at, which naturally results in capacity loss compared with a uniform system.

In the second embodiment of the invention the measurement of the power control parameters is carried out both before and after carrying out the interference cancellation. In that case, the first measurement rapidly provides a measurement result that does not depend on the delay inevitably connected with the interference cancellation. On the basis of the measurement after the interference cancellation, a final, more accurate, result is obtained on the basis of which a more accurate adjustment may be carried out that leads to a desired quality of the user's signal.

The structure of the receiver in accordance with the second embodiment of the invention is illustrated in the block diagram in FIG. **5**. As in the receiver in FIG. **2**, the receiver of the invention comprises an antenna **20**, by means of which the received signal is applied to radio frequency elements **21**. From the radio frequency elements the signal

is applied via an A/D converter **22** to a first measurement means **50**, where a preliminary measurement of the power control parameters is carried out. This corresponds to the measurement method employed in prior art methods. From the first measurement means **50** the signal is applied to means **23**, where the interference cancellation and detection of the received signal is carried out. The receiver further comprises means **51** which carry out the measurement of the power control parameters from the received signal which has been processed with interference cancellation methods, means **51** being connected after interference cancellation and detection means **23**. The signal obtained from means **51** is further applied to other elements of the receiver. The receiver further comprises control means **25** that control the operation of the above mentioned elements and calculate the actual power control commands on the basis of the parameters obtained from measurement means **50** and **51**.

Although the invention has been described above with reference to the examples in accordance with the attached drawings, it is obvious that the invention is not limited thereto, but it may be modified in a variety of ways within the scope of the inventive idea set forth in the attached claims.

We claim:

1. A method for controlling transmission power in a cellular communication system, comprising the steps of:

receiving a signal by a receiver as a result of transmission by a transmitter;

subjecting the thereby received signal to interference cancellation to obtain a received signal which has been subjected to interference cancellation;

measuring parameters required for power control of the transmitter from said received signal which has been subjected to interference cancellation; and

said receiver controlling transmission power of said transmitter by use of said parameters.

2. The method of claim **1**, wherein:

said parameters include power of said received signal.

3. The method of claim **1**, wherein:

said parameters include signal-to-interference ratio of said received signal.

4. The method of claim **1**, further including:

also measuring parameters required for power control of the transmitter from said received signal before subjecting said received signal to said interference cancellation;

and said receiver controlling said transmission power of said transmitter by use not only of the respective said parameters measured from said received signal which has been subjected to interference cancellation but also of the respective said parameters measured from said received signal before said received signal has been subjected to interference cancellation.

5. A method for controlling transmission power in a cellular communication system, comprising the steps of:

receiving each of a plurality of signals by a receiver as a result of respective transmissions by a plurality of transmitters;

subjecting each thereby received signal to interference cancellation to obtain a respective received signal which has been subjected to interference cancellation;

measuring parameters required for power control of respective ones of said transmitters from respective ones of said received signals which have been subjected to interference cancellation; and

said receiver controlling transmission power of respective ones of said transmitters by use of respective ones of said parameters;

said receiving comprising detecting each said received signal from a given frequency band, in decreasing magnitude of received signal power, such that prior to detection of each said received signal subsequent to one having a greatest received signal power, effects of interference of those of said received signals having stronger received signal power are eliminated from the respective said received signals.

6. A method for controlling transmission power in a cellular communication system, comprising the steps of:

receiving each of a plurality of signals by a receiver as a result of respective transmissions by a plurality of transmitters;

subjecting each thereby received signal to interference cancellation to obtain a respective received signal which has been subjected to interference cancellation;

measuring parameters required for power control of respective ones of said transmitters from respective ones of said received signals which have been subjected to interference cancellation; and

said receiver controlling transmission power of respective ones of said transmitters by use of respective ones of said parameters;

said receiving comprising detecting all of said received signals in parallel, from a given frequency band.

7. The method of claim **6**, comprising:

practicing said detecting in a plurality of stages; and

measuring said parameters in a plurality of stages.

8. A receiver in a cellular communication system, comprising:

means for reducing multiple access interference;

means for controlling transmission power of a transmitter on the basis of reception by said receiver of a signal as a result of transmission by said transmitter; and

first means for measuring parameters required for controlling transmission power of said transmitter by said receiver, said measuring means being connected in said receiver functionally after said interference cancellation means.

9. The receiver of claim **8**, further comprising:

second means for measuring parameters required for power control of the transmitter from said received signal before subjecting said received signal to said interference cancellation;

said means for controlling transmission power being arranged for controlling said transmission power by use not only of the respective said parameters measured by said first means for measuring, but also the respective of said parameters measured by said second means for measuring.

10. A receiver in a cellular communication system, comprising:

means for reducing multiple access interference;

means for controlling transmission power of each of a plurality of transmitters on the basis of reception by said receiver of respective signals as a result of respective transmissions by said transmitters, to thereby provide respective receiver signals;

means for measuring parameters required for controlling transmission power of respective ones of said transmitters by said receiver, said measuring means being connected in said receiver functionally after said interference cancellation means, and

detector means for detecting each said received signal from a given frequency band, in decreasing order of received signal power, such that prior to detection of each said received signal subsequent to one having a greatest received signal power, effects of interference of those at said received signals having stronger received signal power are eliminated from the respective said received signals.

11. A receiver in a cellular communication system, comprising:

means for reducing multiple access interference;

means for controlling transmission power of each of a plurality of transmitters on the basis of reception by said receiver of respective signals as a result of respective transmissions by said transmitters, to thereby provide respective receiver signals;

means for measuring parameters required for controlling transmission power of respective ones of said transmitters by said receiver, said measuring means being connected in said receiver functionally after said interference cancellation means, and

detector means for detecting all of said received signals in parallel, from a given frequency band.

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