EXHIBIT 20

Intel® PXA27x Processor Family

Electrical, Mechanical, and Thermal Specification

Data Sheet

- High-performance processor:
  - —Intel XScale® microarchitecture with Intel® Wireless MMX™ Technology
  - —7 Stage pipeline
  - —32 KB instruction cache
  - —32 KB data cache
  - —2 KB “mini” data cache
  - —Extensive data buffering
- 256 Kbytes of internal SRAM for high speed code or data storage preserved during low-power states
- High-speed baseband processor interface (Mobile Scalable Link)
- Rich serial peripheral set:
  - —AC’97 audio port
  - —I^2S audio port
  - —USB Client controller
  - —USB Host controller
  - —USB On-The-Go controller
  - —Three high-speed UARTs (two with hardware flow control)
  - —FIR and SIR infrared communications port
- Hardware debug features — IEEE JTAG interface with boundary scan
- Hardware performance-monitoring features with on-chip trace buffer
- Real-time clock
- Operating-system timers
- LCD Controller
- Universal Subscriber Identity Module interface
- Low power:
  - —Wireless Intel Speedstep® Technology
  - —Less than 500 mW typical internal dissipation
  - —Supply voltage may be reduced to 0.85 V
  - —Four low-power modes
  - —Dynamic voltage and frequency management
- High-performance memory controller:
  - —Four banks of SDRAM: up to 104 MHz @ 1.8 V I/O interface
  - —Six static chip selects
  - —Support for PCMCIA and Compact Flash
  - —Companion chip interface
- Flexible clocking:
  - —CPU clock from 104 to 520 MHz
  - —Flexible memory clock ratios
  - —Frequency changes
  - —Functional clock gating
- Additional peripherals for system connectivity:
  - —SD Card/MMC Controller (with SPI mode support)
  - —Memory Stick card controller
  - —Three SSP controllers
  - —Two I^2C controllers
  - —Four pulse-width modulators (PWMs)
  - —Keypad interface with both direct and matrix keys support
  - —Most peripheral pins double as GPIOs

Order Number 280003-004

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Revision History

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Date	Revision	Description
April 2004	-001	First public release of the EMTS
June 2004	-002	Re-release at same time as Intel® PXA270 Processor EMTS
June 2004	-003	Modified Watchdog Reset timing description Chapter 6, “Reset and Power Manager Timing Specifications” Corrected 13MHz Oscillator slew rate specification Chapter 5, “Oscillator Electrical Specifications” Updated title reference to the Stacked Memory data sheet “*Intel® PXA27x Processor Family Memory Subsystem Datasheet”* Chapter 5, “Oscillator Electrical Specifications” Removed PXA273 details from this datasheet
April 2005	-004	Modified PXA27x Processor Family Package top view, Chapter 3, “Package Information” Added note to VCC_BB voltage specifications, Chapter 5, “Electrical Specifications” Modified Core Voltage and Frequency Electrial Specifications, Chapter 5, “Electrical Specifications” Modified SDRAM Interface AC Specificatons ,Chapter 6, “AC Timing Specifications” Modified description about the basic material properties of the processor components,Chapter 3, “Package Information”

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Documentation Feedback Form for the Intel® PXA27x Processor Family Electrical, Mechanical, Thermal Specification

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1. Overall organization of the manual:	5 ☐	4 ☐	3 ☐	2 ☐	1 ☐
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3. Overall organization of content within chapters:	5 ☐	4 ☐	3 ☐	2 ☐	1 ☐
4. Accuracy of the content:	5 ☐	4 ☐	3 ☐	2 ☐	1 ☐
5. Sufficient level of detail to the content:	5 ☐	4 ☐	3 ☐	2 ☐	1 ☐
6. Readability/comprehension of the content:	5 ☐	4 ☐	3 ☐	2 ☐	1 ☐
7. Accuracy/Usefulness of tables and figures:	5 ☐	4 ☐	3 ☐	2 ☐	1 ☐
8. Accuracy/functionality of cross-references:	5 ☐	4 ☐	3 ☐	2 ☐	1 ☐
9. Accuracy/usefulness of lists (index, TOC, etc.):	5 ☐	4 ☐	3 ☐	2 ☐	1 ☐

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12. This manual needs to have less of:

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14. The thing(s) I liked least about this manual:

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Introduction 1

The Intel® PXA27x Processor Family (referred to throughout this document as the Intel PXA27x processor family) provides industry-leading multimedia performance, low-power capabilities, rich peripheral integration and second generation memory stacking. Designed from the ground up for wireless clients, it incorporates the latest Intel advances in mobile technology over its predecessor, the Intel® PXA255 processor. The Intel PXA27x processor family redefines scalability by operating from 13 MHz up to 520 MHz, providing enough performance for the most demanding mobile applications.

The Intel PXA27x processor family is the first Intel processor to include Intel® Wireless MMX™ technology, enabling high-performance, low-power multimedia acceleration with a general-purpose instruction set. Intel® Quick Capture technology provides a flexible and powerful camera interface for capturing digital images and video. While performance is key in the Intel PXA27x processor family, power consumption is also a critical component. The new capabilities of Wireless Intel SpeedStep® technology set the standard for low-power consumption.

The Intel PXA27x processor family is available in both discrete and stacked versions in the following configurations:

- Intel® PXA271 processor (Intel PXA271 processor)with 32 MBytes of Intel StrataFlash® Memory and 32 MBytes of Low-Power SDRAM
- Intel® PXA272 processor (Intel PXA272 processor) with 64 MBytes of Intel StrataFlash® Memory

1.1 About This Document

This document constitutes the electrical, mechanical, and thermal specifications for the Intel PXA27x processor. It contains a functional overview, mechanical data, package signal locations, targeted electrical specifications, and functional bus waveforms. For detailed functional descriptions other than parametric performance, refer to the *Intel® PXA27x Processor Family Developers Manual*.

1.1.1 Number Representation

All numbers in this document are **base 10** unless designated otherwise. Hexadecimal numbers have a prefix of 0x, and binary numbers have a prefix of 0b. For example, 107 is represented as 0x6B in hexadecimal and 0b110_1011 in binary.

1.1.2 Typographical Conventions

All signal and register-bit names appear in uppercase. Active low items are prefixed with a lowercase “n”.

Bits within a signal name are enclosed in angle brackets:

EXTERNAL_ADDRESS<31:0>
nCS<1>

Bits within a register bit field are enclosed in square brackets:

REGISTER_BITFIELD[3:0]

REGISTER_BIT[0]

Single-bit items have either of two states:

- **clear** — the item contains the value 0b0. To clear a bit, write 0b0 to it.
- **set** — the item contains the value 0b1. To set a bit, write 0b1 to it.

1.1.3 Applicable Documents

Table 1-1 lists supplemental information sources for the Intel PXA27x processor family. Contact an Intel representative for the latest document revisions and ordering instructions.

Table 1-1. Supplemental Documentation

Document Title
Intel® PXA27x Processor Family Developers Manual
ARM® Architecture Version 5T Specification (Document number ARM* DDI 0100D-10), and *ARM® Architecture Reference Manual* (Document number ARM* DDI 0100B)
Intel® XScale™ Core Developer's Manual
Intel® Wireless MMX™ Technology Developer's Guide
Intel® PXA27x Processor Design Guide
Intel® PXA27x Processor Power Supply Requirements Application Note
Intel® PXA27x Processor Family Memory Subsystem Datasheet

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Functional Overview 2

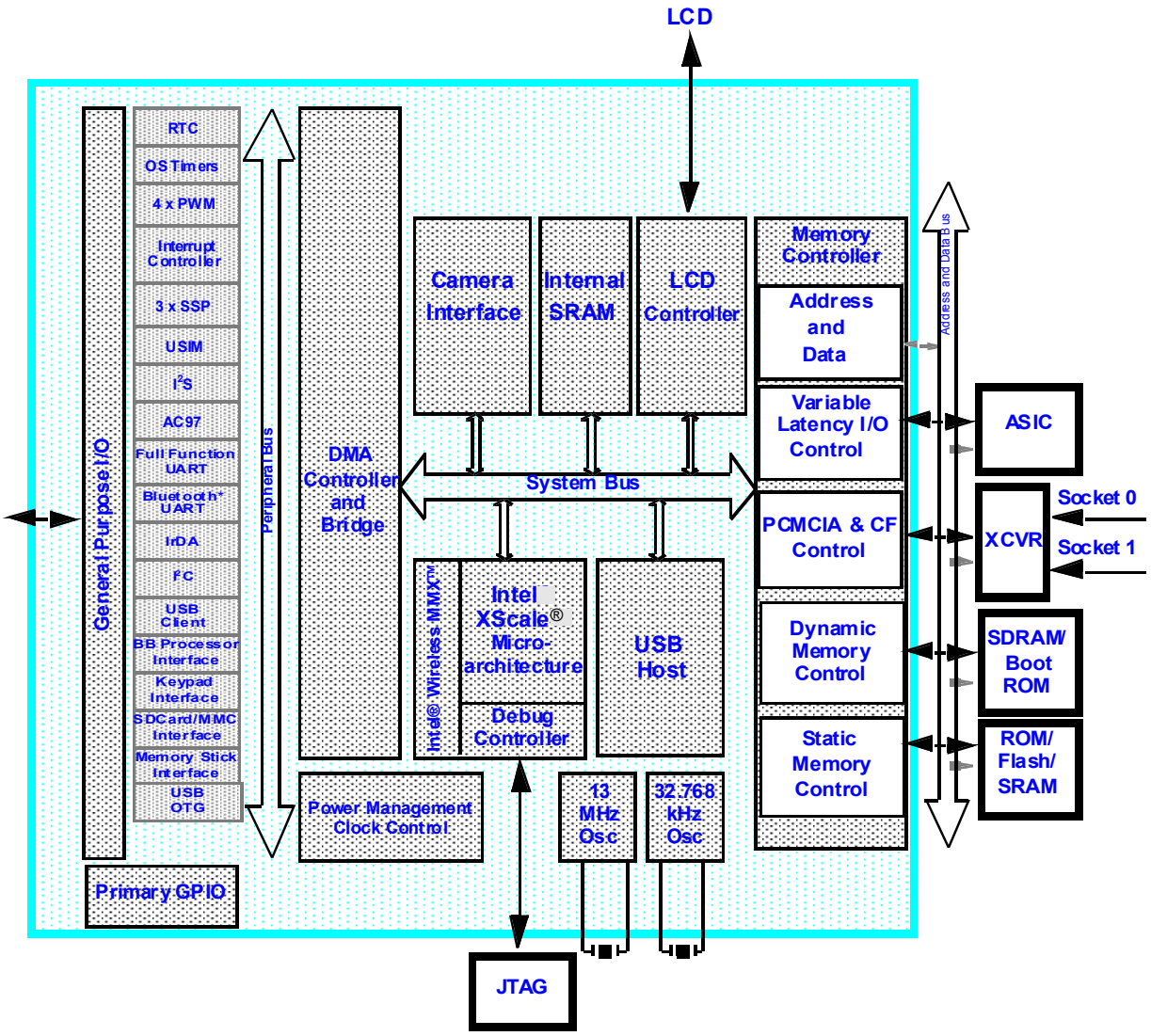
The Intel PXA27x processor family is an integrated system-on-a-chip microprocessor for high performance, dynamic, low-power portable handheld and hand-set devices. It incorporates the Intel XScale® technology which complies with the ARM* version 5TE instruction set (excluding floating-point instructions) and follows the ARM* programmer's model. The Intel PXA27x processor family also provides Intel® Wireless MMX™ media enhancement technology, which supports integer instructions to accelerate audio and video processing. In addition, it incorporates Wireless Intel Speedstep® Technology, which provides sophisticated power management capabilities enabling excellent MIPs/mW performance.

The Intel PXA27x processor family provides a scalable, bi-directional data interface to a cellular baseband processor, supporting seven logical channels and other features. The operating-system (OS) timer channels and synchronous serial ports (SSPs) also accept an external network clock input so that they can be synchronized to the cellular network. The processor also provides a Universal Subscriber Identity Module* (USIM) card interface.

The Intel PXA27x processor memory interface gives designers flexibility as it supports a variety of external memory types. The processor also provides four 64 kilobyte banks of on-chip SRAM, which can be used for program code or multimedia data. Each bank can be configured independently to retain its contents when the processor enters a low-power mode. An integrated LCD panel controller supports displays up to 800 by 600 pixels, permitting 1-, 2-, 4-, and 8-bit gray scale and 1-, 2-, 4-, 8-, 16-, 18-, and 24-bit color pixels. A 256-byte palette RAM provides flexible color mapping.

A set of serial devices and general-system resources offers computational and connectivity capability for a variety of applications. Figure 2-1 shows the block diagram for a typical Intel PXA27x processor system.

Figure 2-1. Intel® PXA27x Processor Family Block Diagram, Typical System



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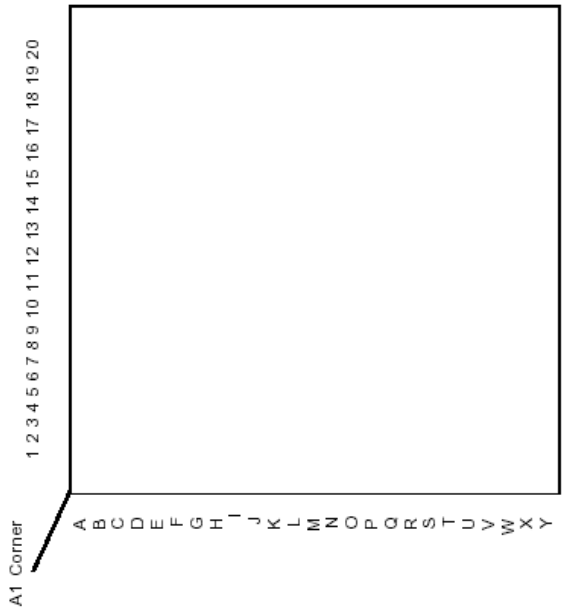
Package Information 3

This chapter provides the mechanical specifications for the Intel PXA27x processor family.

3.1 Package Information

Figure 3-1. 14 x 14 mm Intel® PXA27x Processor Family Package, Top View



The Intel PXA27x processor family has the following characteristics:

- Ball pitch: 0.65mm
- Ball diameter: 0.30 mm
- Substrate thickness: 0.21 mm
- Mold thickness: 0.45 mm

The Intel PXA27x processor family is packaged in a 14- by 14-mm, 336-pin, 0.65-mm package, as shown in Figure 3-2 and Figure 3-3.

Refer to Table 3-1 for package configuration information for Figure 3-1 and Figure 3-2.

3.2 Processor Materials

Figure 3-2. 14 x 14 mm Intel® PXA27x Processor Family Package, Top View

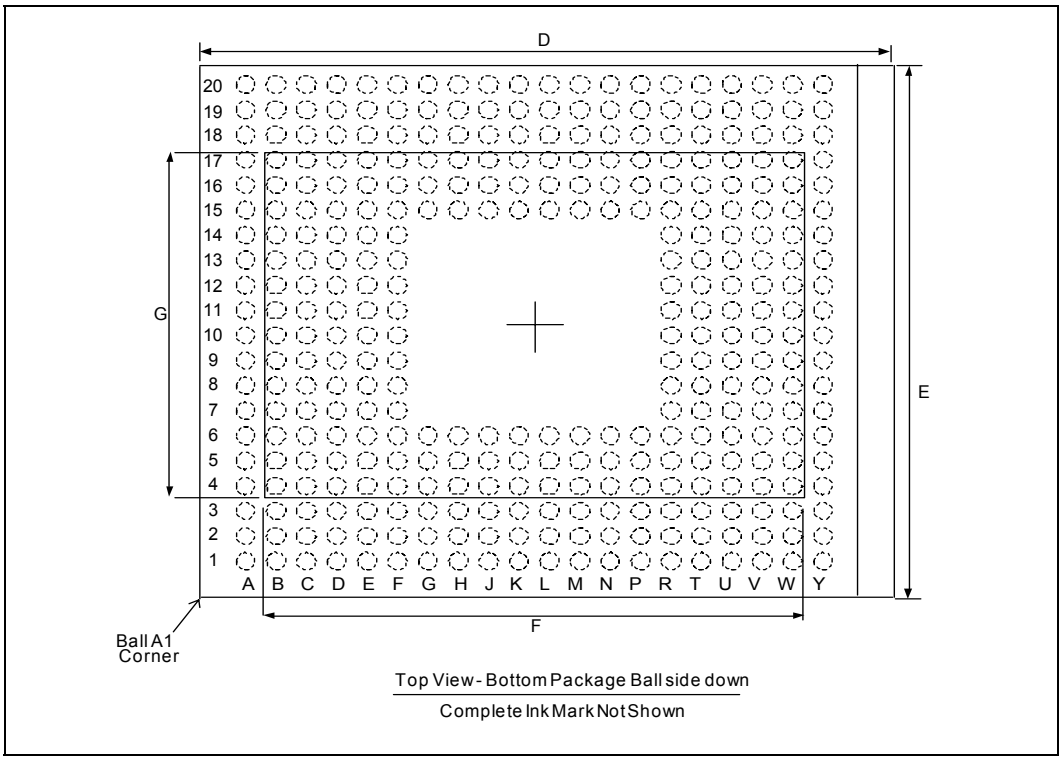


Figure 3-3. 14 x 14-mm Intel® PXA27x Processor Family Package, Side View

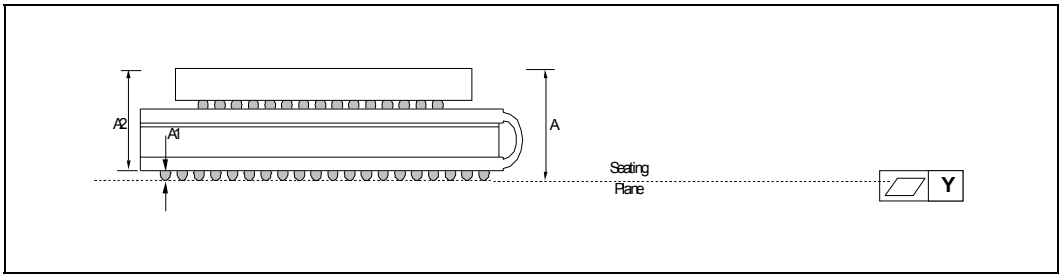


Table 3-1. Intel® PXA27x Processor Family Package Information (Sheet 1 of 2)

Dimension	Symbol	Min	Typical	Max
Pacakge Height	A			1.55
Ball Height	A1	0.180		
Package Body Thickness	A2	1.121		1.195
Ball (Lead) Width	b	0.350	0.4	0.450
Bottom Package Body Width	D	13.9	14	14.1
Bottom Package Body Length	E	13.9	14	14.1

Table 3-1. Intel® PXA27x Processor Family Package Information (Sheet 2 of 2)

Dimension	Symbol	Min	Typical	Max
Top Package Body Width	F	10.9	11	11.1
Top Package Body Length	G	12.9	13	13.1
Pitch	[e]		0.650	
Ball (Lead) Count	N		336	
Seating Plane Coplanarity	Y			0.150
Corner to Ball A1 Distance Along D	S1		0.825	
Corner to Ball A1 Distance Along E	S2		0.825	

Table 3-2 describes the basic material properties of the processor components.

Component	PXA271 FSCSP Material	PXA272 FSCSP Material
Mold compound	ShinEtsu KMC 2500 VAT1	ShinEtsu KMC 2500 VAT1
Solder balls(Leaded)	63% Sn/37% Pb	63% Sn/37% Pb
Solder balls(Pb-free)	N/A	94.5% Sn/5.0% Ag/0.5% Cu

3.3 Junction To Case Temperature Thermal Resistance

Parameter	Value and Units
Theta Jc	2 degrees C/watt

3.4 Processor Markings

Figure 3-4 details the processor top markings, which identify the Intel PXA27x processor family in the 336-pin package. Refer to Table 3-1 for product information.

Figure 3-4. Processor Markings, Intel® PXA27x Processor Family

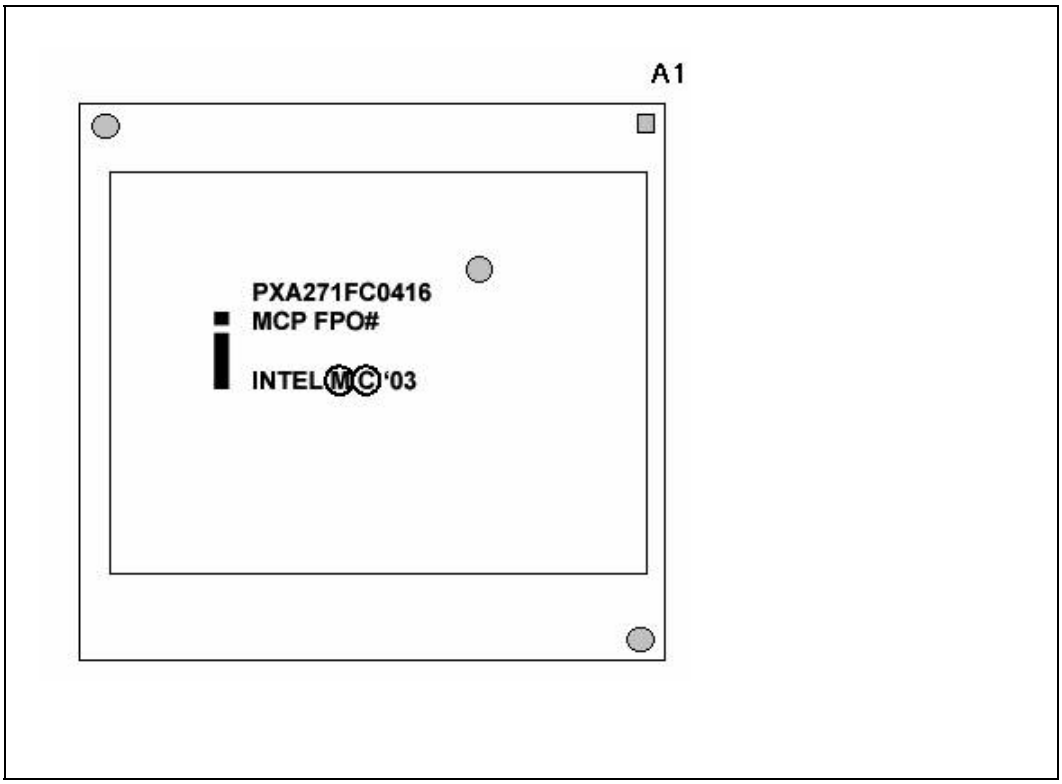
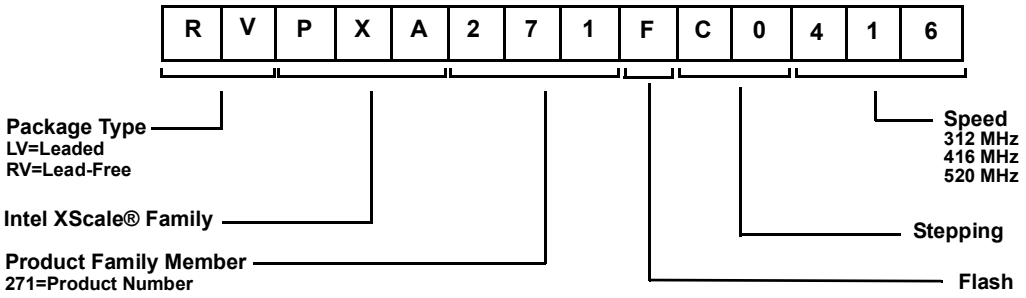


Figure 3-5. Intel® PXA27x Product Information Decoder



3.5 Intel® PXA27x Processor Family Identification Markings

Table 3-2 shows the stacked memory configuration for each of the Intel PXA27x processor family packages.

Table 3-2. Intel® PXA27x Processor Family ID Markings

PXA	PXA27x Package Stepping	Level 1 Name[1]	Apps Processor CPU Stepping	Stacked Memory Configuration	Reference Documentation
PXA271	C0	LVPXA271FC0	C0	1x256 Mbit x 16 Flash + 1x256 Mbit x 16 SDRAM	-*Intel® PXA27x Memory Subsytem (x16) with LPSDRAM Data Sheet* Order No. 301855-001 -*Intel® PXA27x Memory Subsystem (x32) Data Sheet* Order No. 301854-001
PXA272	C0	LVPXA272FC0	C0	2x256Mbit x 32 Flash	

NOTES:
1. From Top Package markings in figures above

3.6 Tray Drawing

For tray drawing information, refer to the Intel Developer website for the *Intel® Wireless Communications and Computing Package Users Guide*.

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