

EXHIBIT 22



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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|--|-------------|----------------------|---------------------|------------------|
| 11/173,565 | 07/01/2005 | Brian J. Campbell | 5888-00500 | 8561 |
| 35690 | 7590 | 09/10/2007 | EXAMINER | |
| MEYERTONS, HOOD, KIVLIN, KOWERT & GOETZEL, P.C. P.O. BOX 398 AUSTIN, TX 78767-0398 | | | NGUYEN, HIEN N | |
| | | | ART UNIT | PAPER NUMBER |
| | | | 2824 | |
| | | | MAIL DATE | DELIVERY MODE |
| | | | 09/10/2007 | PAPER |

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

DETAILED ACTION

Election/Restrictions

1. **Claims 15-20** are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected claims of Group II, there being no allowable generic or linking claim. Election was made without traverse in the reply filed on **7/18/07**.
2. Applicant's election without traverse of **Group I (claims 1-14)** in the reply filed on **7/18/07** is acknowledged.
3. **Claims 1-14** are presented for examining.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. **Claims 1-14** are rejected under 35 U.S.C. 102(e) as being anticipated by U.S.

Patent No. 7,120,061 issued to **Daga**.

- **Regarding claim 1**, Daga figures 3-8 show an integrated circuit (400) comprising at least one logic circuit (420) supplied by a **first supply voltage (405, Ext VDD)** , and at least one memory circuit (430) coupled to the logic circuit

and supplied by a **second supply voltage (415, Hi VDD)**, and wherein the memory circuit is configured to be read and written responsive to the logic circuit even if the first supply voltage is less than the second supply voltage during use. **See column 3, lines 35-53.** In here, the high voltage level (415) during “writing mode” **is higher than** the external voltage (405) during “read mode” renders the limitation “*the first voltage supply voltage*” is *less than “the second supply voltage”*.

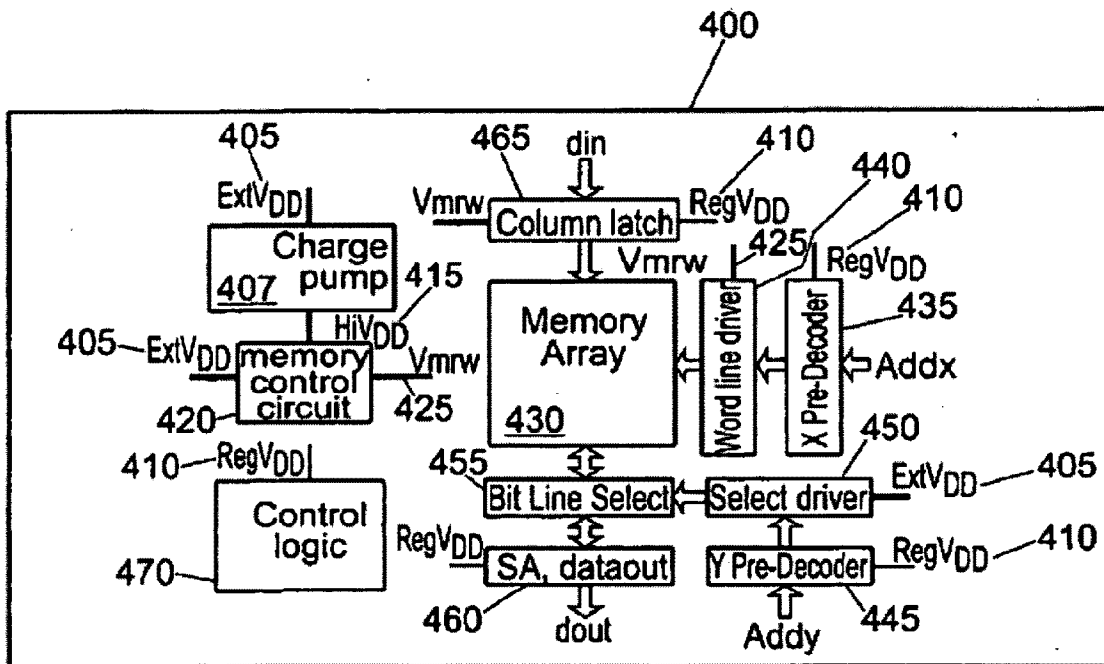


FIG. 4

- Regarding claims 2 and 3, the memory circuit is supplied by first supply voltage (405) in addition to second supply voltage (415) through the word

Art Unit: 2824

line driver (440) in order for the memory cells to be accessed. Column 3, lines 47-53, and Figure 6.

- **Regarding claim 4**, a level shifter circuit (525) supplied with the second supply voltage (here the variable voltage V_{mrw} , 505), wherein the level shifter circuit is coupled to receive an input signal (Read, 535) from the logic circuit and to level shift the input signal to the second supply voltage from the first supply voltage (405), and wherein the level shifter circuit is coupled to provide the level-shifted signal to the word line driver circuit. See column 4, lines 8-40).

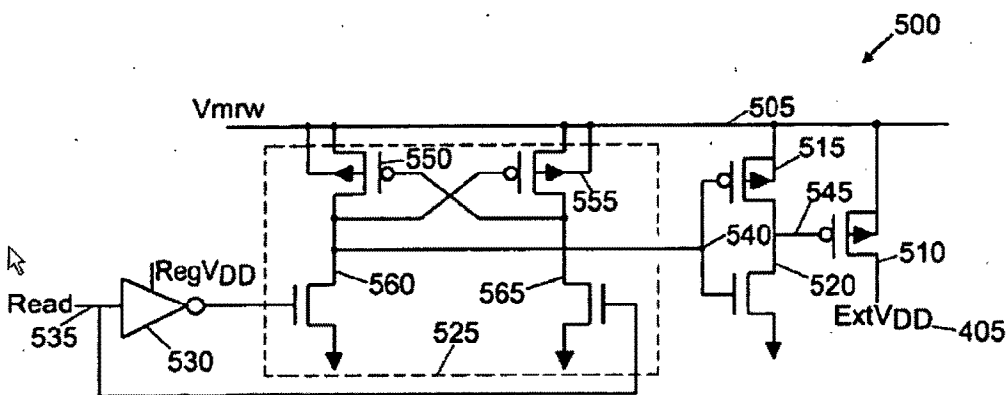


FIG. 5

- **Regarding claim 5**, the input signal comprises a clock signal (from the ADDX, see figure 6). wherein the clock signal triggers a **precharge** (see column 7, lines 10-30 and flow chart Fig. 9).

- **Regarding claim 6**, the word line driver circuit is further coupled to receive one or more additional input signals that are not level shifted. (by level shifter 625).

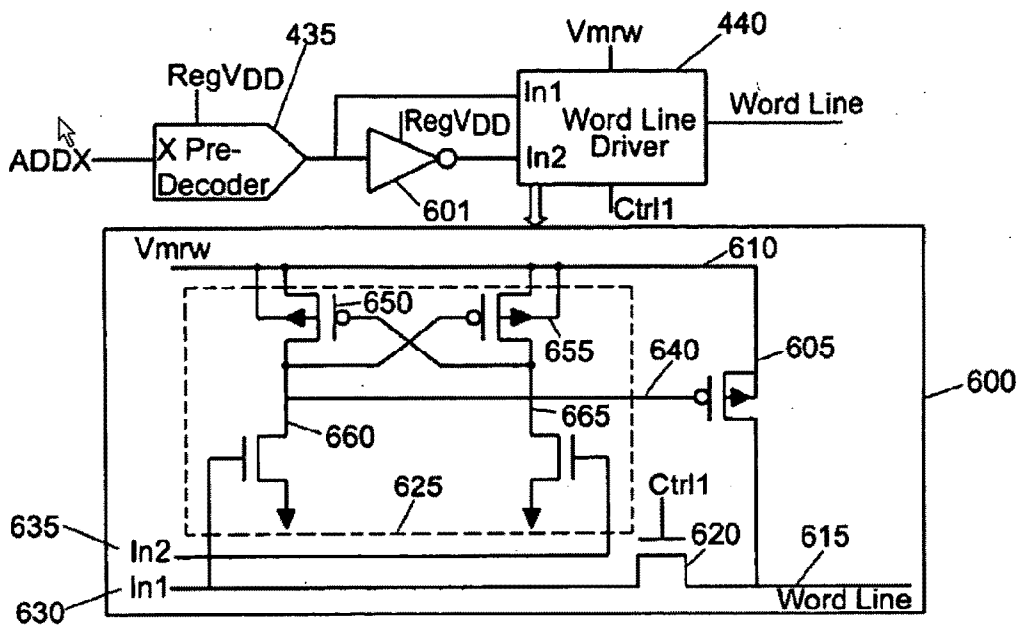


FIG. 6

- **Regarding claim 7**, the level shifter circuit comprises an output inverter (550) comprising a series connection of two n-type (NMOS) transistors (560, 565), wherein a gate of a first of the NMOS transistors is coupled to receive the level-shifted signal, and wherein a gate of a second of the NMOS transistors is coupled to the first supply voltage (through the line 505). See figure 5.
- **Regarding claim 8**, a first of the PMOS (555) is coupled to receive the level-shifted signal, and wherein a gate of a second of the PMOS (550) is coupled to the first supply voltage (**Vmrw**). The voltage Vmrw is a variable voltage which

Art Unit: 2824

can be set at first or second supply voltage by a charge pump. (column 3, lines 30-34).

- **Regarding claims 9 and 10**, see figure 6 and 7 wherein the memory circuit comprises a **bit line driver circuit (800)** coupled to the pair of bit lines (Fig. 6) and configured to drive the pair of bit lines to write the first memory cell, and wherein the bit line driver circuit is supplied with **first supply voltage (Ext VDD)**.

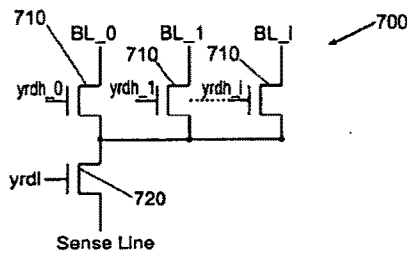


FIG. 7

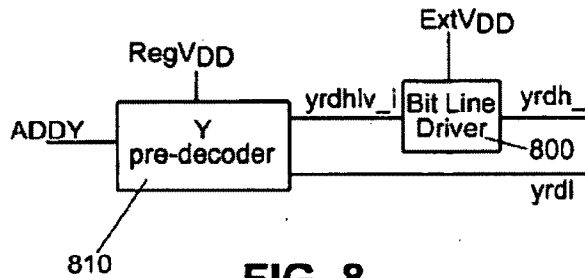


FIG. 8

- **Regarding claims 11 and 12**, Figure 9 show a flow chart that discuss a precharge circuit to to precharge the pair of bit lines to prepare for the read (950) to store (960) or hold (970) during periods of inactivity the first supply voltage. See column 7, lines 10-30.
- **Regarding the method as claimed in claims 13-14**, the apparatus of figure 4 is capable to perform the function of reading *“using signals that are referenced to the first supply voltage, wherein the memory cell is supplied with a second supply voltage that is greater than the first supply voltage during use”* as discussed in paragraph 4 (claims 1-12) above.

Conclusion

Art Unit: 2824

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Chow et al (6,920,060) and Jyouno et al (7,245,532) which disclose various method of operating a memory device are cited as of interest.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hien N. Nguyen whose telephone number is (571) 272-1879. The examiner can normally be reached on Monday through Thursday 9:30 AM to 7:00 PM..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

H. Nguyen
August 27, 2007

Hien Nguyen
Patent Examiner

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| | Filing Date | | 2005-07-01 | |
| | First Named Inventor | Brian J. Campbell | | |
| | Art Unit | 2818 2824 | | |
| | Examiner Name | Unknown <i>H. NGUYEN</i> | | |
| | Attorney Docket Number | 5888-00500 | | |

| U.S. PATENTS | | | | | | |
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| Examiner Initial* | Cite No | Patent Number | Kind Code ¹ | Issue Date | Name of Patentee or Applicant of cited Document | Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear |
| <i>HN</i> | 1 | 6501306 | | 2002-12-31 | Soo-Hwan, et al. | |
| <i>HN</i> | 2 | 5450365 | | 1995-09-12 | Kaoru | |
| <i>HN</i> | 3 | 4879690 | | 1989-11-07 | Kenji, et al. | |

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| HW | 1 | International Search Report and Written Opinion for PCT/US2006/026098, mailed November 23, 2006, 11 pages. | <input type="checkbox"/> |

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| HN | 2 | 7098692 | | 2006-08-29 | Joshi et al | | | |
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| Examiner Name | Unknown | H. NGUYEN | |
| Attorney Docket Number | 5888-00500 | | |

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| HJ | 1 | P.A. Semi, "The PWRficient Processor Family," January 2006, pp. 1-31. | <input type="checkbox"/> |
| HJ | 2 | U.S. Patent Application No. 11/160,236, filed December 13, 2006. | <input type="checkbox"/> |

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| Notice of References Cited | Application/Control No. 11/173,565 | Applicant(s)/Patent Under Reexamination CAMPBELL ET AL. | |
| | Examiner Hien N. Nguyen | Art Unit 2824 | Page 1 of 1 |

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| * | B US-6,920,060 | 07-2005 | Chow et al. | 365/145 |
| * | C US-7,245,532 | 07-2007 | Jyouno et al. | 365/185.08 |
| | D US- | | | |
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Index of Claims



Application/Control No.

11/173,565

Examiner

Hien N. Nguyen

Applicant(s)/Patent under Reexamination

CAMPBELL ET AL.

Art Unit

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CONFIRMATION NO. 8561

Table with 5 columns: SERIAL NUMBER (11/173,565), FILING OR 371(c) DATE (07/01/2005), CLASS (365), GROUP ART UNIT (2824), ATTORNEY DOCKET NO. (5888-00500)

APPLICANTS
Brian J. Campbell, Sunnyvale, CA;
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Daniel C. Murray, Morgan Hill, CA;
Gregory S. Scott, Santa Clara, CA;
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IF REQUIRED, FOREIGN FILING LICENSE GRANTED **
07/25/2005

Table with 5 columns: Foreign Priority claimed (no), 35 USC 119 (a-d) conditions met (no), STATE OR COUNTRY (CA), SHEETS DRAWING (4), TOTAL CLAIMS (20), INDEPENDENT CLAIMS (2)

ADDRESS
35690

TITLE
Integrated circuit with separate supply voltage for memory that is different from logic circuit supply voltage

Table with 2 columns: FILING FEE RECEIVED (1000), FEES: Authority has been given in Paper No. to charge/credit DEPOSIT ACCOUNT No. for following: (List of fee options: All Fees, 1.16 Fees (Filing), 1.17 Fees (Processing Ext. of time), 1.18 Fees (Issue), Other, Credit)