EXHIBIT 23

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 11/173,565	§	Examiner:	Nguyen, Hien N.
Filed: July 1, 2005	§	Group/Art Unit:	2824
Inventor(s):	§	Atty. Dkt. No:	5888-00500
Brian J. Campbell, Vincent R. von Kaenel, Daniel C. Murray, Gregory S. Scott, and Sribalan Santhanam	§		
Title: Integrated Circuit with Separate Supply Voltage for Memory That is Different from Logic Circuit Supply Voltage	§		

RESPONSE TO OFFICE ACTION OF
September 10, 2005

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This paper is submitted in response to the Office Action of September 10, 2005, to further highlight why the application is in condition for allowance.

Please amend the case as listed below.

IN THE CLAIMS:

Please amend the claims as set forth below:

1. (Currently Amended) An integrated circuit comprising:

at least one logic circuit supplied by a first supply voltage received on a first input to the integrated circuit; and

at least one memory circuit coupled to the logic circuit and supplied by a second supply voltage received on a second input to the integrated circuit, and wherein the memory circuit is configured to be read and written responsive to the logic circuit even if the first supply voltage is less than the second supply voltage during use, and wherein the memory circuit comprises at least one memory array, and wherein the memory array comprises a plurality of memory cells that are continuously supplied by the second supply voltage during use.

2. (Original) The integrated circuit as recited in claim 1 wherein the memory circuit is supplied by the first supply voltage in addition to the second supply voltage.

3. (Currently Amended) The integrated circuit as recited in claim 1 wherein the memory circuit comprises ~~a first memory cell supplied by the second supply voltage and~~ a word line driver circuit supplied by the second supply voltage, wherein ~~the~~ a first memory cell of the plurality of memory cells is coupled to receive a word line from the word line driver circuit to activate the first memory cell for access.

4. (Original) The integrated circuit as recited in claim 3 wherein the memory circuit further comprises a level shifter circuit supplied with the second supply voltage, wherein the level shifter circuit is coupled to receive an input signal from the logic circuit and to level shift the input signal to the second supply voltage from the first supply voltage, and wherein the level shifter circuit is coupled to provide the level-shifted signal to the word

line driver circuit.

5. (Original) The integrated circuit as recited in claim 4 wherein the input signal comprises a clock signal, and wherein the word line driver circuit comprises a dynamic logic circuit, and wherein the clock signal triggers a precharge of the dynamic logic circuit.

6. (Original) The integrated circuit as recited in claim 5 wherein the word line driver circuit is further coupled to receive one or more additional input signals that are not level shifted.

7. (Original) The integrated circuit as recited in claim 4 wherein the level shifter circuit comprises an output inverter comprising a series connection of two n-type metal oxide semiconductor (NMOS) transistors, wherein a gate of a first of the NMOS transistors is coupled to receive the level-shifted signal, and wherein a gate of a second of the NMOS transistors is coupled to the first supply voltage.

8. (Original) The integrated circuit as recited in claim 7 wherein the output inverter further comprises a series connection of two p-type metal oxide semiconductor (PMOS) transistors, wherein a gate of a first of the PMOS transistors is coupled to receive the level-shifted signal, and wherein a gate of a second of the PMOS transistors is coupled to the first supply voltage, and wherein a source of the second of the PMOS transistors is coupled to the second supply voltage.

9. (Original) The integrated circuit as recited in claim 3 wherein the first memory cell is coupled to a pair of bit lines, and wherein the memory circuit comprises a bit line driver circuit coupled to the pair of bit lines and configured to drive the pair of bit lines to write the first memory cell, and wherein the bit line driver circuit is supplied with the first supply voltage.

10. (Original) The integrated circuit as recited in claim 3 wherein the first memory cell is

coupled to a pair of bit lines, and wherein the memory circuit comprises a sense amplifier circuit coupled to the pair of bit lines and configured to sense a value of the first memory cell for output in response to a read, and wherein the sense amplifier circuit is supplied with the first supply voltage.

11. (Original) The integrated circuit as recited in claim 10 wherein the memory circuit further comprises a bit line precharge circuit configured to precharge the pair of bit lines to prepare for the read, and wherein the bit line precharge circuit is supplied by the first supply voltage.

12. (Original) The integrated circuit as recited in claim 11 wherein the memory circuit further comprises a bit line hold circuit configured to hold the precharge on the pair of bit lines during periods of inactivity, and wherein the bit line hold circuit is supplied by the first supply voltage.

13. (Currently Amended) A method comprising:

a logic circuit reading a memory cell, the logic circuit supplied by a first supply voltage received on a first input to the integrated circuit; and

the memory cell responding to the read using signals that are referenced to the first supply voltage, wherein the memory cell is supplied with a second supply voltage that is greater than the first supply voltage during use, and wherein the second supply voltage is received on a second input to the integrated circuit, and wherein the memory circuit comprises at least one memory array, and wherein the memory array comprises a plurality of memory cells that are continuously supplied by the second supply voltage during use.

14. (Original) The method as recited in claim 13 further comprising:

the logic circuit writing the memory cell using signals that are referenced to the first supply voltage; and

the memory cell storing the write data from the logic circuit.

15-20. (Cancelled)

21. (New) An integrated circuit comprising:

at least one logic circuit supplied by a first supply voltage; and

at least one memory circuit coupled to the logic circuit and supplied by a second supply voltage, and wherein the memory circuit is configured to be read and written responsive to the logic circuit even if the first supply voltage is less than the second supply voltage during use, and wherein the memory circuit comprises a first memory cell supplied by the second supply voltage and a word line driver circuit supplied by the second supply voltage, wherein the first memory cell is coupled to receive a word line from the word line driver circuit to select the first memory cell for access, and wherein the memory circuit further comprises a level shifter circuit supplied with the second supply voltage, wherein the level shifter circuit is coupled to receive a clock signal from the logic circuit and to level shift the clock signal to the second supply voltage from the first supply voltage, and wherein the level shifter circuit is coupled to provide the level-shifted clock signal to the word line driver circuit, and wherein the word line driver circuit comprises a dynamic logic circuit, and wherein the clock signal triggers a precharge of the dynamic logic circuit.

22. (New) The integrated circuit as recited in claim 21 wherein the word line driver circuit is further coupled to receive one or more additional input signals that are not level shifted.

23. (New) The integrated circuit as recited in claim 21 wherein the level shifter circuit comprises an output inverter comprising a series connection of two n-type metal oxide semiconductor (NMOS) transistors, wherein a gate of a first of the NMOS transistors is coupled to receive the level-shifted signal, and wherein a gate of a second of the NMOS transistors is coupled to the first supply voltage.

24. (New) The integrated circuit as recited in claim 23 wherein the output inverter further comprises a series connection of two p-type metal oxide semiconductor (PMOS) transistors, wherein a gate of a first of the PMOS transistors is coupled to receive the level-shifted signal, and wherein a gate of a second of the PMOS transistors is coupled to the first supply voltage, and wherein a source of the second of the PMOS transistors is coupled to the second supply voltage.

REMARKS

After entry of this amendment, claims 1-14 and 21-24 are pending. In the present Office Action, claims 1-14 were rejected under 35 U.S.C. § 102(e) as being anticipated by Daga, U.S. Patent No. 7,120,061 ("Daga"). Applicants respectfully traverse this rejection and request reconsideration.

Claims 1-14

Applicants respectfully submit that claims 1-14 recite combinations of features not taught or suggested in the cited art. For example, claim 1 recites a combination of features including: "the memory circuit comprises at least one memory array, and wherein the memory array comprises a plurality of memory cells that are continuously supplied by the second supply voltage during use". Daga does not anticipate the above highlighted features.

Daga teaches a non-volatile memory such as an EEPROM or Flash memory (see, e.g., Daga, col. 3, lines 20-24). In such memories, the memory array does not include memory cells that are continuously supplied with a supply voltage during use. Indeed, the memory arrays are designed to retain values without any power applied (hence the "nonvolatile" nature of such cells). Instead, some sort of charge storage is used, such as a floating gate structure.

Daga teaches his memory array 430 without any power supply inputs. (See, e.g., Fig. 4 and its description where no power supply is provided to the memory array 430). Instead, the memory array receives word lines from the word line driver circuit to select a line of storage to output data, and the stored charge in the memory array provides the data on the bit lines. The bit line select circuit then selects the bit(s) of interest to be provided to the senseamp circuit. (See, e.g., Daga, col. 3, lines 43-64). For a write, the data is driven by the column latch 465 on the bit lines into the memory array (See, e.g., Daga, col. 3, lines 1-6). Accordingly, Daga's memory array is not supplied with a power supply voltage.

Furthermore, the word lines (and bit lines) are only active during reads and writes. Thus, when no read or write is being performed, there is no voltage of any sort applied to Daga's memory array 430 (e.g. there is not power supply voltage and there is no input signal voltage either). These teachings fail to teach or suggest "the memory circuit comprises at least one memory array, and wherein the memory array comprises a plurality of memory cells that are continuously supplied by the second supply voltage during use."

Furthermore, Daga's integrated circuit has only one power supply input to the integrated circuit ($ExtV_{DD}$, see Fig. 3). Thus, Daga fails to anticipate "a first supply voltage received on a first input to the integrated circuit; and … a second supply voltage received on a second input to the integrated circuit" as recited in claim 1.

For at least the above stated reasons, Applicants submit that claim 1 is patentable over the cited art. Claim 13 recites a combination of features including features similar to those highlighted above with regard to claim 1. Accordingly, claim 13 is patentable over the cited art as well. Claims 2-12 and 14 depend from claims 1 or 13 and recite additional combinations of features not taught or suggested in the cited art.

New Claims 21-24

Applicants respectfully submit that new claims 21-24 recite combinations of features not taught or suggested in the cited art. For example, claim 21 recites a combination of features including: "the level shifter circuit is coupled to receive a clock signal from the logic circuit and to level shift the clock signal to the second supply voltage from the first supply voltage, and wherein the level shifter circuit is coupled to provide the level-shifted clock signal to the word line driver circuit, and wherein the word line driver circuit comprises a dynamic logic circuit, and wherein the clock signal triggers a precharge of the dynamic logic circuit."

Claim 21 is essentially originally-filed claim 5, rewritten in independent form. With regard to claim 5, the Office Action asserted that Daga anticipated a clock signal

with the ADDX input in Fig. 6, and the precharge mentioned in Fig. 9 and its description in col. 7, lines 10-30. Applicants respectfully disagree. The ADDX input is an address: "X pre-decoder receives and decodes an address" (Daga, col. 3, lines 44-45). The address is not a clock. Furthermore, nothing teachings that the word line driver circuit is a dynamic logic circuit that has a precharge triggered by the address input. The word line driver circuit in Fig. 6 (element 600) is not a dynamic circuit and there is no precharge. The description at col. 7, lines 10-30 mentions the precharge of the word line (but not the word line driver circuit), and does not describe how that precharge is triggered, merely saying it occurs during a memory read (See Daga, col. 7, lines 23-24).

Accordingly, Applicants submit that claim 21 is patentable over the cited art. Claims 22-24 depend from claim 21 and recite additional combinations of features not taught or suggested in the cited art.

CONCLUSION

Applicants submit the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5888-00500/LJM.

Also enclosed herewith are the following items:

Respectfully submitted,

/Lawrence J. Merkel/
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