EXHIBIT 30

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/179,814	06/24/2002	Anthony M. Fadell	APL225	4934

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EXAMINER	
VU, TRISHA U	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 11/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/179,814	FADELL ET AL.	
	Examiner	Art Unit	
	Trisha U. Vu	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02-19-03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-18 are presented for examination.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: reference number **100** (page 6, line 22), reference number **108** (page 6, line 24), reference number **122** (page 7, line 10). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-2, 5-8, 11-14, and 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bruce et al. (WO 01/67457 A1) (hereinafter Bruce) in view of Burrows (US Patent No. 6,377,530).

As to claim 1, Bruce teaches an apparatus for providing a direct connection between an external memory source and a local solid state memory (50) in order to facilitate a high speed data transfer in a system that includes a central processing unit (52) connected to a main system bus (72), comprising: a direct memory access (DMA) bus (70); a local solid state memory (50) coupled to the DMA bus; a port receptor connected to the DMA bus arranged to receive an external connector (page 8, line 26-35); a direct memory access bus switch (interface 49) coupled by way of the DMA bus to the CPU that provides a direct connection between the port receptor and the solid state memory by way of the DMA bus only thereby bypassing the main system bus and the CPU when an appropriate data transfer request is received and processed by the CPU such that the high speed data transfer between the port receptor and the solid state memory is provided only when the appropriate data transfer request is received and processed by the CPU (Fig. 3 and page 7 line 32 to page 8 line 19). However, Bruce does not explicitly disclose the solid state memory includes hard disk drive (HDD). Burrows teaches implementing HDD (col. 3, lines 37-56). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include HDD as taught by Burrows in the system of Bruce to enables the portable device to store a large amount of data while maintaining an acceptable level of power consumption and an optimal data retrieval time (col. 3, lines 37-40).

As to claim 2, Bruce further teaches until the appropriate data transfer request is received and processed by the CPU, the CPU is directly connected to the HDD (Fig. 3).

As to claim 5, Bruce further teaches a memory device (SDRAM, Flash memory) coupled to the DMA bus (page3, lines 15-18).

As to claim 6, Bruce further teaches the memory device is selected from a group comprising: an SDRAM device, a Flash ROM device, and an EPROM device (page3, lines 15-18).

As to claim 7, Bruce teaches a method for providing a direct connection between an external memory source and a local solid state memory in order to facilitate a high speed data transfer in a system that includes a central processing unit (52) connected to a main system bus (72), comprising: providing a direct memory access (DMA) bus (70); coupling a local solid state memory to the DMA bus; connecting a port receptor to the DMA bus arranged to receive an external connector (page 8, line 26-35); coupling a direct memory access bus switch bus to the CPU by way of the DMA; only when an appropriate data transfer request is received and processed by the CPU, providing a direct connection between the port receptor and the solid state memory by way of the DMA bus only thereby bypassing the main system bus and the CPU; and providing the high speed data transfer between the port receptor and the solid state memory (Fig. 3 and page 7 line 32 to page 8 line 19). However, Bruce does not explicitly disclose the solid state memory includes hard disk drive (HDD). Burrows teaches implementing HDD (col. 3, lines 37-56). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include HDD as taught by Burrows in the system of Bruce to

enables the portable device to store a large amount of data while maintaining an acceptable level of power consumption and an optimal data retrieval time (col. 3, lines 37-40).

As to claim 8, Bruce further teaches directly connecting the CPU to the HDD until the appropriate data transfer request is received and processed by the CPU (Fig. 3).

As to claim 11, Bruce further teaches a memory device (SDRAM, Flash memory) coupled to the DMA bus (page3, lines 15-18).

As to claim 12, Bruce further teaches the memory device is selected from a group comprising: an SDRAM device, a Flash ROM device, and an EPROM device (page3, lines 15-18).

As to claim 13, Bruce further teaches an apparatus for providing a direct connection between an external memory source and a local hard drive in order to facilitate a high speed data transfer in a system that includes a central processing unit (52) connected to a main system bus (72), comprising: means for providing a direct memory access (DMA) bus (70); means for coupling a local solid state memory to the DMA bus; means for connecting a port receptor to the DMA bus arranged to receive an external connector (page 8, line 26-35); means for coupling a direct memory access bus switch bus to the CPU by way of the DMA; only when an appropriate data transfer request is received and processed by the CPU, means for providing a direct connection between the port receptor and the solid state memory by way of the DMA bus only thereby bypassing the main system bus and the CPU; and means for providing the high speed data transfer between the port receptor and the solid state memory (Fig. 3 and page 7 line 32 to page 8

line 19). However, Bruce does not explicitly disclose the solid state memory includes hard disk drive (HDD). Burrows teaches implementing HDD (col. 3, lines 37-56). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include HDD as taught by Burrows in the system of Bruce to enables the portable device to store a large amount of data while maintaining an acceptable level of power consumption and an optimal data retrieval time (col. 3, lines 37-40).

As to claim 14, Bruce further teaches means for directly connecting the CPU to the HDD until the appropriate data transfer request is received and processed by the CPU (Fig. 3).

As to claim 17, Bruce further teaches a memory device (SDRAM, Flash memory) coupled to the DMA bus (page3, lines 15-18).

As to claim 18, Bruce further teaches the memory device is selected from a group comprising: an SDRAM device, a Flash ROM device, and an EPROM device (page3, lines 15-18).

4. Claims 3-4, 9-10, and 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bruce et al. (WO 01/67457 A1) (hereinafter Bruce) in view of Burrows (US Patent No. 6,377,530), and further in view of Okawa (US Patent No. 6,804,263).

As to claims 3 and 4, the argument above for claim 1 applies. However, Bruce and Burrows do not explicitly disclose the port receptor is a FireWire port receptor and the apparatus is incorporated into a portable FireWire enable device. Okawa teaches portable FireWire enable device and Fire Wire port receptor (at least col. 1, lines 17-34).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the apparatus to be portable FireWire enable device having Fire Wire port receptor as taught by Okawa in the system of Bruce and Burrows because FireWire provides high speed data transmission and real-time transfer of data (col. 1, lines 17-25).

As to claims 9 and 10, the argument above for claim 7 applies. However, Bruce and Burrows do not explicitly disclose the port receptor is a FireWire port receptor and the system is incorporated into a portable FireWire enable device. Okawa teaches portable FireWire enable device and Fire Wire port receptor (at least col. 1, lines 17-34). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the system to be portable FireWire enable device having Fire Wire port receptor as taught by Okawa in the system of Bruce and Burrows because FireWire provides high speed data transmission and real-time transfer of data (col. 1, lines 17-25).

As to claims 15 and 16, the argument above for claim 13 applies. However, Bruce and Burrows do not explicitly disclose the port receptor is a FireWire port receptor and the system is incorporated into a portable FireWire enable device. Okawa teaches portable FireWire enable device and Fire Wire port receptor (at least col. 1, lines 17-34). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the system to be portable FireWire enable device having Fire Wire port receptor as taught by Okawa in the system of Bruce and Burrows because

FireWire provides high speed data transmission and real-time transfer of data (col. 1, lines 17-25).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, as the art disclose DMA communication:

US Patent	5,828,856	Bowes et al.
US Patent	6,718,405	Rogers
US Patent	6,078,742	Chow
US Patent	6,249,833	Takahashi
US Patent	6,658,520	Bennett
US Patent	6,701,405	Adusumilli et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trisha U. Vu whose telephone number is 571-272-3643. The examiner can normally be reached on Mon-Thur and alternate Fri from 8:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trisha U. Vu
Examiner
Art Unit 2112

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TRISHA VU
PRIMARY EXAMINER