EXHIBIT 31

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Robbin et al

Application No.: 10/179,814

Filed: June 24, 2002

Title: METHODS AND APPARATUS FOR PROVIDING AUTOMATIC HIGH SPEED DATA CONNECTION IN A PORTABLE DEVICE (AS AMENDED)

Attorney Docket No.: APL1P225

Examiner: Vu, Trisha U

Group: 2112

Confirmation No.: 4934

CERTIFICATE OF FACSIMILE TRANSMISSION
I hereby certify that this correspondence is being transmitted by facsimile to fax number 703-872-9306 to the U.S. Patent and Trademark Office on March 4, 2005.

Signed: _____
Agnes Spence

AMENDMENT A

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated November 5, 2004, please amend the above-identified patent application as follows:

Amendment to the Specification is found on page 2 of this paper.

Listing of Pending Claims are found starting at page 3 of this paper.

Remarks/Arguments begin on page 9 of this paper.

IN THE SPECIFICATION

Please replace the title with as follows:

--METHODS AND APPARATUS FOR PROVIDING AUTOMATIC HIGH SPEED DATA CONNECTION IN ~~A FIREWIRE ENABLED~~ PORTABLE ~~MULTIMEDIA~~ DEVICE--

PENDING CLAIMS

1. (Currently Amended) An apparatus for providing a direct connection between an external memory source and a local hard drive in order to facilitate a high speed data transfer in a system that includes a central processing unit (CPU) connected to a main system bus, comprising:

a direct memory access (DMA) bus;

a local hard drive (HDD) coupled to the DMA bus;

a port receptor connected to the DMA bus arranged to receive an external connector;

a direct memory access bus switch coupled by way of the DMA bus to the CPU that provides a direct connection between the port receptor and the HDD by way of the DMA bus **wherein when the direct memory access bus switch provides the direct connection between the port receptor and the HDD by way of the DMA bus, the CPU is unable to access the HDDonly thereby bypassing the main system bus and the CPU when an appropriate data transfer request is received and processed by the CPU such that the high speed data transfer between the port receptor and the HDD is provided only when the appropriate data transfer request is received and processed by the CPU**.

2. (Currently Amended) An apparatus as recited in claim 1, further comprising:

until the **direct memory access bus switch provides the direct connection between the port receptor and the HDD by way of the DMA bus** ~~appropriate data transfer request is received and processed by the CPU~~, the CPU is directly connected to the HDD.

3. (Original) An apparatus as recited in claim 1, wherein the port receptor is a FireWire port receptor.

4. (Original) An apparatus as recited in claim 1, wherein the apparatus is incorporated into a portable FireWire enabled device.

5. (Cancelled)

6. (Cancelled)

7. (Currently Amended) A method for providing a direct connection between an external memory source and a local hard drive in order to facilitate a high speed data transfer in a system that includes a central processing unit (CPU) connected to a main system bus, comprising:

providing a direct memory access (DMA) bus;

coupling a local hard drive (HDD) to the DMA bus;

connecting a port receptor to the DMA bus arranged to receive an external connector;

coupling a direct memory access bus switch bus to the CPU by way of the DMA;

only when an appropriate data transfer request is received and processed by the CPU,

providing a direct connection between the port receptor and the HDD by way of the DMA bus **during which the CPU is unable to access the HDD.** ~~**only thereby bypassing the main system bus and the CPU; and**~~

~~**providing the high-speed data transfer between the port receptor and the HDD.**~~

8. (Original) A method as recited in claim 7, further comprising:

directly connecting the CPU to the HDD until the appropriate data transfer request is received and processed by the CPU.

9. (Original) A method as recited in claim 7, wherein the port receptor is a FireWire port receptor.

10. (Original) A method as recited in claim 7, wherein the system is incorporated into a portable FireWire enabled device.

11. (Cancelled)

12. (Cancelled)

13. (Currently Amended) An apparatus for providing a direct connection between an external memory source and a local hard drive in order to facilitate a high speed data transfer in a system that includes a central processing unit (CPU) connected to a main system bus, comprising:

means for providing a direct memory access (DMA) bus;

means for coupling a local hard drive (HDD) to the DMA bus;

means for connecting a port receptor to the DMA bus arranged to receive an external connector;

means for coupling a direct memory access bus switch bus to the CPU by way of the DMA;

~~only when an appropriate data transfer request is received and processed by the CPU~~,

means for providing a direct connection between the port receptor and the HDD by way of the DMA bus only thereby bypassing the main system bus and the CPU **such that the CPU is unable to access the HDD.**~~; and~~

~~means for providing the high speed data transfer between the port receptor and the HDD.~~

14. (Original) An apparatus as recited in claim 13, further comprising:

means for directly connecting the CPU to the HDD until the appropriate data transfer request is received and processed by the CPU.

15. (Original) An apparatus as recited in claim 13, wherein the port receptor is a FireWire port receptor.

16. (Original) An apparatus as recited in claim 13, wherein the system is incorporated into a portable FireWire enabled device.

17. (Cancelled)

18. (Cancelled)

19. (New) In a system that includes a central processing unit (CPU) connected to a main system bus, an apparatus for providing a direct high speed data transfer connection between an external device having an external device connector and a local memory comprising:

a direct memory access (DMA) bus connected to the local memory;

a port receptor connected to the DMA bus arranged to receive the external device connector;

a high speed cable detection circuit for detecting if a high speed cable is connected to the port receptor and wherein, when the high speed cable detected, the high speed cable detection circuit generates and forwards a high speed data transfer request to the CPU; and

a direct memory access bus switch that provides the direct high speed data transfer connection between the port receptor and the local memory as directed by the CPU based upon the high speed data transfer request, wherein when the direct memory access bus switch provides the direct connection between the port receptor and the local memory, the CPU is unable to access the local memory.

20. (New) An apparatus as recited in claim 19, wherein the high speed cable is an IEEE 1394 compliant cable.

21. (New) An apparatus as recited in claim 19, wherein the local memory is selected from a group comprising: an SDRAM device, a Flash ROM device, an EPROM device, and a hard disk drive (HDD).

22. (New) In a system that includes a central processing unit (CPU) and a local memory, a method for providing a direct high speed data transfer connection between a port receptor and the local memory, comprising:

detecting a high speed cable connected at the port receptor;

generating a high speed data transfer request when the high speed cable is detected;

providing the direct high speed data transfer connection between the local memory and the port receptor based upon the high speed data transfer request; and

disabling access between the CPU and the local memory.

23. (New) A method as recited in claim 22, wherein the local memory is a hard disk drive (HDD).

24. (New) A method as recited in claim 22, wherein the port receptor is an IEEE 1394 compliant port receptor.

25. (New) A method as recited in claim 22, wherein the local memory is selected from a group comprising: an SDRAM device, a Flash ROM device, and an EPROM device.

REMARKS

A number of claims were rejected under 35 U.S.C. 103(a) as being unpatentable over Bruce et al. (WO/01/67457 A1) in view of Burrows (U.S. Patent 6,377,530). Bruce et al. describes a high speed interface for an audio player device for use with a base unit 1 (see Fig. 1) shown in a preferred embodiment in Fig. 3 as player device 42. As described in Bruce et al., the player device 42 includes a solid state memory 50, a microprocessor 52 that controls operation of the device, and an electronic interface 49 that physically connects directly to the base unit 1 via the bus 73. Bruce et al., at page 5, line 24, states:

> The electronic interface 49...enables the base unit 1 to have direct memory access (DMA) via data bus 70 to the SDRAM memory 50, thereby providing the facility to by-pass the microprocessor 52. However the interface 49 can also access the microprocessor 52 via data bus 72 and the **microprocessor 52 can access the memory 50 via bus connection 74**...(emphasis added).

In this arrangement, during the period of time that the base unit 1 is granted direct access to the memory 50, the microprocessor 52 also has access to the memory 50, thereby creating the potential for memory access conflict (and a requisite arbitration scheme to resolve any conflict) between the processor 52 and the base unit 1.

In contrast to Bruce et al., the claim 1 provides for selectively enabling a bi-directional high speed data transfer path between an external device and a system memory so as to avoid any potential conflicts during a high speed data transfer operation by effectively disabling any microprocessor/system memory access during for the duration of the high speed data transfer operation. More particularly, claim 1 states:

> a direct memory access bus switch coupled by way of the DMA bus to the CPU that provides a direct connection between the port receptor and the HDD by

> way of the DMA bus, wherein when the direct memory access bus switch provides the direct connection between the port receptor and the HDD by way of the DMA bus, **the CPU is unable to access the HDD.**
>
> (emphasis provided)

In this way, the apparatus of claim 1, in contrast to the cited reference, prevents the CPU from accessing the HDD when providing a direct connection between the port receptor and the HDD. Consequently, conflicts between the CPU and system memory are prevented during high speed data transfer.

Claim 1 is, therefore, not rendered obvious by the primary reference Bruce et al. Furthermore, the secondary reference Burrows merely provides for a system memory in the form of a hard disk drive (HDD). Thus, Burrow does not overcome the deficiencies of Bruce et al.

Accordingly, Applicants submit that claim 1 is not rendered obvious by any combination of Bruce et al. and/or Burrows and respectfully requests that the Examiner withdraw the rejection under 35 U.S. C. §103(a).

All other independent claims (i.e., claims 7, 13, 20 and 23) recite similar limitations as does claim 1 with regards to the discussion above and are, therefore, also submitted to be allowable over the cited art.

All dependent claims depend either directly or indirectly from claims 1, 7, 13, 20 and 23 and are therefore also submitted to be allowable.

CONCLUSION

Applicant believes that all pending claims are allowable and respectfully requests a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
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