EXHIBIT 32

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Fadell et al.	Attorney Docket No.: APL1P225/P2729
Application No.: 10/179,814	Examiner: Vu, Trisha U.
Filed: June 24, 2002	Group: 2112
Title: METHODS AND APPARATUS FOR PROVIDING AUTOMATIC HIGH SPEED DATA CONNECTION IN PORTABLE DEVICE (as amended)	Confirmation No.: 4934

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first-class mail on August 17, 2005 in an envelope addressed to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.

Signed: Linda L. Pollock

Linda L. Pollock

AMENDMENT B

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Final Office Action dated June 3, 2005, please consider the following response:

Listing of Pending Claims are found starting at page 2 of this paper.

Amendments to the Drawings begin on page 7 of this paper and include attached replacement sheets.

Remarks/Arguments begin on page 8 of this paper.

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Amended) An apparatus for providing a direct connection between an external memory source and a local hard drive in order to facilitate a high speed data transfer in a system that includes a central processing unit (CPU) connected to a main system bus, comprising:

a direct memory access (DMA) bus;

a local hard drive (HDD) coupled to the DMA bus;

a port receptor connected to the DMA bus arranged to receive an external connector;

a direct memory access bus switch coupled by way of the DMA bus to the CPU that provides a direct connection between the port receptor and the HDD by way of the DMA bus wherein when the direct memory access bus switch provides the direct connection between the port receptor and the HDD by way of the DMA bus, the CPU is unable to access the HDD.

2. (Previously Amended) An apparatus as recited in claim 1, further comprising:

until the direct memory access bus switch provides the direct connection between the port receptor and the HDD by way of the DMA bus, the CPU is directly connected to the HDD.

3. (Original) An apparatus as recited in claim 1, wherein the port receptor is a FireWire port receptor.

4. (Original) An apparatus as recited in claim 1, wherein the apparatus is incorporated into a portable FireWire enabled device.

5. (Cancelled)

6. (Cancelled)

7. (Currently Amended) A method for providing a direct connection between an external memory source and a local hard drive in order to facilitate a high speed data transfer in a system that includes a central processing unit (CPU) connected to a main system bus, comprising:

providing a direct memory access (DMA) bus;

coupling a local hard drive (HDD) to the DMA bus;

connecting a port receptor to the DMA bus arranged to receive an external connector;

coupling a direct memory access bus switch ~~bus~~ to the CPU by way of the DMA;

only when an appropriate data transfer request is received and processed by the CPU,

providing a direct connection between the port receptor and the HDD by way of the DMA bus during which the CPU is unable to access the HDD.

8. (Original) A method as recited in claim 7, further comprising:

directly connecting the CPU to the HDD until the appropriate data transfer request is received and processed by the CPU.

9. (Original) A method as recited in claim 7, wherein the port receptor is a FireWire port receptor.

10. (Original) A method as recited in claim 7, wherein the system is incorporated into a portable FireWire enabled device.

11. (Cancelled)

12. (Cancelled)

13. (Previously Amended) An apparatus for providing a direct connection between an external memory source and a local hard drive in order to facilitate a high speed data transfer in a system that includes a central processing unit (CPU) connected to a main system bus, comprising:

means for providing a direct memory access (DMA) bus;

means for coupling a local hard drive (HDD) to the DMA bus;

means for connecting a port receptor to the DMA bus arranged to receive an external connector;

means for coupling a direct memory access bus switch bus to the CPU by way of the DMA;

means for providing a direct connection between the port receptor and the HDD by way of the DMA bus only thereby bypassing the main system bus and the CPU such that the CPU is unable to access the HDD.

14. (Original) An apparatus as recited in claim 13, further comprising:

means for directly connecting the CPU to the HDD until the appropriate data transfer request is received and processed by the CPU.

15. (Original) An apparatus as recited in claim 13, wherein the port receptor is a FireWire port receptor.

16. (Original) An apparatus as recited in claim 13, wherein the system is incorporated into a portable FireWire enabled device.

17. (Cancelled)

18. (Cancelled)

19. (Previously Presented) In a system that includes a central processing unit (CPU) connected to a main system bus, an apparatus for providing a direct high speed data transfer connection between an external device having an external device connector and a local memory comprising:

a direct memory access (DMA) bus connected to the local memory;

a port receptor connected to the DMA bus arranged to receive the external device connector;

a high speed cable detection circuit for detecting if a high speed cable is connected to the port receptor and wherein, when the high speed cable detected, the high speed cable detection circuit generates and forwards a high speed data transfer request to the CPU; and

a direct memory access bus switch that provides the direct high speed data transfer connection between the port receptor and the local memory as directed by the CPU based upon the high speed data transfer request, wherein when the direct memory access bus switch provides the direct connection between the port receptor and the local memory, the CPU is unable to access the local memory.

20. (Previously Presented) An apparatus as recited in claim 19, wherein the high speed cable is an IEEE 1394 compliant cable.

21. (Previously Presented) An apparatus as recited in claim 19, wherein the local memory is selected from a group comprising: an SDRAM device, a Flash ROM device, an EPROM device, and a hard disk drive (HDD).

22. (Previously Presented) In a system that includes a central processing unit (CPU) and a local memory, a method for providing a direct high speed data transfer connection between a port receptor and the local memory, comprising:

detecting a high speed cable connected at the port receptor;

generating a high speed data transfer request when the high speed cable is detected;

providing the direct high speed data transfer connection between the local memory and the port receptor based upon the high speed data transfer request; and

disabling access between the CPU and the local memory.

23. (Previously Presented) A method as recited in claim 22, wherein the local memory is a hard disk drive (HDD).

24. (Previously Presented) A method as recited in claim 22, wherein the port receptor is an IEEE 1394 compliant port receptor.

25. (Previously Presented) A method as recited in claim 22, wherein the local memory is selected from a group comprising: an SDRAM device, a Flash ROM device, and an EPROM device.

Amendments to the Drawings:

The attached two (2) sheets of drawings include changes to Fig. 1 and Fig. 2. These sheets replace the original sheets including Fig. 1 and Fig. 2. In Figure 1, previously omitted reference numbers 100, 108 and 122 have been added. In Figure 2, previously omitted reference number 122 has been added.

Attachment: Replacement Sheets

REMARKS

Claims 19 and 22 were rejected under 35 U.S.C. 102(b) as being unpatentable over U.S. Patent 4,975,832 issued to Saito that describes a microcomputer system with dual DMA mode transmissions. More particularly, Saito specifically teaches a system having a CPU (12), memory (13), I/O port (11) coupled to an I/O device (17) by single bus system (15) where the "the DMA controller can cause the CPU either to be electrically coupled to the bus system for programmed CPU data transmission between the I/O device and memory, or to be uncoupled therefrom for DMA data transmission". (see Abstract) Therefore, Saito requires that during DMA data transmission, the CPU is disconnected from the bus system and unable to communicate with any devices connected thereto (required by the MODIFIED HOLD REQUEST signal).

In contrast to Saito, claim 19 provides that the CPU is **always** connected to the main system bus 116 and is therefore always in communication with any device connected thereto (such as SDRAM 110, Flash ROM 112, etc.) and is only unable to access the hard disk drive HDD 102 during the period of time in which data is being transferred directly between the port 118 and the HDD 102. In this way, the CPU 106 remains operational, in contrast to Saito, and able to interact with any device connected to the main bus 116 concurrent with the direct data transfer.

Therefore, the Applicants believe that neither claims 19 nor 22 are anticipated by Saito and respectfully request that the Examiner withdraw the 35 U.S.C. 102(b) rejections thereof.

The remaining claims were rejected under 35 U.S.C. 103(a) as being unpatentable over Saito in view of U.S. Patent 6,377,530) issued to Burrows or Saito or in view of U.S. Patent 6,377,530) issued to Burrows further in view of U.S. Patent 6,804,263 issued to Okawa. Neither

of the secondary references, taken singly or in any combination with Saito, render any of the rejected claims as being obvious. For example, the secondary reference Burrows merely provides for a system memory in the form of a hard disk drive (HDD). Thus, Burrow does not overcome the deficiencies of Saito.

Accordingly, Applicants submit that claims 1, 7, 13, 19 and 22 are not anticipated nor rendered obvious by any combination of Saito and/or Burrows and/or Okawa and respectfully requests that the Examiner withdraw the rejection under 35 U.S. C. §102(b) and 35 U.S. C. §103(a).

All dependent claims depend either directly or indirectly from claims 1, 7, 13, 19, 22 and are therefore also submitted to be allowable.

CONCLUSION

Applicants believe that all pending claims are allowable and respectfully request a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,

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