IN THE UNITED STATES DISTRICT COURT FOR THE
WESTERN DISTRICT OF WISCONSIN

NOKIA CORPORATION, Plaintiff, v. APPLE INC., Defendant.	Civil Action No. 10-CV-249 **JURY TRIAL DEMANDED**
APPLE INC., Counterclaim-Plaintiff, v. NOKIA CORPORATION and NOKIA INC., Counterclaim-Defendants.	

DECLARATION OF DR. DAVID T. BLAAUW

I, Dr. David T. Blaauw, hereby declare as follows:

1. I have been retained by counsel for Nokia Corporation and Nokia Inc. (collectively, "Nokia") in support of their representation of Nokia against Apple Inc. in *Nokia Corporation v. Apple Inc.* (10-CV-249).

2. I give this Declaration for use in support of Nokia's Opening Claim Construction Brief regarding U.S. Patent No. 7,760,559 ("the 559 Patent").

3. I am currently a Professor of Electrical Engineering and Computer Science at the University of Michigan. Prior to joining the University of Michigan, I worked for

Motorola, Inc. as an Engineering Manager in the advanced design technology group from 1994 to 2001 and as a Staff Engineer in the semiconductor systems design technology group from 1993 to 1994. Prior to joining Motorola, I worked for IBM Corporation as a Development Staff Member from 1992 to 1993. I received my Bachelor of Science in computer science , with a second major in physics, from Duke University in 1986, my Master of Science in Computer Science from the University of Illinois at Urbana-Champaign in 1989, and my Doctor of Philosophy in Computer Science from the University of Illinois at Urbana-Campaign in 1992.

4. I have experience in the field of integrated circuit design, particularly addressing design issues pertaining to power management, performance, and robustness. My current curriculam vitae is attached to this report as Exhibit A, which includes a list of my research grants, publications, scholarly addresses, and professional activities.

5. I am compensated at a rate of $400 an hour. My opinion is objective, and my compensation is not dependent on the outcome of this litigation.

6. I have reviewed the 559 Patent, its file history, and certain references cited during prosecution.

7. I have been asked to opine as to how one of ordinary skill in the art would understand the meaning of the term “during use” found in the 559 Patent.

8. One of ordinary skill in the art of the subject matter of the 559 Patent would have an M.S. in Electrical Engineering or Computer Science and have at least two years experience in the design of integrated circuits related to power management. I am at least one of ordinary skill in the art.

9. The term “during use” did not have an ordinary and customary meaning to one of ordinary skill in the relevant art as of the priority date of the 559 Patent.

10. “Use” in the context of an integrated circuit is not a binary condition, like “on” and “off” might be for a light switch.

11. An integrated circuit is not generally described as being “in use” or “not in use” in the relevant art.

12. It was known as of the priority date of the 559 Patent that integrated circuits and processors can be configured for various modes, or states, such as “active mode,” “idle mode,” “standby mode,” and “sleep mode.”

13. It would be unclear to one of skill in the art where the line between use and non use of an integrated circuit might be drawn, because the term “use” was not generally recognized as referring to any one particular mode or combination of modes.

14. One skilled in the art at the time of the invention would have been familiar with various techniques for managing power in an integrated circuit.

15. Such techniques generally involved placing all or certain parts of the integrated circuit in a low-power state, or interrupting the power supply to all or certain parts of the integrated circuit, during periods of inactivity.

16. Specific techniques known at the relevant time included “dynamic voltage scaling,” “clock gating,” and “power gating.”

17. Dynamic voltage scaling involves increasing or decreasing the voltage supply to certain components based on the current operating frequency requirements.

18. Clock gating disables the clock to certain components to stop activity and thereby eliminate most of the components’ power consumption.

19. In power gating, the power supply is cut off to components while they are not functionally required.

20. By employing one or more of these and other techniques, an integrated circuit could be configured for a variety of power management modes or states.

21. For example, the Intel "PXA27x" family of processors, which were available at the time of the invention, were configured for at least six processor power modes: (i) Normal mode – wherein power is supplied to all internal power domains including the processor and memory, and all clocks are running; (ii) Idle mode – wherein power is supplied to all internal power domains and most clocks are running, but the processor clock is stopped during periods of inactivity by setting a control register; (iii) Deep-idle mode – another idle mode wherein the CPU PhaseLockedLoop circuit is disabled and instead a more power efficient13MHz oscillator is enabled; (iv) Standby mode – wherein power consumption is reduced, both peripheral and CPU clocks are stopped such that internal activity has stopped, but the state of the memory may be preserved; (v) Sleep mode – wherein power consumption is reduced further, most power supplies including those to the processor and memory can be cut off, most clocks are stopped, and CPU state is lost; and (vi) Deep-sleep mode – another sleep mode that offers the lowest power consumption by further disabling most IO pins of the integrated circuit.

22. The Intel "PXA27x" family of processors did not include a "use" mode.

23. It would be unclear to one of skill in the art which mode or modes would be in effect "during use" of the integrated circuit.

24. One skilled in the art might consider only the normal mode to include "use" of the device because that is the mode in which the entire device – processor, memory, and peripheral components – is fully active.

25. Another skilled in the art might also include one or more of the idle modes as "use" because most of the components including the memory are powered and clocked and the processor continues to monitor one or more internal or external interrupt lines for activity to indicate the need to restore the processor to normal mode.

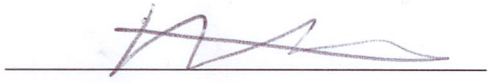
26. A still other person skilled in the art might conclude that the device is still in "use" during the standby mode because the state of the memory can be maintained and thus the integrated circuit can at least be "used" to store data.

27. Further, some skilled in the art might even consider one or more of the sleep modes as "use" because some critical components (e.g., the real time clock (RTC) and the IO pins) are still active and the processor is still monitoring a restricted set of interrupt lines that restore the processor to normal mode; thus, at least some parts of the device are being "used."

28. Reasonable minds would differ, however, on which mode(s) qualify as "use" because the term "during use" did not have a generally accepted meaning in the art.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

Dated: December 17, 2010



Dr. David T. Blaauw