# EXHIBIT A

# CURRICULUM VITAE

# David T. Blaauw

April 2010

## I Personal Data


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|---|---|
| Office Address: | Advanced Computer Architecture Laboratory, 4749 CSE Building<br>The University of Michigan<br>2260 Hayward<br>Ann Arbor, Michigan 48109-2122 |
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## II Employment History

### A. Education

**Doctor of Philosophy** in Computer Science, University of Illinois, Urbana-Champaign, January 1992.
Thesis: "Functional Abstraction in Switch-Level Simulation."
Advisor: Professor Jacob A. Abraham

**Master of Science** in Computer Science, University of Illinois, Urbana-Champaign, May 1989.
Thesis: "Automatic Generation of Behavioral Models."
Advisor: Professor Jacob A. Abraham

**Bachelor of Science** in Physics with a second major in Computer Science, Duke University, May 1986.

### B. Present Position

Professor of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, Michigan.

### C. Employment History

- September 2007 - Present: Professor, Department of Electrical Engineer and Computer Science, University of Michigan, Ann Arbor, Michigan
- August 2001 - September 2007: Associate Professor, Department of Electrical Engineer and Computer Science, University of Michigan, Ann Arbor, Michigan.
- September 1994 - August 2001: Engineering Manager, Advanced Design Technology, Motorola, Inc., Austin, Texas.
- August 1993 - September 1994: Staff engineer, Semiconductor Systems Design Technology Group, Motorola, Inc., Austin, Texas.

- August 1992 - August 1993: Development Staff Member, IBM Corporation, Endicott, New York.

## D. Honors and Awards

- Best Paper Award, "Low Power Circuit Design Based on Heterojunction Tunneling Transistors (HETTs)," ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), August 2009
- 2008 Ted Kennedy Family Team Excellence Award (award shared with Todd Austin, Scott Mahlke, Trevor Mudge, Marios Papaefthymiou). The Ted Kennedy Family Team Excellence Award is an annual award given by the University of Michigan College of Engineering that recognizes the production of an extraordinary and significant piece of work from current or recent collaboration in teaching or research to the College of Engineering.
- 2008 Richard Newton GSRC Industrial Impact Award for "development of the Razor technology" (award shared with Professor Todd Austin). The Richard Newton GSRC Industrial Impact Award is an annual award given by the GSRC DARPA/MARCO center that recognizes research that is "at least five years old and has had a significant industrial impact."
- University of Michigan College of Engineering Research Excellence Award for 2007-2008, January 2008
- Best Paper Nomination, "Energy Efficent Near-threshold Chip Multi-processing," ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), August 2007
- Best Paper Nomination, "Self-timed Regenerators for High-speed and Low-power Interconnect," ACM/IEEE International Symposium on Quality Electronic Design (ISQED), March 2007
- Microprocessor Review Analysts' Choice Award in Innovation for "Introducing Speculation on Correctness as a Method for Allowing Circuit Operation Beyond Worst-Case Design," Microprocessor Review, February 2007
- 2004 IEEE Micro Top Picks special issue on the most industry relevant and significant papers of the year in computer architecture, "Razor: Circuit-Level Correction of Timing Errors for Low-Power Operation"
- University of Michigan Henry Russel Award for "Exceptional Scholarship and Conspicuous Ability as a Teacher," November 2004
- Best Paper Nomination, "Parametric Yield Estimation Considering Leakage Variability," ACM/IEEE Design Automation Conference (DAC), June 2004
- Best Paper Award, "Razor: A Low-Power Pipeline Based on Circuit-Level Timing Speculation," ACM/IEEE International Symposium on Microarchitecture (MICRO), November 2003
- Best Regular Paper Award, "Noise Analysis Methodology for Partially Depleted SOI Circuits," IEEE Custom Integrated Circuits Conference (CICC), September 2003
- IBM Faculty Award, IBM Center for Advanced Studies, June 2003
- Best Paper Award, "Statistical Delay Computation Considering Spatial Correlations," ACM/IEEE Asia-Pacific Design Automation Conference (ASP-DAC), January 2003
- IBM Faculty Award, IBM Center for Advanced Studies, June 2002
- Best Paper Nomination, "Pre-route Noise Estimation in Deep Submicron Integrated Circuits," ACM/IEEE International Symposium on Quality Electronic Design (ISQED), March 2002
- Best Paper Nomination, "Driver Modeling and Alignment for Worst-Case Delay Noise," ACM/IEEE Design Automation Conference (DAC), June 2001

- Best Paper Award, "On-Chip Inductance Modeling and Analysis," ACM/IEEE Design Automation Conference (DAC), June 2000
- Motorola Innovation Award, 1997
- Motorola High Impact Technology Award, 1996

# III Research Experience

## A. Research Interests

My research interests focus on high-performance and low-power VLSI circuits, particularly addressing nano-meter design issues pertaining to power, performance and robustness. My aim is to develop novel circuit design techniques for effective VLSI design in the nano-meter era, in conjunction with efficient and accurate analysis and optimization methods for large, multi-million transistor designs.

## B. Doctoral Students Supervised

| Student | Thesis Title/Topic | Graduation Date |
|---|---|---|
| Aseem Agarwal | Statistical timing analysis for VLSI circuits | Mar 2005 |
| Dongwoo Lee | Analysis and minimization of leakage current | May 2005 |
| Rajeev Rao | Modeling and design of low-power VLSI systems under for multiple sources of uncertainty | Jul 2006 |
| Bo Zhai | Dynamic voltage scaling for embedded processor designs | Mar 2007 |
| Mini Nanua | Leakage and noise analysis in nano-scale technologies | Apr 2007 |
| Sanjay Pant | Power grid analysis and design | Dec 2007 |
| Eric Karl | Reliable computing on unpredictable silicon | Mar 2008 |
| Kaviraj Chopra | Statistical timing analysis including spatial correlations | Apr 2008 |
| Shidhartha Das | Razor: circuit speculation for power and performance efficient design | Oct 2008 |
| Carlos Tokunaga | Circuits and architectures for secure processing | Sep 2008 |
| Ravikishore Gandikota | Crosstalk-Noise analysis for nanometer VLSI circuits | Aug 2009 |
| Brian Cline | Process variation modeling for advance semiconductor circuits | Feb 2010 |
| Prashant Singh | Reliability analysis and wear-out detection | 2010 (expected) |
| Yoonmyung Lee | Ultra Low-Power Memory Design | 2011 (expected) |
| Nurrachman Liu | Automatic tuning of VLSI circuits | 2011 (expected) |
| Cheng Zhou | VLSI wearout modeling | 2011 (expected) |

| Student | Thesis Title/Topic | Graduation Date |
|---|---|---|
| Sudhir Satpathy | Fast and low power inconnect fabrics | 2012 (expected) |
| David Fick | Adaptive Low-power design | 2012 (expected) |
| Zhi Yoong Foo | Low power processor design techniques | 2013 (expected) |
| Gyouho Kim | Ultra-low power visual monitoring | 2014 (expected) |
| Bharan Giridhar | Adaptive Computing | 2014 (expected) |
| YeJoong Kim | Ultra-low voltage circuits | 2014 (expected) |

### C. Masters Students Supervised

| Student | Thesis Title/Topic | Graduation Date |
|---|---|---|
| Bhavana Thudi | Non-iterative switching window computation for delay noise | May 2003 |
| Wesley Kwong | Efficient circuit-level analysis of gate-oxide tunneling current in VLSI designs | May 2003 |
| Toan Pham | Clock skew reduction using Razor flip-flops | Dec 2003 |
| Amit Jain | Delay modeling for non-ramp input transitions | Nov 2004 |
| Amir Borna | Analysis of lithographic variations for chip performance | Aug 2005 |
| Deepesh John | Low power design through typical-case optimization | May 2006 |
| Yueh-Chuan Tzeng | Encryption processor for side channel attack avoidance | May 2006 |
| Meghna Singhal | Low power design using subthreshold operation | May 2006 |
| Sudherssen Kalaiselvan | Razor-3: A circuit speculation and SEU tolerant circuit technique | May 2007 |
| Mao-Ter Chen | Low power sensor node design | Dec 2008 |
| Jeffrey Yeh | Chip design for the developing world | 2009 (expected) |
| Jou-ching (George) Sung | Low power ADC design | August 2009 |
| Junsun Park | Intra-cellular chip design | May 2010 |

### D. Research Grants

- Intel Corporation, “A Confidence Driven Model for Predictable Computing in Future Technologies,” $169,000 total with $56,333 to Blaauw, PI: Prof. Zhengya Zhang, Co-PIs: Prof. David Blaauw, Prof. Peter Chen, and Prof. Dennis Sylvester, University of Michigan, 03/2010 - 02/2011
- QUALCOMM, “Adaptive Design Solutions for VLSI Circuits,” $50,000, gift, 09/01/09

- MARCO/DARPA - Multi-Scale Systems Center (MuSyC), "Subthreshold Sensor Node Design," $394,100 total, PI: Prof. David Blaauw, 11/2009 - 10/2012
- National Science Foundation (NSF), "Reclaiming Moore's Law through Ultra Energy Efficient Computing," $2,778,507 total with $643,700 to Blaauw, PI: Prof. David Blaauw, Co-PIs: Prof. Trevor Mudge, Prof. Dennis Sylvester, University of Michigan, Prof. Chaitali Chakrabarti, Arizona State University, Prof. David Money Harris, Harvey Mudd University, 09/2009 - 08/2014
- National Science Foundation (NSF), "Probabilistic Wearout in Nanoscale," $300,000 with $150,000 to Blaauw, PI: Dennis Sylvester, Co-PI: David Blaauw, 08/2008 - 07/2011
- IBM Corporation/Defense Advanced Research Projects Agency (DARPA), "Strained Si/SiGe/Ge HEterojunction Tunneling Transistor (HETT) e with Steep Subthreshold Slope for Extremely Low Power Electronics," $17,971,252 with $600,000 to Blaauw, PI: Steve Koester, Co-PI: David Blaauw, 01/2008 - 12/2009
- BAE Systems/United States Army, "Center for Objective Microelectronics and Biomimetic Adaptive Technology (COM-BAT)," $8,962,200 with $700,000 to Blaauw, PI:Kamal Sarabandi, Co-PI: David Blaauw, 5/2008 - 5/2013
- Intel Corporation, "Adaptive Digital Design in the Nanometer Regime," $100,000, gift, 3/2008 - 3/2010
- Sun Microsystems, "Robust Low Voltage SRAM Design," $150,000, gift, 9/2007 - 9/2010
- Intel Corporation, "Circuit and Microarchitectural Methods for Subthreshold Design," $40,000, gift, 7/2007
- MARCO/DARPA - Gigascale Systems Research Center (GSRC), "Elastic: An Adaptive Self-Healing Architecture for Unpredictable Silicon," $600,000 total, PI: David Blaauw, 9/2006 - 9/2009
- Semiconductor Research Corporation (SRC), "A Design Optimization Framework for Process Variation Tolerance," $390,000 total with $195,000 to Blaauw, PI: Dennis Sylvester, Co-PI: David Blaauw, University of Michigan, 9/2006 - 8/2009
- Intel Corporation, "Circuit and Microarchitectural Methods for Subthreshold Design" $40,000, gift, 7/2006
- Semiconductor Research Corporation (SRC), "CAD Solutions for Parametric Yield Optimization," $321,000 total with $160,000 to Blaauw, PI Dennis Sylvester, Co-PI: David Blaauw, University of Michigan, 9/2005 - 7/2008
- Intel Corporation, "Circuit and Microarchitectural Methods for Subthreshold Design" $40,000, gift, 7/2005
- NSF Engineering Research Center (ERC) for Wireless Integrated Micro Systems (WIMS), "Subthreshold Processor Design," PI: Kenneth Wise, University of Michigan, $60,000 to Blaauw, 5/2005 - 5/2010
- ARM, Ltd, "Low Power Computing for Embedded Applications," $5,000,000 total, with approx. $1,600,000 to Blaauw, PI: Trevor Mudge, University of Michigan, Co-PIs: David Blaauw, Scott Mahlke, University of Michigan, 5/2005 - 5/2010
- Semiconductor Research Corporation (SRC), "Optimization of Lithographic Induced Variability for Improved Circuit Performance," $161,029, PI: David Blaauw, 9/2004 - 8/2007
- Intel Corporation, "Power Grid Integrity Analysis," $50,000, gift, 7/2004
- Photronics, Inc. $75,000, gift, 6/2004 - 5/2005

- ARM, Ltd, “Low Power Computing for Embedded Applications,” $240,000 total with $60,000 to Blaauw, PI: Trevor Mudge, University of Michigan, Co-PIs: David Blaauw, Scott Mahlke and Todd Austin, University of Michigan, 5/2004 - 5/2005
- National Science Foundation (NSF), Information Technology Research (ITR), “Collaborative Research ITR: Mobile Supercomputing,” $1,900,000 total with $320,603 to Blaauw, PI: Prof. Trevor Mudge, Co-PIs: Prof. David Blaauw, Prof. Todd Austin, Prof. Scott Mahlke, University of Michigan, Prof. Wayne Wolf, Princeton University, Prof. Chaitali Chakrabarti, Arizona State University, 11/2003 - 11/2007
- Intel Corporation, “VLSI Design Curriculum,” $247,292 total with $61,823 to Blaauw, PI: Richard Brown, Co-PIs: Prof. David Blaauw, Prof. Michael Flynn, and Prof. Dennis Sylvester, University of Michigan, 10/2003 - 10/2004
- MARCO/DARPA - Gigascale Systems Research Center (GSRC), “Power Aware Systems,” $600,000 total, PI: David Blaauw, 9/2003 - 9/2006
- IBM Corporation, Center for Advanced Studies, “Static Performance Analysis under Process and Environment Variations,” $40,000, Faculty Award, 9/2003
- Intel Corporation, “Power Grid Integrity Analysis,” $50,000, gift, 7/2003
- Semiconductor Research Corporation (SRC), “Analysis and Reduction of Simultaneous Gate-Oxide Tunneling and Subthreshold Leakage Current,” $360,000 total with $160,000 to Blaauw, PI: David Blaauw, Co-PI: Dennis Sylvester, University of Michigan, 7/2003 - 7/2006
- National Science Foundation (NSF), “Performance Analysis and Optimization for Nanometer Design,” $375,000, PI: David Blaauw, 6/2003 - 6/2006
- ARM, Ltd, “Low Power Computing for Embedded Applications,” $240,000 total with $60,000 to Blaauw, PI: Trevor Mudge, University of Michigan, Co-PIs: David Blaauw and Scott Mahlke, University of Michigan, 5/2003 - 5/2004
- IBM Corporation, Center for Advanced Studies, “Leakage Characterization and Analysis,” $40,000, Faculty Award, 9/2002
- National Science Foundation (NSF), Information Technology Research (ITR), “Methodologies for Robust Design of Information Systems under Multiple Sources of Uncertainty”, $1,800,00 total with $450,000 to Blaauw, PI: David Blaauw, Co-PIs: Prof. Dennis Sylvester, University of Michigan, Prof. Sachin Sapatnekar, University of Minnesota, Prof. Sarma Vrudhula, University of Arizona, 8/2002 - 8/2006
- Intel Corporation, “Power Grid Integrity Analysis,” $50,000, gift, 7/2002
- MARCO/DARPA - Giga-Scale Research Center (GSRC), “Power Management for Nanometer design,” $197,000, PI: David Blaauw, 10/2001 - 8/2003
- Semiconductor Research Corporation (SRC), “Variability in Chip-Level Performance and Signal Integrity Verification,” $257,000, PI: David Blaauw, 10/2001 - 10/2004

## IV Teaching Experience

### A. Undergraduate Courses Taught

| Course Number | Title | Semester | Class Size | Rating (out of 5) |
|---|---|---|---|---|
| UM EECS 270 | Introduction to Logic Design | Fall 2003 | 87 | 4.77 |
| | | Fall 2002 | 109 | 4.77 |
| UM EECS 427 | VLSI Design I | Fall 2006 | 31 | 4.89 |
| | | Fall 2008 | 28 | 4.56 |

### B. Graduate Courses Taught

| Course Number | Title | Semester | Class Size | Rating (out of 5) |
|---|---|---|---|---|
| UM EECS 598 | Advanced VLSI Design | Fall 2005 | 12 | 4.25 |
| UM EECS 598 | Issues in High-Performance Deep-Sub-micron Design | Fall 2001 | 11 | 4.75 |
| UM EECS 627 | Advanced VLSI Design | Winter 2009 | 23 | 4.75 |
| | | Winter 2007 | 20 | 4.79 |
| | | Winter 2006 | 22 | 4.55 |
| | | Winter 2005 | 20 | 4.79 |
| | | Winter 2004 | 35 | 4.59 |
| | | Winter 2003 | 36 | 4.61 |
| | | Winter 2002 | 40 | 4.31 |

# V Publications

## A. Books

1. Ashish Srivastava, Dennis Sylvester and David Blaauw, *Statistical Analysis and Optimization for VLSI: Timing and Power*, Kluwer Academic Publishers, 2005

## B. Book Chapters

1. Shidhartha Das, David Roberts, David Blaauw, David Bull, Trevor Mudge, "Architectural Techniques for Adaptive Computing", Chapter in *Adaptive Techniques for Dynamic Processor Optimization: Theory and Practice*, Alice Wang and Sam Naffziger, editors, Springer Publishing Company, 2008
2. David Blaauw, Sanjay Pant, Rajat Chaudhry and Rajendran Panda, "Design and Analysis of Power Supply Networks," Chapter in *Electronic Design Automation for Integrated Circuits Handbook*, Louise Sheffer, Luciano Lavagno and Grant Martin, editors, CRC Press, 2005
3. Sarvesh Kulkarni, Ashish Srivastava, Dennis Sylvester, David Blaauw, "Power Optimization Techniques using Multiple Supply Voltages," Chapter in *Closing the Power Gap between ASIC and Custom*, David Chinnery and Kurt Keutzer, editors, Kluwer Academic Publishers, 2005
4. David Blaauw, Abhijit Dharchoudhury, Rajendran Panda, "Design and Analysis of Power Distribution Networks for Processor Design," Chapter in IEEE *Design of High Performance Microprocessors Circuits*, Anantha Chandrakasan, William Bowhill, and Frank Fox, editors, IEEE Press, 2000
5. Abhijit Dharchoudhury, Shantanu Ganguly, David Blaauw, "Timing and Signal Integrity Analysis," Chapter in *Handbook for VLSI Design*, Wai Kai Chen, editor, IEEE Press, 2000
6. Dongwoo Lee, Bo Zhai, David Blaauw, Dennis Sylvester, "Static Leakage Reduction through Simultaneous $V_t/T_{ox}$ and State Assignment," Chapter in *Ultra Low-Power Electronics and Design*, Enrico Macii, editor, Kluwer Academic Publishers, 2004

## C. Invited Articles

1. Ronald G. Dreslinski, Michael Wieckowski, David Blaauw, Dennis Sylvester, Trevor Mudge, "Near-Threshold Computing: Reclaiming Moore's Law Through Energy Efficient Integrated Circuits," Proceedings of the IEEE, Special Issue on Ultra-Low Power Circuit Technology, Vol. 98, No. 2, February 2010, pg. 253 - 266
2. David Blaauw, Shidhartha Das, "CPU, Heal Thyself," IEEE Spectrum, August 2009
3. Shidhartha Das, David Blaauw, David Bull, Krisztian Flautner, Rob Aitken, "Addressing Design Margins through Error-tolerant Circuits," ACM/IEEE Design Automation Conference (DAC), July 2009
4. Shidhartha Das, David Blaauw, "Adaptive Design for Nanometer Technology," IEEE International Symposium on Circuits and Systems (ISCAS), May 2009
5. Dennis Sylvester, Scott Hanson, Mingoo Seok, Yu-Shiang Lin, David Blaauw, "Designing Robust Ultra-Low Power Circuits," International Electron Devices Meeting (IEDM), December 2008
6. David Blaauw, Kaviraj Chopra, Ashish Srivastava, Lou Sheffer, "Statistical Timing Analysis: Basic Principles to State-of-the-Art," *Transactions on Computer-Aided Design of Integrated Circuits and Systems* (*T-CAD*), invited review article, Vol. 27, No. 4, April 2008, pg. 589-607
7. Scott Hanson, Bo Zhai, David Blaauw, Dennis Sylvester, "Energy-Optimal Circuit Design," IEEE International SoC Design Conference, November 2007

8. Sanjay Pant, Eli Chiprout, David Blaauw, “Power Grid Physics and Implications for CAD,” *IEEE Design and Test of Computers (D & T)*, Vol. 24, No. 3, May-June 2007, pg. 246-254
9. Dennis Sylvester, Scott Hanson, Bo Zhai, and David Blaauw, “Design strategies for ultra-low voltage circuits,” IEEE International SoC Design Conference, September 2006
10. Scott Hanson, Bo Zhai, David Blaauw, Dennis Sylvester, Andres Bryant, Xinlin Wang, “Energy Optimality and Variability in Subthreshold Design,” ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), September 2006
11. Shidartha Das, David Roberts, Seokwoo Lee, Sanjay Pant, David Blaauw, Todd Austin, Trevor Mudge, Krisztián Flautner, “A Self-Tuning Dynamic Voltage Scaled Processor Using Delay-Error Detection and Correction,” IEEE International Conference on Integrated Circuit Design & Technology (ICICDT), May 2006
12. David Blaauw and Bo Zhai, “Energy Efficient Design for Subthreshold Supply Voltage Operation,” IEEE International Symposium on Circuits and Systems (ISCAS), May 2006
13. Rajeev R. Rao, David Blaauw, Dennis Sylvester, Anirudh Devgan, “Modeling and Analysis of Parametric Yield Under Power and Performance Constraints,” *IEEE Design and Test of Computers (D&T)*, Vol. 22, No. 4, July-August 2005, pg. 376-385
14. Todd Austin, Valeria Bertacco, David Blaauw, Trevor Mudge, “Opportunities and Challenges for Better Than Worst-Case Design,” ACM/IEEE Asia-Pacific Design Automation Conference (ASP-DAC), January 2005, pg. I-2
15. Bo Zhai, David Blaauw, Dennis Sylvester, Krisztián Flautner, “Extended Dynamic Voltage Scaling for Low Power Design,” IEEE International SOC Conference, September 2004, pg. 389-394
16. Todd Austin, David Blaauw, Trevor Mudge, Krisztián Flautner, “Making Typical Silicon Matter with Razor” *IEEE Computer*, March 2004, pg. 57-65
17. David Blaauw, Kaushik Gala, “Inductance: Implications and Solutions for High-Speed Digital Circuits - Inductance Extraction and Modeling,” IEEE International Solid-State Circuits Conference (ISSCC), February 2002, pg. 548-553
18. David Blaauw, “Signal Integrity Issues in High Performance Design,” IEEE International Workshop on Power and Timing Modeling, Optimization and Simulation (Patmos), September 2001, pg. 5.1.1-5.1.4
19. Kaushik Gala, David Blaauw, Junfeng Wang, Vladimir Zolotov, Min Zhao, “Inductance 101: Analysis and Design Issues,” ACM/IEEE Design Automation Conference (DAC), June 2001, pg. 329-334
20. David Blaauw, Kaushik Gala, Vladimir Zolotov, Rajendran Panda, Junfeng Wang, “On-Chip Inductance Modeling,” ACM/IEEE Great Lake Symposium on VLSI Design (GLSVLSI), March 2000, pg. 75-80
21. David Blaauw, “Power Management Issues in High Performance Processor Design,” IEEE Alessandro Volta Workshop on Low-Power Design (VOLTA), March 1999, pg. 2
22. David Blaauw, Abhijit Dharchoudhury, Rajendran Panda, Supamas Sirichotiyakul, Chanhee Oh, Tim Edwards, “Industrial Perspectives on Emerging CAD Tools for Low Power Processor Design,” ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), August 1998, pg. 143-148
23. Abhijit Dharchoudhury, Rajendran Panda, David Blaauw, Ravi Vaidyanathan, Bogdan Tutuianu, David Bearden, “Methodology for the Design and Analysis of Power Distribution Networks on the PowerPC Microprocessor,” ACM/IEEE Design Automation Conference (DAC), June 1998, pg. 738-743

## D. Journals

1. Scott Hanson, ZhiYoong Foo, David Blaauw, Dennis Sylvester, "A 0.5V Sub-Microwatt CMOS Image Sensor with Pulse-Width Modulation Read-Out," *IEEE Journal of Solid-State Circuits (JSSC) to the Special Issue on VLSI Circuits*, Vol. 45, No. 4, April 2010, pgs. 759 - 767
2. Shidhartha Das, Carlos Tokunaga, Sanjay Pant, Wei-Hsiang Ma, Sudherssen Kalaiselvan, Kevin Lai, David Bull, David Blaauw, "Razor II: In Situ Error Detection and Correction for PVT and SER Tolerance," *IEEE Journal of Solid-State Circuits (JSSC)*, ***Invited Paper*** *to the Special Issue on ISSCC,* Vol. 44, No. 1, January 2009, pgs. 32 - 48
3. Ravikishore Gandikota, Kaviraj Chopra, David Blaauw, Dennis Sylvester, "Victim-Alignment in Crosstalk-Aware Timing Analysis," *Transactions on Computer-Aided Design of Integrated Circuits and Systems* (*T-CAD*), Vol. 29, No. 2, pgs. 261 - 274
4. Carlos Tokunaga and David Blaauw, "Securing encryption systems with a switched capacitor current equalizer," *IEEE Journal of Solid-State Circuits (JSSC)*, ***Invited Paper*** *to the Special Issue on ISSCC*, Vol. 45, No. 1, January 2010, pgs. 23 - 31
5. Rajeev Rao, Vivek Joshi, David Blaauw, Dennis Sylvester, "Circuit Optimization Techniques to Mitigate the Effects of Soft Errors in Combinational Logic," *ACM Transactions on Design Automation of Electronic Systems* (*TODAES*), Vol. 15, Issue 1, December 2009, Article 5
6. Bo Zhai, Sanjay Pant, Leyla Nazhandali, Scott Hanson, Javin Olson, Ann Reeves, Michael Minuth, Ryan Helfand, Todd Austin, Dennis Sylvester, David Blaauw, "Energy Efficient Subthreshold Processor Design," *IEEE Transactions on Very Large Scale Integration Systems* (*T-VLSI*), Vol. 17, No. 8, August 2009, pgs. 1127 - 1137
7. Yu-Shiang Lin, Dennis Sylvester, David Blaauw, "Alignment Independent Chip-to-Chip Communication for Sensor Applications using Passive Capacitive Signaling," *IEEE Journal of Solid-State Circuits (JSSC),* ***Invited Paper*** *to the Special Issue on VLSI Circuits*, Vol. 44, No. 4, April 2009, pgs. 1156 - 1166
8. Scott Hanson, Mingoo Seok, Yu-Shiang Lin, Zhiyoong Foo, Daeyon Kim, Yoonmyung Lee, Nurrachman Liu, Dennis Sylvester, David Blaauw, "A Low-Voltage Processor for Sensing Applications with Picowatt Standby Mode," *IEEE Journal of Solid-State Circuits (JSSC),* ***Invited Paper*** *to the Special Issue on VLSI Circuits*, Vol. 44, No. 4, April 2009, pgs. 1145 - 1155
9. Fabio Albano, Yu-Shiang Lin, David Blaauw, Dennis Sylvester, Kensall Wise, Ann Marie Sastry, "A fully integrated microbattery for an implantable microelectromechanical system," *Journal of Power Sources*, August 2008
10. Bo Zhai, Scott Hanson, David Blaauw, Dennis Sylvester, "A Variation-Tolerant Sub-200mV 6-T Subthreshold SRAM," *IEEE Journal of Solid-State Circuits (JSSC)*, ***Invited Paper*** *to the Special Issue on the 2008 Compound Semi-Conductor Integrated Circuit Symposium (CSICS'08),* Vol. 43, No. 10, October 2008, pgs. 2338 - 2348
11. Scott Hanson, Bo Zhai, Mingoo Seok, Brian Cline, Kevin Zhou, Meghna Singhal, Michael Minuth, Javin Olson, Leyla Nazhandali, Todd Austin, Dennis Sylvester, David Blaauw, "Exploring Variability and Performance in a Sub-200 mV Processor", *IEEE Journal of Solid-State Circuits (JSSC)*, ***Invited Paper*** *to the Special Issue on VLSI Circuits*, Vol. 43, No. 4, April 2008, pgs. 881 - 891
12. Prashant Singh, Jae-Sun Seo, David Blaauw, Dennis Sylvester, "Self-timed Regenerators for High-speed and Low-power On-chip Global Interconnect," *IEEE Transactions on Very Large Scale Integration Systems* (*T-VLSI*), Vol. 16, No. 6, June 2008, pgs. 673-677

13. Sarvesh Kulkarni, Dennis Sylvester, David Blaauw, "Design-Time Optimization of Post-Silicon Tuned Circuits using Adaptive Body Bias," *Transactions on Computer-Aided Design of Integrated Circuits and Systems* (*T-CAD*), Vol. 27, No. 3, March 2008, pgs. 481-494

14. Eric Karl, David Blaauw, Dennis Sylvester, Trevor Mudge, "Multi-Mechanism Reliability Modeling and Management in Dynamic Systems," *IEEE Transactions on Very Large Scale Integration Systems* (*T-VLSI*), Vol. 16, No. 4, April 2008, pgs. 476-487

15. Carlos Tokunaga, David Blaauw, Trevor Mudge, "True Random Number Generator with a Metastability-based Quality Control," *IEEE Journal of Solid-State Circuits (JSSC)*, ***Invited Paper*** *to the Special Issue on the 2007 IEEE International Solid-State Circuits Conference (ISSCC)*, Vol. 43, No. 1, January 2008, pgs. 78 - 85

16. Ashish Srivastava, Kaviraj Chopra, Saumil Shah, Dennis Sylvester, David Blaauw, "A Novel Approach to Perform Gate-level Yield Analysis and Optimization Considering Correlated Variations in Power and Performance,"*Transactions on Computer-Aided Design of Integrated Circuits and Systems* (*T-CAD*), Vol. 27, No. 2, February 2008

17. Scott Hanson, Mingoo Seok, Dennis Sylvester, David Blaauw, "Nanometer Device Scaling in Subthreshold Logic and SRAM," *Special Issue of IEEE Transactions on Electron Devices (T-ED),* Vol. 55, Issue 1, January 2008, pgs. 175 - 185

18. Rajeev Rao, Kaviraj Chopra, David Blaauw, Dennis Sylvester, "Computing the Soft Error Rate of a Combinational Logic Circuit Using Parameterized Descriptors," *IEEE Transactions on Very Large Scale Integration Systems* (*T-VLSI*), Vol. 26, Issue 3, March 2007, pgs. 468 - 479

19. Dennis Sylvester, David Blaauw, Eric Karl, "ElastIC: An Adaptive Self-Healing Architecture for Unpredictable Silicon," *IEEE Design and Test of Computers* (*D&T*), Vol. 23, No. 6, November 2006, pg. 484 - 490

20. Dongwoo Lee, David Blaauw, Dennis Sylvester, "Runtime Leakage Minimization through Probability-Aware Optimization," *IEEE Transactions on Very Large Scale Integration Systems* (*T-VLSI*), Vol 14, No. 10, October 2006, 1075-1088

21. Rajeev Rao, Anirudh Devgan, David Blaauw, Dennis Sylvester, "Analytical Yield Prediction Considering Leakage/Performance Correlation," *Transactions on Computer-Aided Design of Integrated Circuits and Systems* (*T-CAD*), Vol 25, Issue 9, September 2006, pg. 1685-1695

22. Scott Hanson, Bo Zhai, Kerry Bernstein, David Blaauw, Andres Bryant, Leland Chang, Koushik Das, Wilfried Haensch, Edward Nowak, Dennis Sylvester, "Ultra-Low Voltage Minimum Energy CMOS" IBM Journal of Research and Development, Vol 50, No. 4/5, July/September 2006, pg. 469-490

23. Kanak Agarwal, Mridul Agarwal, Dennis Sylvester, David Blaauw, "Statistical Interconnect Metrics for Physical-Design Optimization," *Transactions on Computer-Aided Design of Integrated Circuits and Systems* (*T-CAD*), Vol 25, Issue 7, July 2006, pg. 1273-1288

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4. David Blaauw, James Kitchener, Braden Phillips, “Optimizing addition for sub-threshold logic,” Forty-Second Asilomar Conference on Signals, Systems and Computers, October 2008
5. Jae-Sun Seo, Igor Markov, Dennis Sylvester, David Blaauw, “On the Decreasing Significance of Large Standard Cells in Technology Mapping,” International Workshop on Logic & Synthesis (IWLS), June 2008
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15. Mini Nanua and David Blaauw, “Receiver Modeling for Static Functional Crosstalk Analysis,” IEEE International Workshop on Power and Timing Modeling, Optimization and Simulation (Patmos), September 2006
16. Sanjay Pant, David Blaauw, “Timing-aware Decoupling Capacitance Allocation in Power Distribution Networks,” in ACM/IEEE International Workshop on Timing in Synthesis and Specification (TAU), February 2006
17. Kavi Chopra, Bo Zhai, David Blaauw, Dennis Sylvester “A New Statistical Max Operation for Propagating Skewness in Statistical Timing Analysis”, ACM/IEEE International Workshop on Timing in Synthesis and Specification (TAU), February 2006
18. Kavi Chopra, Chandramouli Kashyap, Haihua Su, David Blaauw “Current Source Driver Model Synthesis and Worst-case Alignment for Accurate Timing and Noise Analysis”, ACM/IEEE International Workshop on Timing in Synthesis and Specification (TAU), February 2006

19. Smitha Shyam, Sujay Phadke, Benjamin Lui, Hitesh Gupta, Valeria Bertacco, David Blaauw, "VOLTaiRE: Low-cost Fault Detection Solutions for VLIW Microprocessors," Workshop on Introspective Architecture (WISA), February 2006.
20. Amir Borna, Christopher Progler, David Blaauw, "Correlation Analysis of CD-Variation and Circuit Performance Under Multiple Sources of Variability," SPIE Design and Process Integration for Microelectronic Manufacturing II, Lars W. Liebmann, May 2005
21. Aseem Agarwal, Kaviraj Chopra, Vladimir Zolotov, David Blaauw, "Statistical Timing Based Optimization Using Gate Sizing," ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), February 2005
22. Amit Jain, David Blaauw, Vladimir Zolotov, "Accurate Gate Delay Model for Arbitrary Waveform Shapes," ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), February 2005
23. Christopher Progler, Amir Borna, David Blaauw, Pierre Sixt, "Impact of lithography variability on statistical timing behavior," SPIE Design and Process Integration for Microelectronic Manufacturing II, Lars W. Liebmann, Ed., Vol. 5379, May 2004, pg. 101-110
24. Amit Jain, David Blaauw, "Modeling Flip-Flop Delay Dependencies in Timing Analysis," ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), February 2004
25. Aseem Agarwal, David Blaauw, Vladimir Zolotov, Sarma Vrudhula, "Statistical Timing Analysis Using Bounds and Selective Enumeration," ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), December 2002, pg. 29-36
26. Aseem Agarwal, David Blaauw, Savithri Sundareswaran, Vladimir Zolotov, Min Zhou, Kaushik Gala, Rajendran Panda, "Path-Based Statistical Timing Analysis Considering Inter- and Intra-Die Correlations," ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), December 2002, pg. 16-21
27. Himanshu Kaul, Dennis Sylvester, David Blaauw, "Active Shielding of RLC Global Interconnects," ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), December 2002, pg. 98-104
28. Kanak Agarwal, Dennis Sylvester, David Blaauw, "A Library Compatible Driving Point Model for On-Chip RLC Interconnects," ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), December 2002, pg. 63-69
29. Bhavana Thudi, David Blaauw, "Efficient Switching Window Computation For Cross-Talk Noise," ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), December 2002, pg. 84-91
30. Fadi Aloul, Soha Hassoun, Karem Sakallah, David Blaauw, "Robust SAT-Based Search Algorithm for Leakage Power Reduction," IEEE International Workshop-Power And Timing Modeling, Optimization and Simulation (Patmos), September 2002, pg. 167-177
31. Murat Becer, David Blaauw, Ibrahim Hajj, Rajendran Panda, "Early Probabilistic Noise Estimation for Capacitively Coupled Interconnects," ACM/IEEE International Workshop on System-Level Interconnect Prediction (SLIP), April 2002, pg. 77-83
32. David Blaauw, "Signal Integrity Issues in High Performance Design," IEEE International Workshop - Power and Timing Modeling, Optimization and Simulation (Patmos), September 2001, pg. 5.1.1-5.1.4
33. Vladimir Zolotov, David Blaauw, Rajendran Panda, Chanhee Oh, Savithri Sundareswaran, "Slope Propagation in Static Timing Analysis," ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), December 2000, pg. 91-96
34. Supamas Sirichotiyakul, David Blaauw, Chanhee Oh, Rafi Levy, Vladimir Zolotov, "Driver Modeling and Alignment for Worst-Case Delay Noise," ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), December 2000, pg. 1-7

35. David Blaauw, Tim Edwards, “Generating False Path Free Timing Graphs Using Node Splitting,” ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), March 1999, pg. 112-117
36. David Blaauw, “Power Management Issues in High Performance Processor Design,” IEEE Alessandro Volta Workshop on Low-Power Design (VOLTA), March 1999, pg. 2
37. Daksh Lenther, Satya Pullela, David Blaauw, Shantanu Ganguly, “Hierarchical Clock-network Optimization,” ACM Physical Design Workshop, April 1996, pg. 49-54
38. John Willis, Rob Newshutz, Lance Thompson, Jeff Graves, Tom Dillinger, Jeff Snyder, Nimish Radia, Joe Skovira, David Blaauw, Sidhartha Mohanty, Zhiyuan Li, Sandra Samelson, Matt Lin, “MinSim: Optimized, Compiled VHDL Simulation Using Networked & Parallel Computers,” IEEE VHDL International User Forum, October 1993, pg. 137-144

## G. Patents Issued

1. “Error Detection and Recovery Within Processing Statges of an Integrated Circuit,” Patent Number 7,650,551, issued on January 19, 2010
2. “Data Processor Memory Circuit,” Patent Number 7,533, 226, issued on May 12, 2009
3. “Systematic and Random Error Detection and Recovery Within Processing Stages of An Integrated Circuit,” Patent Number 7,337,356, issued on February 26, 2008
4. “Error Recovery Within Processing Stages of an Integrated Circuit,” Patent Number 7,320,091, issued on January 15, 2008
5. “Data Retention Latch Provision Within Integrated Circuits,” Patent Number 7,310,755, issued on December 18, 2007
6. “Error detection and recovery within processing stages of an integrated circuit,” Patent Number 7,278,080, issued on October 2, 2007
7. “Address Decoding,” Patent Number 7,263,015, issued on August 28, 2007
8. “Systematic and random error detection and recovery within processing stages of an integrated circuit,” Patent Number 7,162,661, issued on January 9, 2007
9. “Methods for analyzing integrated circuits and apparatus therefor,” Patent Number 7,149,674, issued on December 12, 2006
10. “Noise analysis for an integrated circuit model,” Patent Number 7,093,223, issued on August 15, 2006
11. “Memory System having Fast and Slow Data Reading Mechanisms,” Patent Number 7,072,229, issued on July 4, 2006
12. “Data Processor Memory Circuit,” Patent Number 7,055,007, issued on May 30, 2006
13. “Memory System Having Fast and Slow Data Reading Mechanisms,” Patent Number 6,944,067, issued on September 13, 2005
14. “Actively-Shielded Signal Wires,” Patent Number 6,919619, issued on July 19, 2005
15. “Method and Apparatus for Controlling Current Demand in an Integrated Circuit”, Patent Number 6,819,538, issued on November 16, 2004
16. “Cross Coupling Delay Characterization for Integrated Circuits,” Patent Number 6,799,153, issued on September 28, 2004
17. “Iterative, Noise-Sensitive Method of Routing Semiconductor Nets,” Patent Number 6,480,998, issued on November 12, 2002

18. “Waveform Manipulation in Time Warp Simulation,” Patent Number 6,195,628, issued on February 27, 2001
19. “Optimizing Combinational Circuit Layout through Iterative Restructuring,” Patent Number 6,074,429, issued on June 13, 2000
20. “In-Transit Message Detection for Global Virtual Time Calculation in Parallel Time Warp Simulation,” Patent Number 5,956,261, issued on September 21, 1999
21. “Method for Optimizing Element Sizes in a Semiconductor Device,” Patent Number 5,903,471, issued on May 11, 1999
22. “Updating Hierarchical DAG Representations through a Bottom up Method,” Patent Number 5,790,416, issued on August 4, 1998
23. “Complementary Network Reduction for Load Modeling,” Patent Number 5,790,415, issued on August 4, 1998
24. “Simulation Corrected Sensitivity,” Patent Number 5,787,008, issued on July 28, 1998
25. “Accurate Delay Prediction Based on Multi-Model Analysis,” Patent Number 5,751,593, issued on May 12, 1998
26. “Apparatus and Method for the Automatic Determination of a Standard Library Height within an Integrated Circuit Design,” Patent Number 5,737,236, issued April 7, 1998
27. “Integrated Circuit Design and Manufacturing Method and an Apparatus for Designing an Integrated Circuit in Accordance with the Method,” Patent Number 5,689,432, issued on November 18, 1997
28. “Method and Apparatus for Designing an Integrated Circuit,” Patent Number 5,666,288, issued on September 9, 1997
29. “Logic Gate Size Optimization Process for an Integrated Circuit Whereby Circuit Speed is Improved While Circuit Areas is Optimized,” Patent Number 5,619,418, issued on April 8, 1997
30. “Message Sequence Number Control in a Virtual Time System,” Patent Number 5,617,561, issued on April 1, 1997

# VI Scholarly Addresses

## A. Conference Keynote Addresses and Invited Presentations

1. Invited presentation, “Adaptive Sensin and Design for Reliability,” IEEE International Reliability Physics Symposium, May 2009
2. Invited presentation, “Architectural Techniques for Self-Adaptive Computing,” IEEE International Solid-State Circuits Conference (ISSCC), February 2007
3. Invited presentation, “Energy Optimality and Variability in Subthreshold Design,” ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), September 2006
4. Invited presentation, “Energy Efficient Design for Subthreshold Supply Voltage Operation,” IEEE International Symposium on Circuits and Systems (ISCAS), May 2006
5. Invited presentation, “Extended Dynamic Voltage Scaling for Low Power Design,” IEEE International SOC Conference, September 2004
6. Invited presentation, “Signal Integrity Issues in High Performance Design,” IEEE International Workshop-Power And Timing Modeling, Optimization and Simulation (Patmos), Switzerland, September 2001

7. Invited presentation, “Inductance 101: Analysis and Design,” ACM/IEEE Design Automation Conference, June 2001
8. Invited presentation, “Inductance Extraction and Modeling,” ACM/IEEE Great Lakes Symposium on VLSI Design (GLSVLSI), March 2000
9. Keynote address, “Power Management Issues in High Performance Processor Design,” IEEE Alessandro Volta Workshop on Low-Power Design (VOLTA), Italy, March 1999
10. Keynote address, “Industrial Perspectives on Emerging CAD Tools for Low Power Processor Design,” ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), August 1998

## B. Conference Tutorials

1. “Managing Variations Through Adaptive Design Techniques,” half-day tutorial, IEEE International Solid-State Circuits Conference (ISSCC), February 2009
2. “Circuit and CAD Techniques for Low Power Design,” full day tutorial with co-presenter Anantha Chandrakasan, ACM/IEEE Design Automation Conference (DAC), June 2007
3. “Future Trends and Issues in DVS,” full day tutorial with co-presenters Barry Pangrle, David Flynn, David Tamura, ACM/IEEE Design Automation Conference (DAC), June 2005
4. “Leakage Issues in IC Design: Trends, Estimation, Avoidance,” embedded tutorial with co-presenter Anirudh Devgan, ACM/IEEE Asia-Pacific Design Automation Conference (ASP-DAC), January 2005
5. “Low Power Robust Computing,” full day tutorial with co-presenters Todd Austin, Krisztián Flautner, Nam Sung Kim, Trevor Mudge, Dennis Sylvester, ACM/IEEE International Symposium on Microarchitecture (MICRO), November 2004
6. “Standby Leakage Analysis and Optimization Methods for VLSI Design,” full day tutorial with co-presenters Anirudh Devgan, Siva Narendra, Farid Najm, ACM/IEEE International Conference on Computer Aided Design (ICCAD), November 2003
7. “Design for Manufacturing in the Sub-100nm Era,” full day tutorial with co-presenters Louis Scheffer, Sani Nassif, Andrzej Strojwas, ACM/IEEE Design Automation Conference (DAC), June 2003
8. “Inductance Extraction and Modeling,” half-day tutorial with co-presenters Shannon Morton, Phillip Restle, Claude Gauthier, IEEE International Solid-State Circuits Conference (ISSCC), February 2002
9. “On-Chip and Package Inductance Issues,” half day tutorial with co-presenter Rajendran Panda, ACM/IEEE International Symposium on Quality Electronic Design (ISQED), March 2001
10. “Signal Integrity Analysis in High Performance Design,” full day tutorial with co-presenters Anirudh Devgan, Abhijit Dharchoudhury, ACM/IEEE International Conference on Computer-Aided Design (ICCAD), November 1999
11. “Interconnect-Driven Performance Optimization for Deep Submicron Layout Systems,” full day tutorial with co-presenters Jason Cong, Ren-Song Tsay, ACM/IEEE Design Automation Conference (DAC), June 1997

## C. University Lectures and Seminars Presentations

1. “Razor: Power and Reliability Trade-Offs in DVS,” Invited Presentation, India Institute of Technology (IIT) Mumbay, India, December 2004
2. “Razor: A Low-Power Pipeline Based on Circuit-Level Timing Speculation,” Invited Seminar, University of Delft, Netherlands, August 2004

3. “Dynamic Voltage Scaling Based on Timing Speculation,” Invited Presentation, University of Arizona, October 2003
4. “Statistical Analysis of Circuit Performance,” Distinguished Lecture Series, University of Toronto, April 2003
5. “Signal Integrity in High Performance Design,” Center for Low Power Electronic Seminar Series, University of Arizona, February 2001
6. “Deep Submicron Issues in High Performance Designs,” Microsystems Technology Laboratories Seminar Series, Massachusetts Institute of Technology, October, 2000
7. “CAD Challenges for High-Performance and Low-Power Processor Designs,” Electrical and Computer Engineering Graduate Seminar, University of Illinois, Urbana-Champaign, February 1999
8. “Emerging Deep Submicron Issues in Industrial Designs,” Electrical and Computer Engineering Graduate Seminar, Purdue University, February 1999

### D. Industrial Invited Presentations

1. “Low Voltage Circuits for Ultra Low Energy Consumption,” QualCom Corporation, San Diego, CA, May, 2007
2. “Energy Efficient Computation using Low Voltage Operation,” Sun MicroSystems, Santa Clara, CA, May, 2007
3. “Ultra Low Power Sensor Design using Extreme Voltage Scaling,” Philips Research Laboratory, Eindhoven, Netherlands, August, 2006
4. “Low Power Sensor Design,” Totoya Research Center, Detroit, MI, April, 2006
5. “Subthreshold Processor Design,” Freescale Semiconductor, Austin, TX, January 2006
6. “Computer-Aided Design Methods for Nano-meter VLSI Designs,” Intel Corporation, Strategic CAD Laboratory, Portland, OR, January 2006
7. “Advanced Circuit Design Techniques for Low-Power Design,” Intel Corporation, Circuits Research Laboratory, Portland, OR, January 2006
8. “Subthreshold Design for Low Power Sensor Processors,” ARM Ltd, Cambridge, England, December 2005.
9. “Razor: Low Power and Robust Design using DVS,” Nvidia Design Corporation, San Jose, CA, November 2005
10. “Statistical Timing Analysis: Basic Principles and State-of-the-Art,” CLK Design Automation, Boston, MA, October 2005
11. “Razor: Low Power and Robust Design using DVS,” Freescale Semiconductor, Austin, TX, October 2005
12. “Statistical Performance Analysis and Optimization,” Synopsys Inc, San Jose, CA, February 2005
13. “Circuit Analysis and Optimization Method for High-Performance Design,” Intel Strategic Computer-Aided Design Laboratory, Portland, OR, December 2004
14. “Energy efficient computation using subthreshold operation,” Intel Circuits Research Laboratory, Portland, Oregon, December 2004
15. “Razor Prototype Chip Results,” ARM Ltd, Cambridge England, September 2004
16. “Subliminal Systems, the Final Computing Frontier,” ARM Ltd, Cambridge England, September 2004

17. “Statistical Timing Analysis,” LSI Logic Corporation, May 2004
18. “Analysis and Minimization Techniques for Subthreshold and Gate Oxide Leakage Current,” Intel Circuits Research Laboratory, Portland, Oregon, January 2004
19. “Razor: A Low-Power Pipeline Based on Circuit-Level Timing Speculation,” Intel Circuits Research Laboratory, Portland, Oregon, January 2004
20. “Razor: Dynamic Voltage Scaling Based on Timing Speculation,” IBM Austin Research Laboratory, Austin, Texas, October 2003
21. “Statistical Performance Analysis,” Intel Timing Verification Seminar, Portland Oregon, June 2003
22. “Leakage Analysis for High-Speed Circuits,” Intel Circuits Research Laboratory, Portland, Oregon, May 2003
23. “Statistical Timing Analysis,” Magma Design Automation, December 2003
24. “Performance Analysis of Power-Supply Noise on High-Speed Circuits,” Intel Strategic Computer-Aided Design Laboratory, Portland, Oregon, May 2003
25. “Leakage and Power Analysis for Deep-Submicron VLSI,” Texas Instruments Corp., Dallas, Texas, April 2003
26. “Performance and Power Analysis in High-Performance VLSI Designs,” Motorola Advanced Design Technology Group, Austin, Texas, February 2003
27. “Leakage Analysis and Reduction Methods,” IBM Austin Research Laboratory, Austin, Texas, February 2003
28. “Statistical Timing Analysis for VLSI Design,” IBM Design Automation Professional Interest Seminar, IBM T. J. Watson Research Center, York Town, New York, September 2002
29. “Variability in Chip-Level Performance Analysis,” Intel Performance Verification Seminar, Intel Inc., Haifa, Israel, May 2002
30. “Signal Integrity Methods for Deep Submicron Design,” Cadence Deep-Submicron Design Seminar, Cadence Berkeley Labs, Berkeley, California, December 2001
31. “Signal Integrity Issues in High-Performance Design,” Motorola Internal Conference on Signal Integrity, Austin, Texas, October 2000
32. “Circuit Analysis Techniques,” Motorola Timing Meeting, Motorola, Inc., Tel Aviv, Israel, April 2000

# VII Professional Activities

## A. Professional Societies

- Senior Member of the Institute of Electrical and Electronics Engineers (IEEE).
- Member of the Association of Computing Machinery (ACM).

## B. Editor, Co-Editor, and Associate Editor Positions

- Associate editor, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (*TCAD*), December 2003 - January 2006
- Co-guest editor, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (*TCAD*), special issue on the Design Automation Conference, 2002
- Co-guest editor, *IEEE Design and Test of Computers*, special issue on the Design Automation Conference, 2002

- Co-guest editor, *IEEE Transactions on Very Large Scale Integration Systems* (*T-VLSI*), special issue on Low Power Electronics, 1999

## C. Conference and Workshop Chair Positions

- Panel Chair, ACM/IEEE Design Automation Conference (DAC), 2003
- Co-Chair, technical program committee, ACM/IEEE Design Automation Conference (DAC), 2002
- Co-Chair, technical program committee, ACM/IEEE Design Automation Conference (DAC), 2001
- General Co-Chair, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2000
- Tutorial Chair, ACM/IEEE Design Automation Conference (DAC), 2000
- Co-Chair, technical program committee, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 1999

## D. Consulting

- Weil, Gotshal & Manges, Legal Consulting, 2008 - 2010
- Nascentric, Technical Consulting, 2008
- WilmerHale, Legal Consulting, 2007
- CLK Design Automation (CLK-DA), Technical Consulting, 2005 - 2008

## E. Conference Organization

- Member, technical program committee, IEEE International Solid-State Circuits Conference (ISSCC), 2009
- Member, technical program committee, IEEE International Solid-State Circuits Conference (ISSCC), 2008
- Member, technical program committee, ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), 2007
- Member, technical program committee, IEEE International Solid-State Circuits Conference (ISSCC), 2007
- Member, executive committee, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2006
- Member, technical program committee, IEEE International Solid-State Circuits Conference (ISSCC), 2006
- Member, technical program committee, ACM/IEEE Design Automation Conference (DAC), 2006
- Member, executive committee, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2005
- Member, technical program committee, ACM/IEEE Design Automation Conference (DAC), 2005
- Member, technical program committee, ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), 2005
- Member, executive committee, ACM/IEEE International Symposium on Physical Design (ISPD), 2005
- Member, executive committee, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2004

- Member, technical program committee, ACM/IEEE International Conference on Computer-Aided Design (ICCAD), 2004
- Member, technical program committee, ACM Workshop on Power-Aware Computer Systems (PACS), 2004
- Member, technical program committee, ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), 2004
- Member, technical program committee, ACM/IEEE International Symposium on Physical Design (ISPD), 2004
- Member, executive committee, ACM/IEEE Design Automation Conference (DAC), 2003
- Member, executive committee, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2003
- Member, technical program committee, ACM/IEEE International Conference on Computer-Aided Design (ICCAD), 2003
- Member, technical program committee, ACM/IEEE International Symposium on Physical Design (ISPD), 2003
- Member, executive committee, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2003
- Member, executive committee, ACM/IEEE Design Automation Conference (DAC), 2002
- Member, executive committee, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2002
- Member, technical program committee, ACM/IEEE International Conference on Computer-Aided Design (ICCAD), 2002
- Member, technical program committee, ACM/IEEE International Symposium on Physical Design (ISPD), 2002
- Member, technical program committee, ACM/IEEE Design Automation and Test in Europe Conference (DATE), 2002
- Member, executive committee, ACM/IEEE Design Automation Conference (DAC), 2001
- Member, executive committee, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2001
- Member, technical program committee, IEEE International Conference on Computer Design (ICCD), 2001
- Member, executive committee, ACM/IEEE Design Automation Conference (DAC), 2000
- Member, executive committee, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2000
- Member, technical program committee, ACM/IEEE Design Automation Conference (DAC), 2000
- Member, technical program committee, IEEE International Conference on Computer Design (ICCD), 2000
- Member, technical program committee, ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), 2000
- Member, executive committee, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 1999
- Member, technical program committee, ACM/IEEE Design Automation Conference (DAC), 1999

- Member, technical program committee, IEEE International Conference on Computer Design (ICCD), 1999
- Member, technical program committee, ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), 1999
- Member, technical program committee, ACM/IEEE Design Automation Conference (DAC), 1998
- Member, technical program committee, IEEE International Conference on Computer Design (ICCD), 1998
- Member, technical program committee, ACM/IEEE Workshop on Timing in Synthesis and Specification (TAU), 1998
- Member, technical program committee, ACM/IEEE Design Automation Conference (DAC), 1997

## F. Refereeing and Reviewing

- NSF, SRC, Natural Science and Engineering Research Council of Canada (NSERC)
- IEEE , IEEE T-VLSI, ACM TODAES, IEEE D&T
- DAC, ICCAD, ISLPED, ICCD, ISPD, TAU, DATE, ISCAS, ISQED, PACS